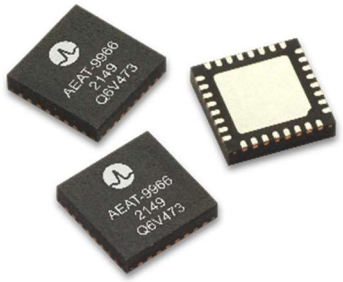
Datasheet

AEAT-9966

Dual Chip Magnetic Encoder IC
10-Bit to 18-Bit Programmable Angular Magnetic Encoder with Safety



Description

The Broadcom AEAT-9966 is a dual/redundancy angular magnetic rotary sensor that provides accurate angular measurement over a full 360 degrees of rotation.
A sophisticated system uses integrated Hall sensor elements with complex analog and digital signal processing within a single device.
A simple two-pole magnet generates the necessary magnetic field by rotating it in perpendicular. Wide magnetic field sensor configurations allow On Axis (end of shaft) or Off Axis (side of shaft, axial and radial) modes in application.
The Broadcom AEAT-9966 is a versatile solution capable of supporting a broad range of applications with its robust architecture to measure and deliver both absolute and incremental signals.
The absolute angle measurement provides an instant indication of the magnet's angular position with a selectable and re- programmable resolution from 10 to 18 bits. When selected, its positioning data is then represented in its digital form to be assessed through a standard SSI (parity) and SPI (with CRC and Parity option) communication protocol. Where desired, users may also choose to receive its absolute angle position in PWM-encoded output signals. The incremental positions are indicated on ABI and UVW signals with wide user configurable resolution from 1CPR and up to 20,000CPR of ABI signals and pole pairs from 1 to 32pole pairs (2 to 64 poles) for UVW commutation signals.

Key Features

- 5V and 3.3V operating voltage
- Operating temperature from –40°C to 125°C
- 2 chips of Magnetic Encoder in one package
- 1mA Current consumption in Sleep mode
- Programmable 10 bits up to 18 bits of absolute resolution
- Programmable Incremental ABI resolution ranging from 1 to 20000CPR
- Commutation angle output UVW 1pp to 32pp
- Absolute output over 2-wire SSI, 3-wire SSI, 4-wire SPI and PWM.
- Dedicated output pin for ABI, UVW and Serial Interface
- Dedicated zero reset and error pin
- EEPROM architecture for multiple-time user programmable
- Optional 56-bit memory lock function
- Automatic integral non-linearity angle correction for high accuracy
- Designed conformance to ISO26262 ASIL-D and SIL3 with secondary chip as redundancy
- Compact QFN-32 leads (5 mm × 5 mm) package

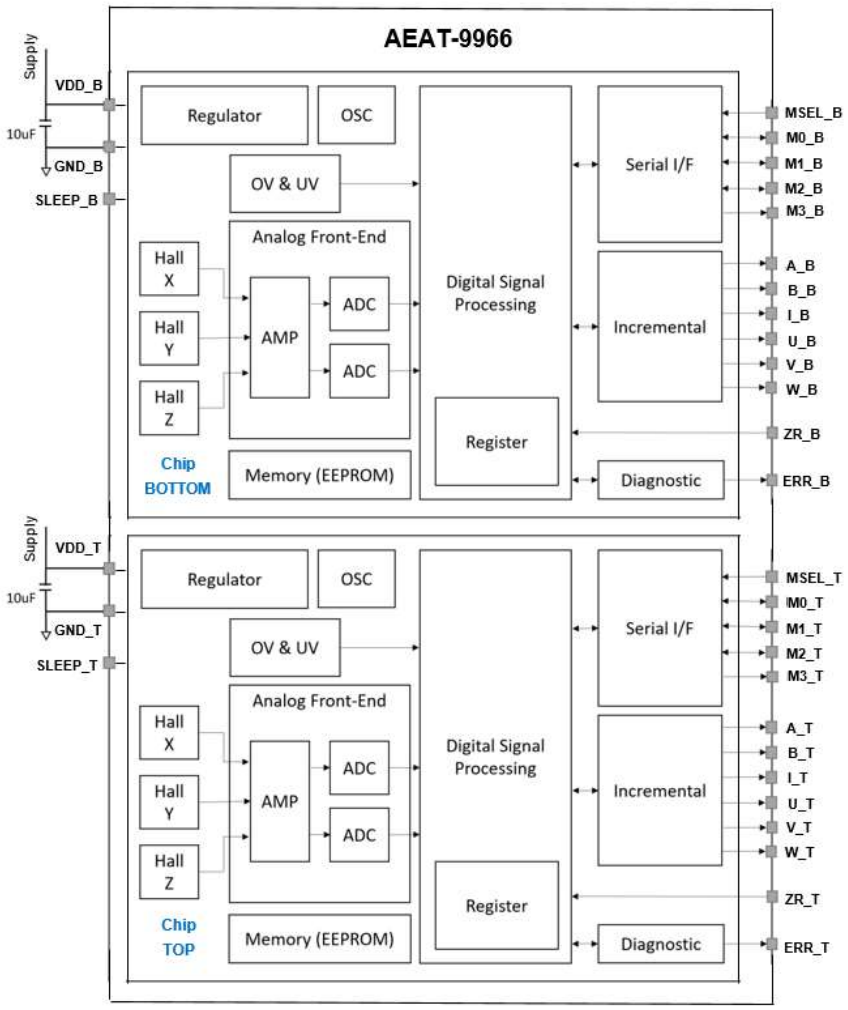
Applications

- Brushless DC motor and stepper motor
- Resolver and potentiometer replacement
- Industrial automation and robotics
- Industrial sewing machine and textiles equipment
- Light Detection and Range (LiDAR)

NOTE This product is not specifically designed or manufactured for use in any specific device. Customers are solely responsible for determining the suitability of this product for its intended application and solely liable for all loss, damage, expense, or liability in connection with such use.

Functional Description

Figure 1 AEAT-9966 Block Diagram



The AEAT-9966 integrate with two identical magnetic encoder chip in one package. Each chip is independent.

The AEAT-9966 is manufactured with a CMOS standard process. It is capable of accurately measuring a magnet's rotational angle when it is placed in alignment and in perpendicular to the device by using its integrated Hall sensors to detect its magnetic field. The detected magnetic signals are then taken as input signals to be properly conditioned to negate its non-idealities before inputting them into the analog amplifiers for strength amplification and filtering. After which, the amplified analog signals are then fed into the internal analog-to-digital converter (ADC) to be converted into digital signals for the final stage of digital processing.

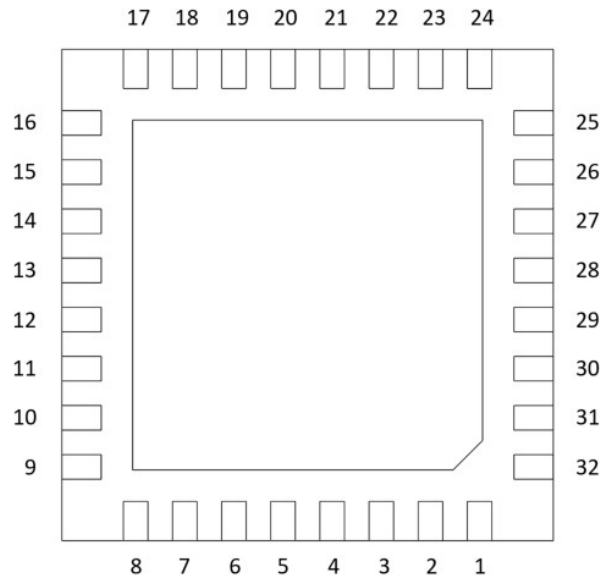
The digital processing provides a digitized output of the absolute and incremental signals.
The used magnet should have sufficient magnetic field strength mT to generate the magnetic field for the signal generation as highlighted in the Recommended Magnetic Input Specifications section. The device provides digital information of magnetic field strength high MHi and magnetic field strength low MLo from output protocols to indicate whether the magnets are too close or too far away from our device's surface.

Users can assess the device's digitized absolute data using standard Synchronous Serial Interface (SSI) or Serial Peripheral Interface (SPI) protocols. In addition, an absolute angular representation also can be selected using a pulse width modulated (PWM) signal.

The incremental outputs are available from digital outputs of their dedicated A, B, and I pins as well as the commutation output U,V and W.

Pin Assignment

Figure 2 Pin Configurations



Pinout Description

Pin QFN32	Pin Name	Description	Pin QFN32	Pin Name	Description
1	ZR_T	Sleep Mode (Chip Top)	17	ZR_B	Zero Reset (Chip Bottom)
2	M0_B	Serial Interface M0 (Chip Bottom)	18	M0_T	Serial Interface M0 (Chip Top)
3	ERR_T	Error (Chip Top)	19	ERR_B	Error (Chip Bottom)
4	M1_B	Serial Interface M1 (Chip Bottom)	20	M1_T	Serial Interface M1 (Chip Top)
5	MSEL_T	Interface Select (Chip Top)	21	MSEL_B	Interface Select (Chip Bottom)
6	M2_B	Serial Interface M2 (Chip Bottom)	22	M2_T	Serial Interface M2 (Chip Top)
7	M3_B	Serial Interface M3 (Chip Bottom)	23	M3_T	Serial Interface M3 (Chip Top)
8	A_B	Incremental A (Chip Bottom)	24	A_T	Incremental A (Chip Top)
9	B_B	Incremental B (Chip Bottom)	25	B_T	Incremental B (Chip Top)
10	I_B	Incremental I (Chip Bottom)	26	I_T	Incremental I (Chip Top)
11	U_B	Commutation U (Chip Bottom)	27	U_T	Commutation U (Chip Top)
12	VSS_T	Ground supply (Chip Top)	28	VSS_B	Ground supply (Chip Bottom)
13	V_B	Commutation V (Chip Bottom)	29	V_T	Commutation V (Chip Top)
14	VDD_T	Power supply (Chip Top)	30	VDD_B	Power supply (Chip Bottom)
15	W_B	Commutation W (Chip Bottom)	31	W_T	Commutation W (Chip Top)
16	SLEEP_B	Sleep Mode (Chip Bottom)	32	SLEEP_T	Sleep Mode (Chip Top)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	125	°C	
DC Supply Voltage VDDA pin	VDD_B VDD_T	 -0.3	 6.06	 Volts	
Input Voltage Range	V_{in}	-0.3	6	Volts	
Electrostatic Discharge (HBM)		-4.0	+4.0	kVolts	
Moisture Sensitivity Level		-	1		

CAUTION Subjecting the product to stresses beyond those listed in this section may cause permanent damage to the devices. These are stress ratings only and do not imply that the devices will function beyond these ratings. Exposure to the extremes of these conditions for extended periods may affect product reliability.

Electrical Characteristics

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Ambient Temperature	T_A	-40	–	125	°C	
DC Supply Voltage to VDD pin 5V operation 3.3V operation	VDD_B VDD_T	 4.5 3.0	 5.0 3.3	 5.5 3.6	 Volts	
Incremental Output Frequency	f_{MAX}	–	–	1.0	MHz	Frequency = Velocity(rpm) x CPR/60
Load Capacitance	C_L	–	–	15	pF	

Systems Parameters

Condition: Electrical characteristics over the recommended operating conditions. Typical values specified at VDD = 5.0V and 25°C, optimum placement of magnet, and both chips are tied to same supply VDD and control SLEEP

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Current Consumption						
Supply Current Normal Operation Mode	IDD_{NOM}	–	48	-	mA	5V
	IDD_{NOM}	–	44	-	mA	3.3V
Supply Current Sleep Mode	IDD_{IDLE}	–	700	-	uA	5V & 3.3V
Digital Outputs (DO)						
High Level Output Voltage	V_{OH}	VDD - 0.5	–	–	Volts	Normal operation
Low Level Output Voltage	V_{OL}	–	–	GND + 0.4	Volts	
Power-up time Absolute Output Incremental Output PWM Output	t_{PwrUp}	–	10	-	ms	

Digital Inputs (DI)						
Input High Level	V_{IH}	0.7xVDD	–	–	Volts	
Input Low Level	V_{IL}	–	–	0.3xVDD	Volts	
Pull-up low level input current	I_{IL}	–	–	120	µA	
Pull-down high level input current	I_{IH}	–	–	120	µA	

Encoding Characteristics

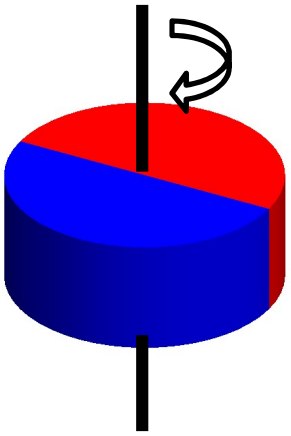
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Absolute Output						
Resolution	RES	10		18	Bit	Programmable 10 to 18 bits
Integral Non-Linearity ON-axis	INL_{nom}	–	+/-0.05	–	Deg	Best fit line, centered magnet. T_A = 25°C Voltage = 5V INL Angle correction
Integral Non-Linearity OFF-axis		–	+/-0.15	–		
Integral Non-Linearity ON-axis	INL_{dis}	–	+/-0.15	–	Deg	Best fit line, over displacement of magnet. T_A = 25°C Voltage = 5V
Integral Non-Linearity OFF-axis		–	+/-0.25	–		
Integral Non-Linearity ON-axis	INL_{temp}	–	+/-0.10	–	Deg	Best fit line, over temperature range T_A = –40 to +125°C Voltage = 5V
Integral Non-Linearity OFF-axis		–	+/-0.40	–		
Differential Non-Linearity	DNL_{nom}		+/-0.02		Deg	T_A = 25°C Voltage = 5V
Output Sampling Rate	f_S	–	10	–	MHz	Based on SSI protocol
Latency		–	80	–	ns	At constant speed
Incremental Output (Channel ABI)						
Resolution	R_{INC}	1	–	20000	CPR	Programmable
Index Pulse Width	P_O	90	–	360	°e	Programmable options: 90, 180, 270, or 360 °e. Refer to diagram page 20
Index Pulse State	P_S	90	–	360	°e	Relation between Index output to Incremental AB state. Programmable options: 0, 90, 180, or 270°e. Refer to diagram page 20
Index State		90	–	360	°e	Programmable options: 90, 180, 270, or 360 °e. Refer to diagram page 20
PWM Output						
PWM frequency	f_{PWM}	122		976	Hz	Adjustable based on our PWM settings
Minimum pulse width	PW_{MIN}		1		µs	
Maximum pulse width	PW_{MAX}		16384		µs	

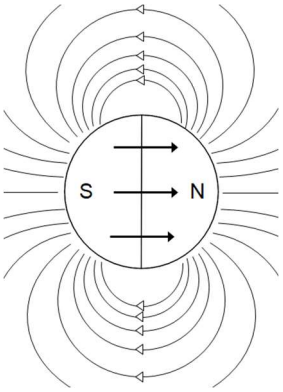
NOTE Encoding Characteristics over Recommended Operating Range unless otherwise specified. Applied for both chips

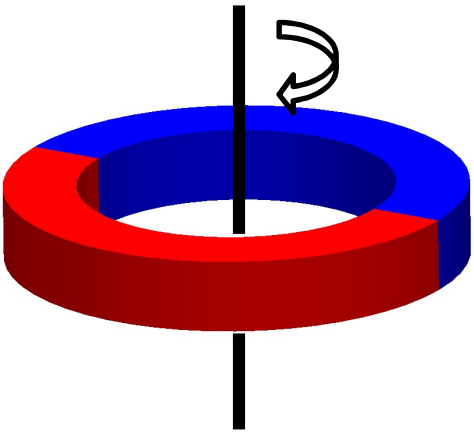
Recommended Magnetic Input Specifications

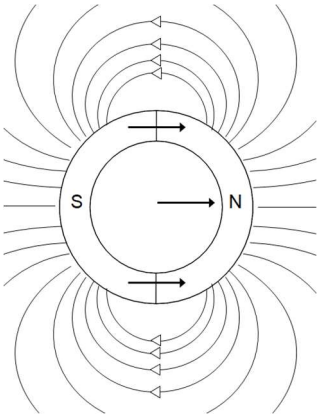
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Diameter Disc magnet Ring magnet ID /OD	d	 4 -	 6 ID,15 OD,25	 - -	 mm mm mm	Recommended magnet: Cylindrical magnet or ring magnet diametrically magnetized & 1 pole pair.
Thickness Disc magnet Ring magnet	t	 - 2	 2.5 6	 - -	 mm mm	
Magnetic input filed magnitude On-axis (Disc Magnet) Off-axis (Ring Magnet)	Bpk	 45 30	 - -	 100 150	 mT mT	Required vertical/horizontal component of the magnetic field strength on the die's surface, measured along concentric circle.
Magnet displacement radius	R_m			0.25	mm	Displacement between magnet axis to the device center
Recommended magnet material and temperature drift			-0.12		%/K	NdFeB (Neodymium Iron Boron),grade N35SH

Diametrically Magnetized Magnet





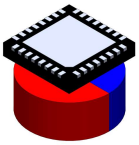
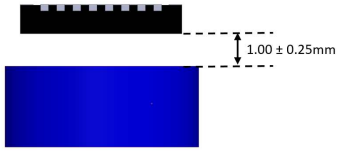
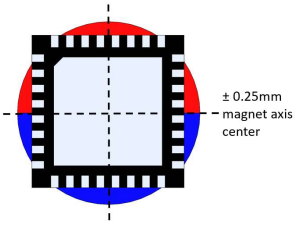
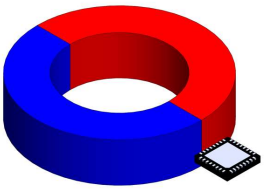
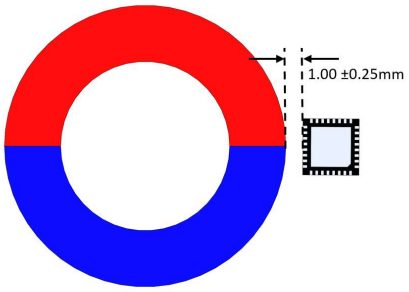
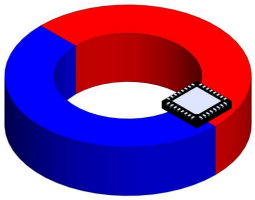
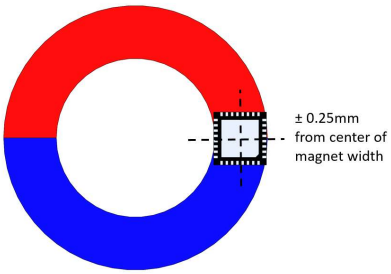
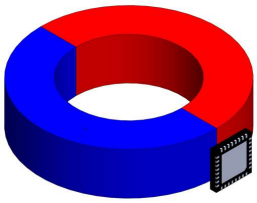
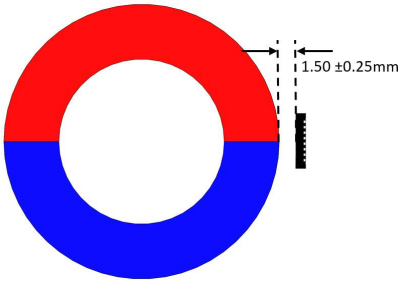




Magnet and IC Package Placement

AEAT-9966 multi-axis capability comes from multiple integrated hall devices that allows flexibility on the sensor mounting with respect to the magnet. Generally, the shaft end configuration senses the vertical field (Z-component perpendicular to chip surface) and the rest of the configuration senses the horizontal field (X and Y components parallel to the chip surface).
The nominal mounting tolerance is indicated the table below.

Chip illustration: Chip 1 in the bottom and Chip 2 in the top

Configuration	Gap tolerance	X-Y tolerance
Shaft End 		
Side Shaft 		
Axial 		
Radial 		

Communication Protocol

Important Note: Two chips are independence; subsequence explanation and definition are based on one chip.

Serial Interface Format

AEAT-9966 serial interface host up to 10 different protocols for position output and memory access. The protocol is configurable with the combination of physical I/O **MSEL** and **M0** and memory settings **PSEL**, **SPI4[0]** and **SPI4[1]**. The default factory settings is all zero in which it is either **SPI3** or **SPI4-16a** depending on **MSEL** state.
All of the protocols selection can be switched during operation.

MATS Table (UVW Mode -> M1=U & M2=V)

Mode / Pin	SPI3	SSI3a	SSI3b	SSI2a	SSI2b	SPI4-16a	SPI4-16b	SPI4-16c	SPI4-8	PWM
MSEL	0	0	0	0	0	1	1	1	1	1
PSEL	x	0	1	0	1	0	0	0	0	1
SPI4[1]	x	x	x	x	x	0	0	1	1	x
SPI4[0]	x	x	x	x	x	0	1	0	1	x
M0	0	1	1	1	1	NCS	NCS	NCS	NCS	-
M1	DIN	NSL	NSL	0	0	MOSI	MOSI	MOSI	MOSI	-
M2	SCK	SCL	SCL	SCL	SCL	SCK	SCK	SCK	SCK	-
M3	DO	DO	DO	DO	DO	MISO	MISO	MISO	MISO	PWM

NOTE PSEL, SPI4[1], SPI4[0] are configure through memory

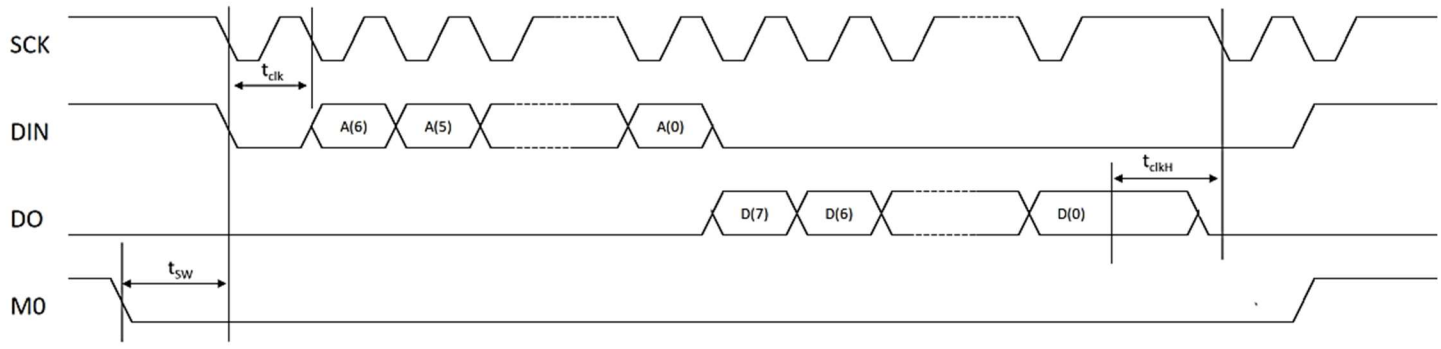
MSEL, M0 are configure through IO pads

Serial Peripheral Interface (SPI3)

SPI3 protocols only allow access to memory read write. Assert 0 on **MSEL** and **M0** pin to configure it. The SPI is implemented with CPOL=0 and CPHA=0, data is propagated on the clock falling edge.

- M1 → SPI_Data Input (DIN) signal for SPI protocol, input to AEAT-9966
- M2 → SPI_Clock Input (SCK) signal for SPI protocol, input to AEAT-9966
- M3 → SPI_Data Output (DO) signal for SPI protocol, output from AEAT-9966

SPI3 Timing Diagram

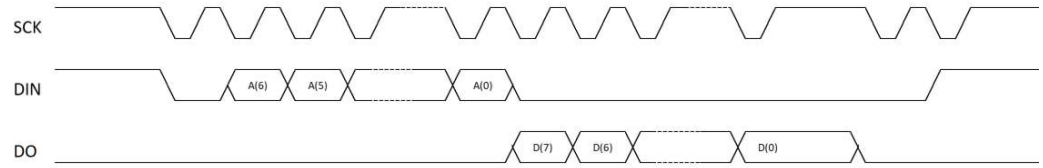


Symbol	Description	Min	Typ	Max	Unit
t_{SW}	Time between SCn falling edge and CLK rising edge	1	-	-	us
t_{clk}	Serial clock period	-	-	100	ns
t_{clkH}	CLK high time after end of last clock period	300	-	-	ns

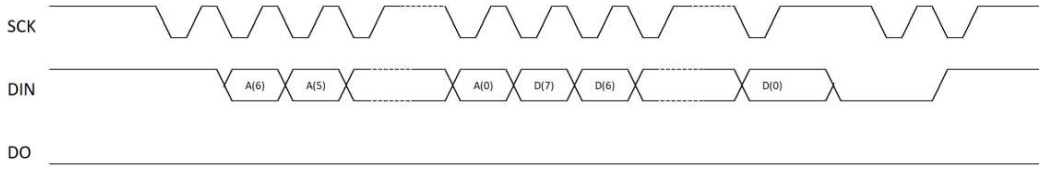
NOTE

- The user should read back data to confirm data is written successfully

SPI3 Read



SPI3 Write

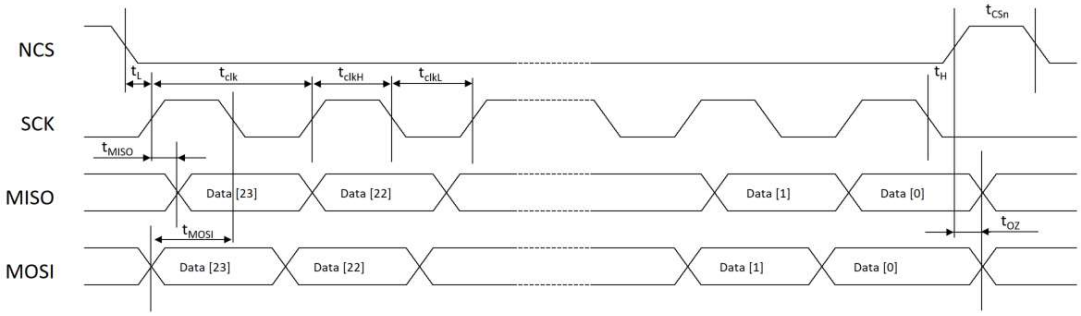


Serial Peripheral Interface (SPI4)

SPI protocol uses four pins from AEAT-9966. These four pins are shared between UVW, SSI, SPI protocols. MSEL (input pin) selects either protocol at a time. Assert 1 on MSEL pin to select the SPI4 protocol.
SPI4 protocols allow user to access memory read or write and position data. It uses CPOL=0, CPHA=1 for triggering.

- M0 → SPI_Chip Select (NCS) signal for SPI protocol, input to AEAT-9966
- M1 → SPI_Data Input (MOSI) signal for SPI protocol, input to AEAT-9966
- M2 → SPI_Clock Input (SCK) signal for SPI protocol, input to AEAT-9966
- M3 → SPI_Data Output (MISO) signal for SPI protocol, output from AEAT-9966

SPI4 Timing Diagram



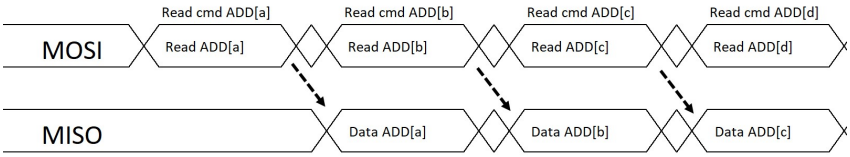
Symbol	Description	Min	Typ	Max	Unit
t_L	Time between SCn falling edge and CLK rising edge	350			ns
t_{clk}	Serial clock period	100			ns
t_{clkL}	Low period of serial clock	50			ns
t_{clkH}	High period of serial clock	50			ns
t_H	Time between last falling edge of CLK and rising edge of CSn	$t_{clk/2}$			ns
t_{CSn}	High time of CS between two transmission	350			ns
t_{MOSI}	Data input valide to clock ege	20			ns
t_{MISO}	CLK edge to data output valid		51		ns
t_{OZ}	Time between CSn rising dege and MISO HiZ		10		ns

NOTE

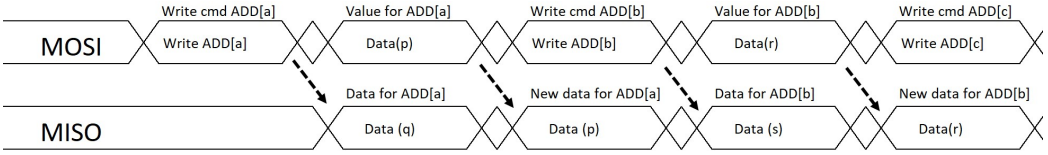
- The user should read back data to confirm data is written successfully

SPI4 Command and Data Frame

SPI4 Read sequence



SPI4 Write sequence



SPI-4(A) 16-bit (Parity)

By default the chip is configured to SPI4 16-bit selection, **PSEL = 0, SPI4[1] = 0, SPI4[0] = 0** in the register setting.

	Data Format																			
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Master to Slave					P	RW	0	0	0	0	0	0	Addr/Data[7:0]							
Slave to Master (memory)					P	EF	0	0	0	0	0	0	Data[7:0]							
Slave to Master (pos 10b)					P	EF	Pos[9:0]										0	0	0	0
Slave to Master (pos 11b)					P	EF	Pos[10:0]											0	0	0
Slave to Master (pos 12b)					P	EF	Pos[11:0]												0	0
Slave to Master (pos 13b)					P	EF	Pos[12:0]													0
Slave to Master (pos 14b)					P	EF	Pos[13:0]													
Slave to Master (pos 15b)				P	EF	Pos[14:0]														
Slave to Master (pos 16b)			P	EF	Pos[15:0]															
Slave to Master (pos 17b)		P	EF	Pos[16:0]																
Slave to Master (pos 18b)	P	EF	Pos[17:0]																	

P: Parity

EF: Error Flag

RW: Read = 1, Write = 0

SPI4-(B) 24-bit (CRC)

To configure the chip to SPI4 24-bit selection, set **PSEL = 0, SPI4[1] = 0, SPI4[0] = 1** in the register setting.

	Data Format																								
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Master to Slave					0	RW	0	0	0	0	0	0	Addr/Data[7:0]								CRC[7:0]							
Slave to Master (memory)					W	E	0	0	0	0	0	0	Data[7:0]								CRC[7:0]							
Slave to Master (pos 10b)					W	E	Pos[9:0]										0	0	0	0	CRC[7:0]							
Slave to Master (pos 11b)					W	E	Pos[10:0]											0	0	0	CRC[7:0]							
Slave to Master (pos 12b)					W	E	Pos[11:0]												0	0	CRC[7:0]							
Slave to Master (pos 13b)					W	E	Pos[12:0]													0	CRC[7:0]							
Slave to Master (pos 14b)					W	E	Pos[13:0]														CRC[7:0]							
Slave to Master (pos 15b)				W	E	Pos[14:0]															CRC[7:0]							
Slave to Master (pos 16b)			W	E	Pos[15:0]																CRC[7:0]							
Slave to Master (pos 17b)		W	E	Pos[16:0]																	CRC[7:0]							
Slave to Master (pos 18b)	W	E	Pos[17:0]																		CRC[7:0]							

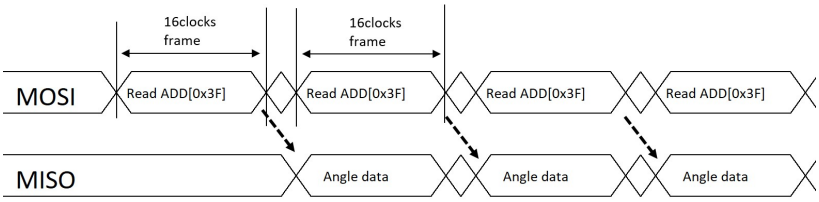
W: Warning

E: Error

RW: Read = 1, Write = 0

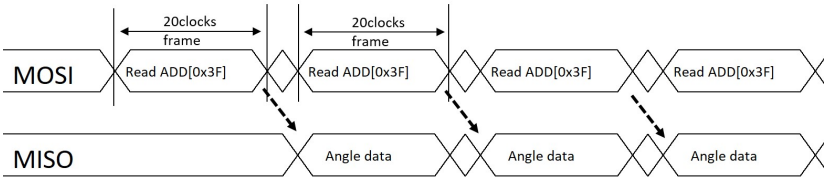
Position Read

Absolute position data can be obtain by sending read command to address **0x3F.**



In the event of higher single turn resolution (15-bit and above), the command and data frame size is adjusted accordingly.

Example: 18bit + 2bit (parity and error)



Serial Synchronous Interface 3-wire (SSI3)

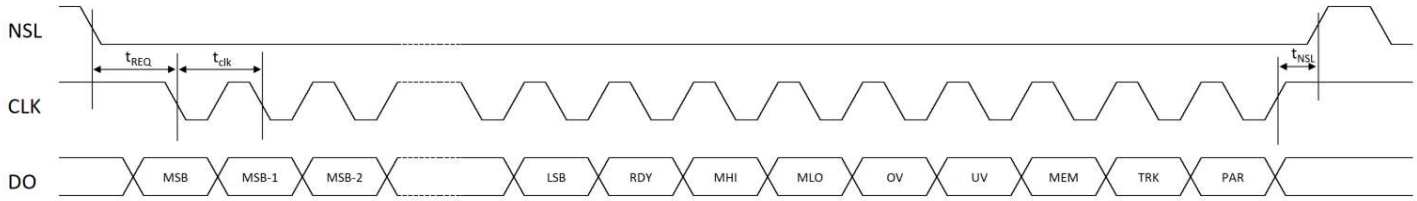
SSI3 protocol uses three pins from AEAT-9966. These three pins are share between UVW, SSI, SPI protocols. MSEL (input pin) selects either protocol at a time. Assert 0 on **MSEL** pin and 1 on **M0** pin to select the SSI protocol.

- M1 → SSI_NSL Input (NSL) signal for SSI protocol, input to from AEAT-9966
- M2 → SSI_Clock Input (CLK) signal for SSI protocol, input to AEAT-9966
- M3 → SSI_Data Output (DO) signal for SSI protocol, output from AEAT-9966

It is available in 2 options per PSEL register setting:

Figure 6 SSI Protocol Timing Diagram

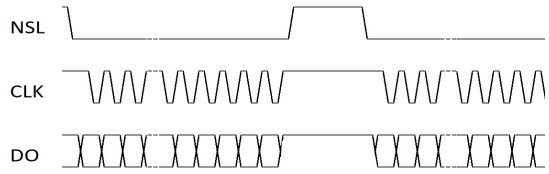
Default : Data Output with 3 wire SSI to 10Mhz clock rates



Symbol	Description	Min	Typ	Max	Unit
tclk	SSI_SPI_SEL switch time	1	-	-	Us
tREQ	SCL hight time between NLS falling edge and first SCL falling edge	300	-	-	ns
tNSLH	NSL high time between 2 successive SSI reads	200	-	-	ns

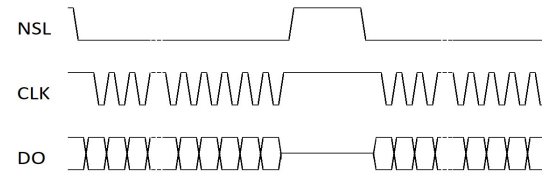
SSI-3(A)

By default the chip is configured to SSI-3(A) selection, **PSEL = 0** in the register setting.
DO pin is held at high state once NSL pin is high



SSI-3(B)

To configure chip to SSI-3(B) selection, **PSEL = 1** in the register setting.
DO pin is tristate (high impedance) state once NSL pin is high

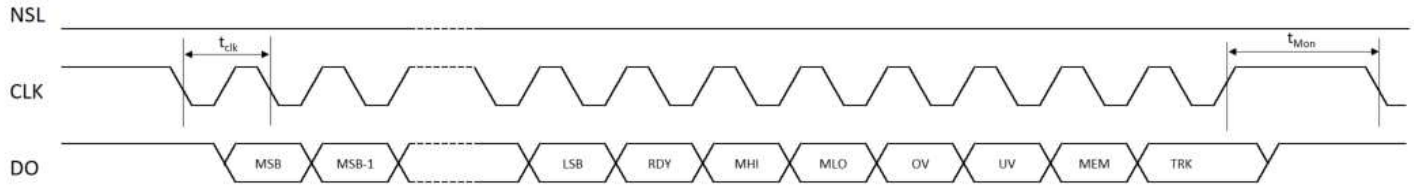


Serial Synchronous Interface 2-wire (SSI2)

SSI2 protocol uses two pins from AEAT-9966. These two pins share between SSI, SPI protocols. MSEL (input pin) selects either protocol at a time. Assert 0 on **MSEL** & **M1** pin and 1 on **M0** pin upon power up.

- M2 → SSI_Clock Input (CLK) signal for SSI protocol, input to AEAT-9966
- M3 → SSI_Data Output (DO) signal for SSI protocol, output from AEAT-9966

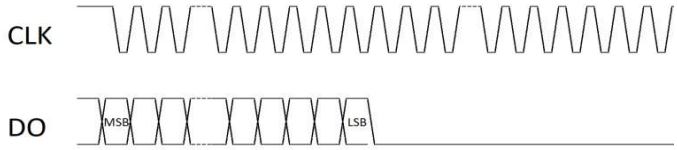
Depending on the PSEL setting, it can be configured as SSI2(A) Ring Mode or SSI2(B) No Ring Mode.
Data is latched on the first CLK falling edge and transmit on the next falling edge.
Reconfirm rising/falling?



Symbol	Description	Min	Typ	Max	Unit
tClk	NSL low time after rising edge of last clock period for an SSI read	250	-	tM/2	ns
tM	NSL high time between 2 successive SSI reads	-	16.5	18.0	us

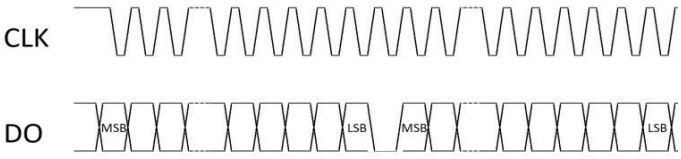
SSI-2(A)

By default the chip is configured to SSI-2(A) selection, **PSEL = 0** in the register setting.
Output single data position and remains low after LSB until the next monoflops (tM) expires.

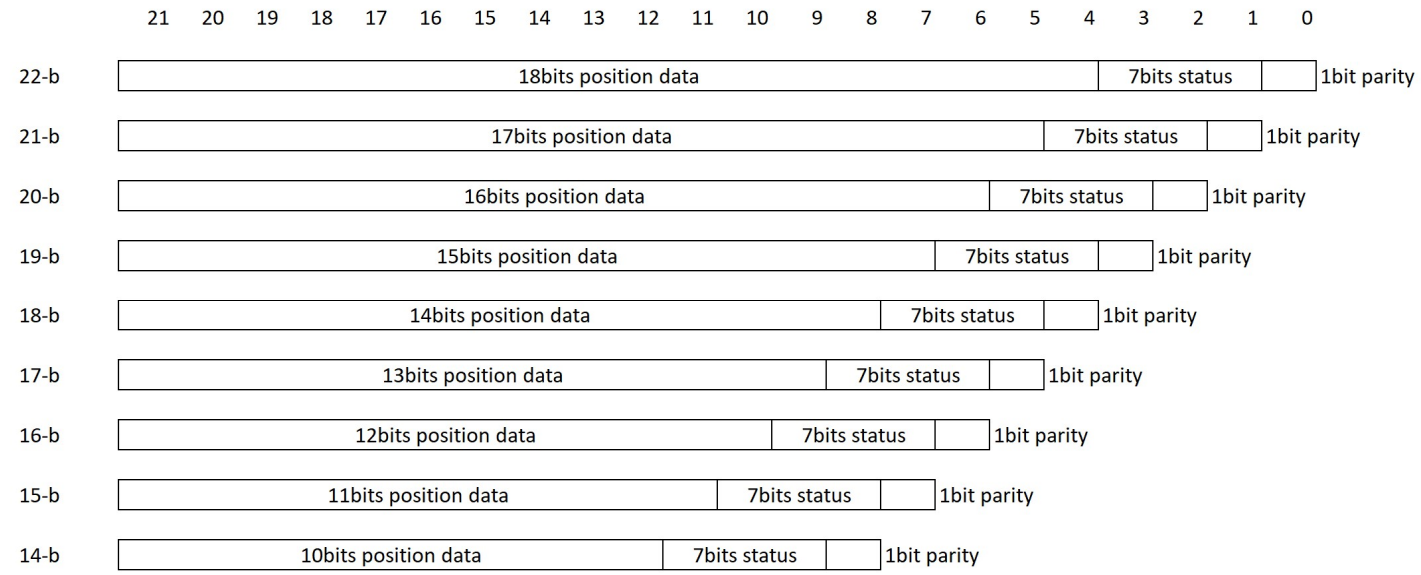


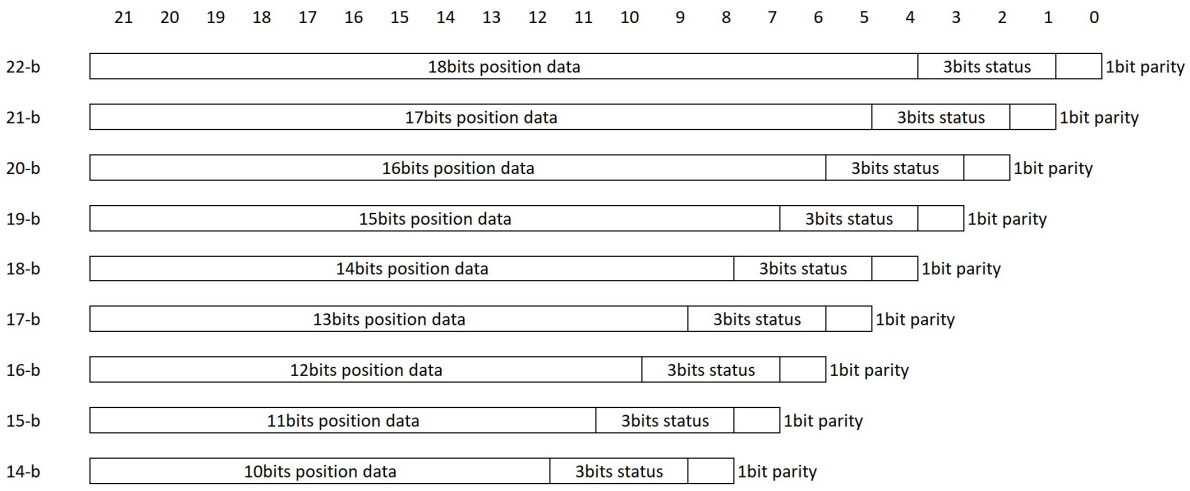
SSI-2(B)

To configure chip to SSI-2(B) selection, **PSEL = 1** in the register setting.
The same position data can be continuously output by sending clock train and data is separated by a single low pulse.
Data will be refresh on the next monoflop (tM) expires.



SSI READ Data Format





NOTE

- 7-b status: {Ready, MHI, MLO, OV, UV, Mem, Trck}
- Refer to Status and Warning section for more details

Safety and Non-safety protocol format

The position serial interfaces is available in Safety and Non-safety format; applicable for SSI3, SSI2 and SPI-8.

Position (n-bit)	Status / Alarm (7-bit)							Parity (1-bit)
Position[(n-1):0]	READY	MHI	MLO	OV	UV	MEM	TRK	parity

Position (n-bit)	Status / Alarm (8-bit)						SC (8-bit)	CRC (8/16-bit)
Position[(n-1):0]	Status[1:0] (1)	MHI	MLO	OV	UV	MEM	TRK	SC [7:0] (2)	CRC [7/15:0] (3)

NOTE

1. 2-bit status to indicate the safety status
    i. Status = 2b'00 : Encoder not ready
    ii. Status = 2b'01 : Encoder not ready, Force test failed
    iii. Status = 2b'10 : Encoder not ready
    iv. Status = 2b'11 : Encoder not ready, Force test passed
2. SC denotes as "Sequence Count" or life counter that automatically increment on every position transmission. The counting starts from 1 to 255 and the initial value upon power up is configurable.
3. CRC poly 0x1021 or 0x1D, initial value is configurable (0x0000, 5555, AAAA, FFFF)

Status and Alarm

Error bit is trigger if either Magnet High (MHI), Magnet Low (MLO), Memory Error (MEM_Err) or communication error.

Details of error bit is available in register address below:

Address	bit							
	7	6	5	4	3	2	1	0
0x21	RDY	MHI	MLO	OV	UV	MEM	TRK	

- **Ready:** The chip is ready, and the ready value is 1.
- **Parity :** 1-b parity is even parity.
- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is flag high consistently, change the weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is flag high consistently, change the stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Overvoltage (OV) Error:** This indicates that the input supply has exceeded above the limit. When this is flag high consistently, check the supply line. The value for this alarm is represented as 1.
- **Undervoltage (UV) Error:** This indicates that the input supply has dropped below the limit. When this is flag high consistently, check the supply line. The value for this alarm is represented as 1.
- **Memory Error (MEM) Error:** This indicates that the memory corruption has occurred. When this is flag high, perform power cycle to reload the memory. The value for this alarm is represented as 1.
- **Tracker (TRK) Error:** This indicates that the angular error exceed 5° within 5ms. When this is flag high consistently, perform power cycle to re-initialize the sensor. The value for this alarm is represented as 1.

Power Modes

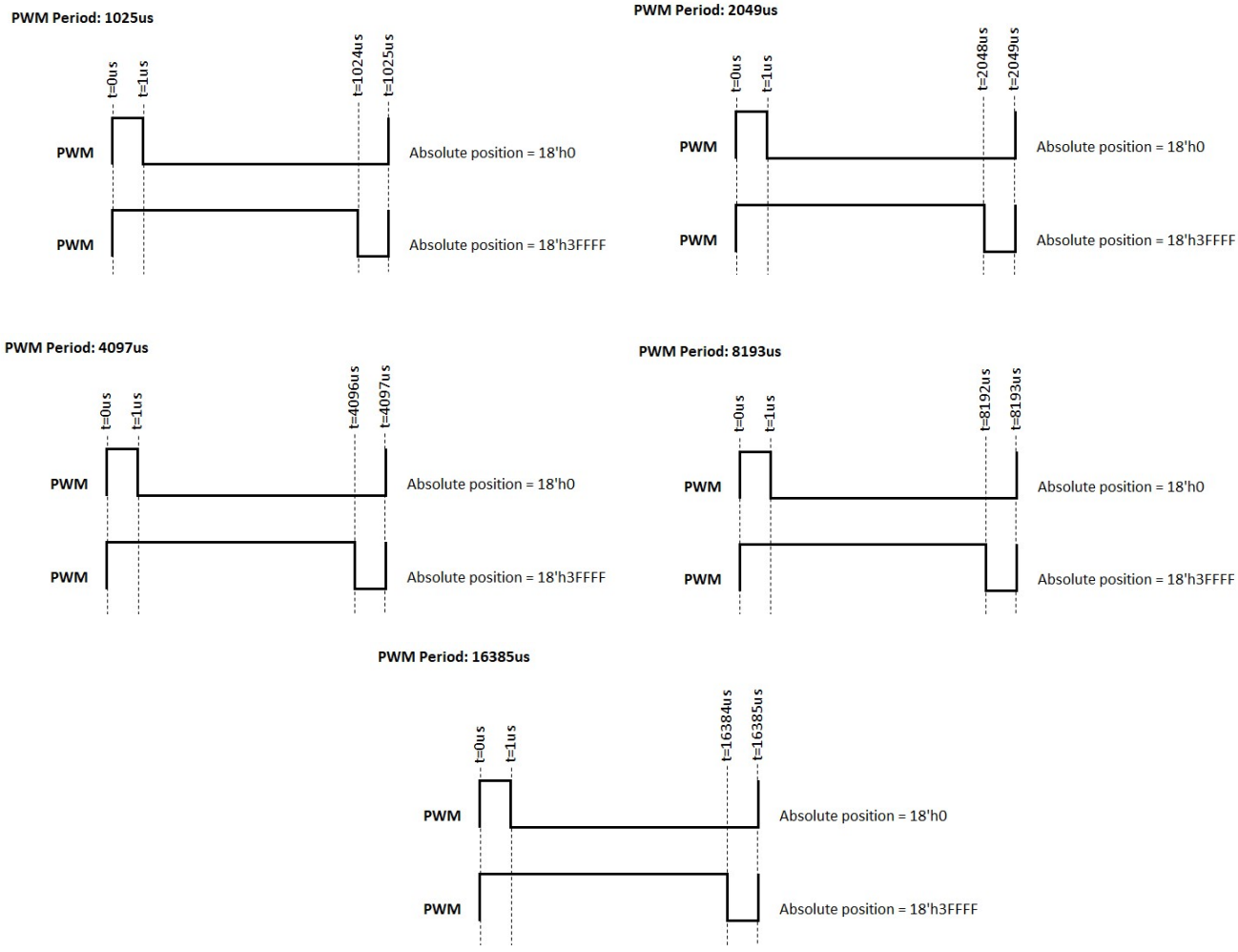
AEAT-9966 is design with 2 power modes; (1) **Active Mode** where the chip operates under full functions with normal current consumption, IDD_{NOM}. (2) **Sleep Mode** powered down the chip front-end and digital processing blocks, only the detection block to track on user input with low current consumption, IDD_{IDLE}.

PWM

PWM protocol uses one output pin (W_PWM) from AEAT-9966. Note that W_PWM pin is shared between UVW and PWM protocols. The PWM signals are configurable to have period of 1025, 2049, 4097, 8193 or 16385 µs. During power-up, the PWM signal is 0 before chip ready.

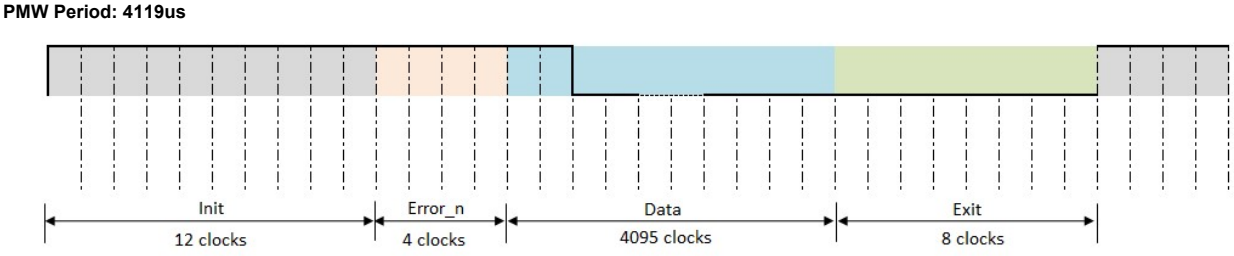
PWM Signals (Period = 1025/2049/4097/8193/16385 µs)

- PWM period: 1025, 2049, 4097, 8193, 16385 µs



PWM protocols is also available in with Init, Error_n, and Exit along with Data information.

PWM Signals (Period = 1047/2071/4119/8215/16407 µs)



Incremental Output Format

The AEAT-9966 provides ABI and UVW signals to indicate incremental position of the motor.

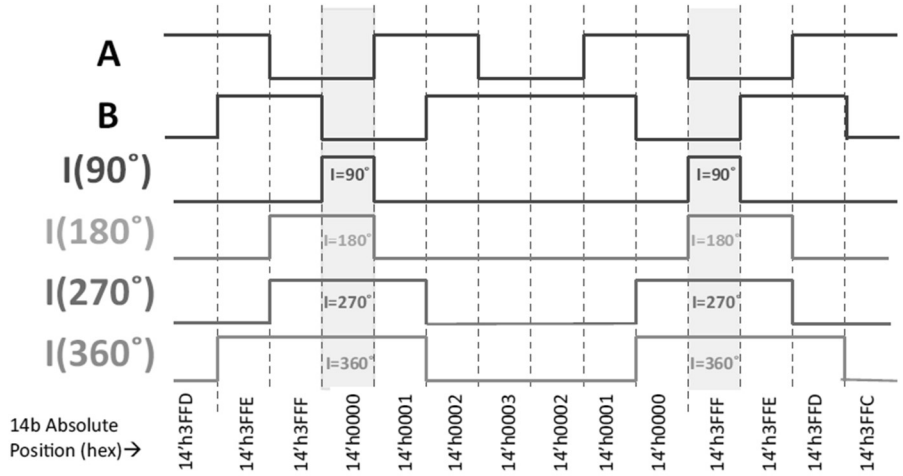
ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B, and I).

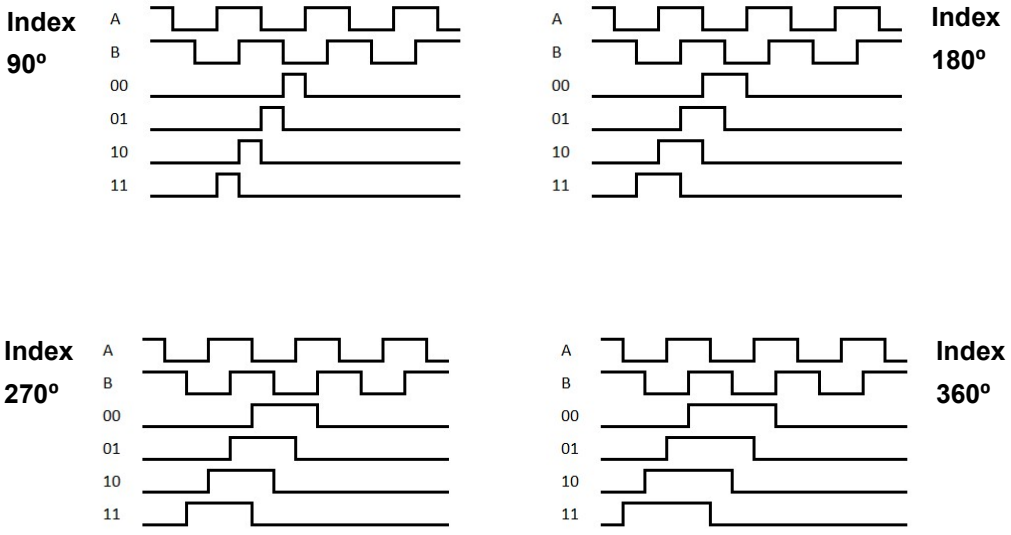
The index signal marks the absolute angular position and typically occurs once per revolution The ABI signal is configurable using the memory map registers. It supports the following configuration:

- Programmable CPR: 1 to 20000CPR
- Programmable I-width: 90, 180, 270, or 360 electrical degrees (edeg)
- Programmable I-State : 90, 180, 270, or 360 electrical degrees (edeg)

Figure 7 ABI Signal (4096 CPR, with Different I-Width Settings), Assuming User Sets Hysteresis at 0.02 Mechanical Degree



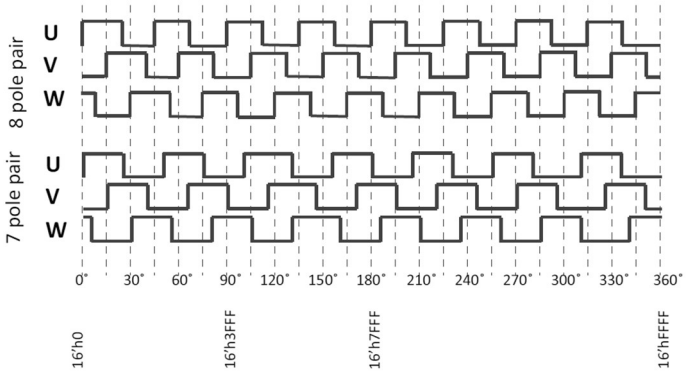
The Index position is configurable among the incremental state.
Index signal raise high once per turn at absolute zero position.

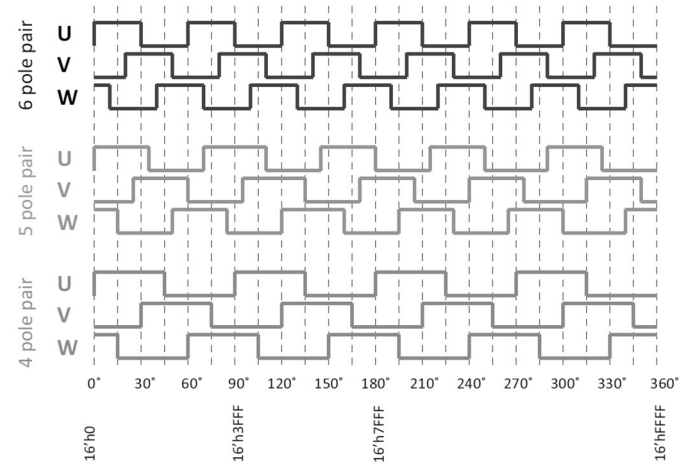


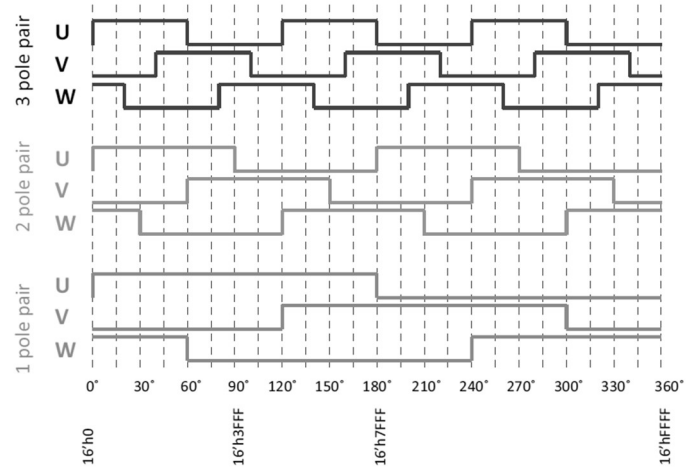
UVW

Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback and is available using three output pins. Note that W_PWM pin is shared between the UVW and PWM protocols.

AEAT-9966 can configure pole pairs from 1 to 3232 equivalents to 2 to 6464 poles.

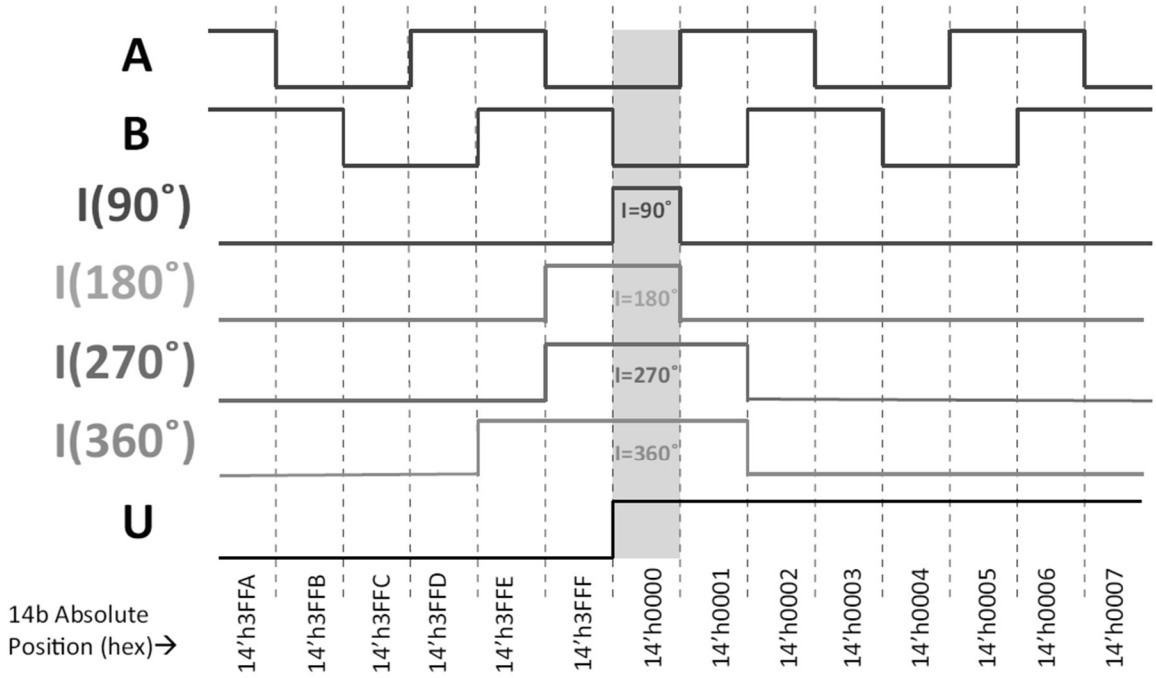






Note that signal U from UVW protocol is tagged to signal I from the ABI protocol as shown in the following figure.

Figure 8 U-to-I Tagging



Package Drawings (in mm)

Figure 9 AEAT-9966, 32 QFN Dimensions

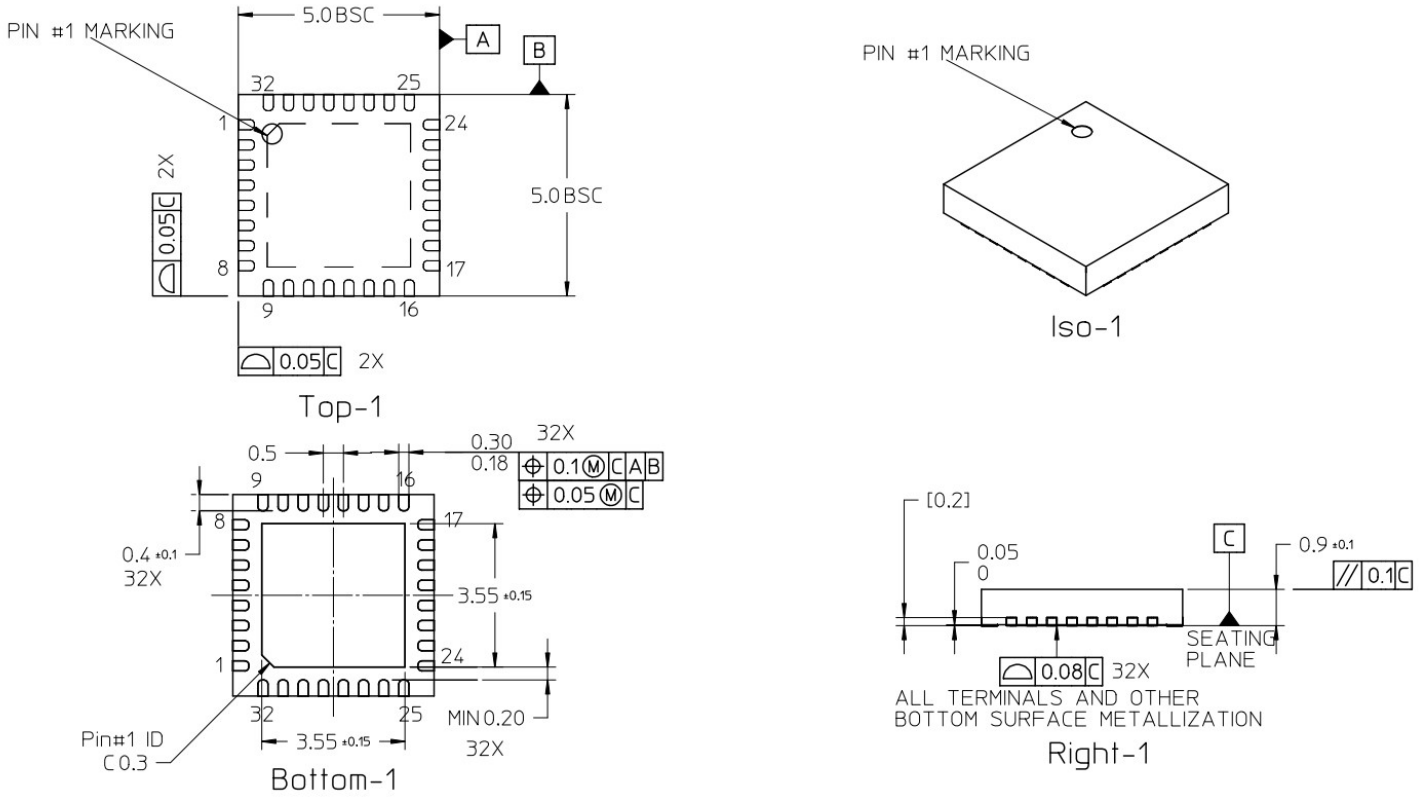
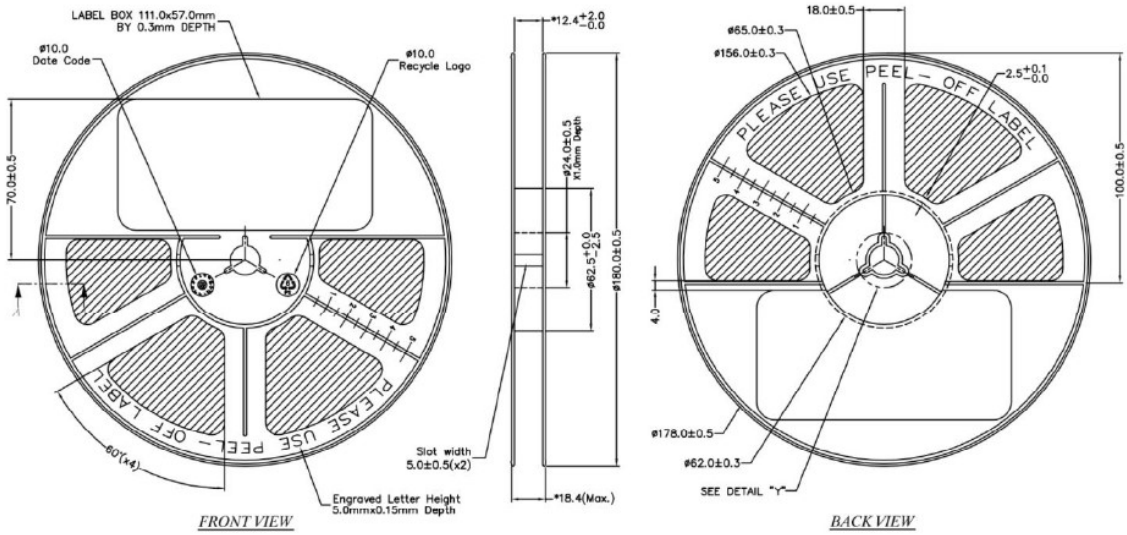


Figure 10 Reel Dimensions



Product Ordering Information

Ordering Part Number	Product Description	Package	Delivery Form
AEAT-9966-100	18Bits Dual Magnetic Encoder On-Off Axis Tape Reel 1000	QFN 32 leads, 5 mm × 5 mm	Tape & Reel
AEAT-9966-102	18Bits Dual Magnetic Encoder On-Off Axis Tape Reel 100	QFN 32 leads, 5 mm × 5 mm	Tape & Reel
AEAT-9966-Q32	18Bits Dual Magnetic Encoder On-Off Axis	QFN 32 leads, 5 mm × 5 mm	Tube