

GaAs HBT PROGRAMMABLE 5-BIT COUNTER, DC - 2.2 GHz



Typical Applications

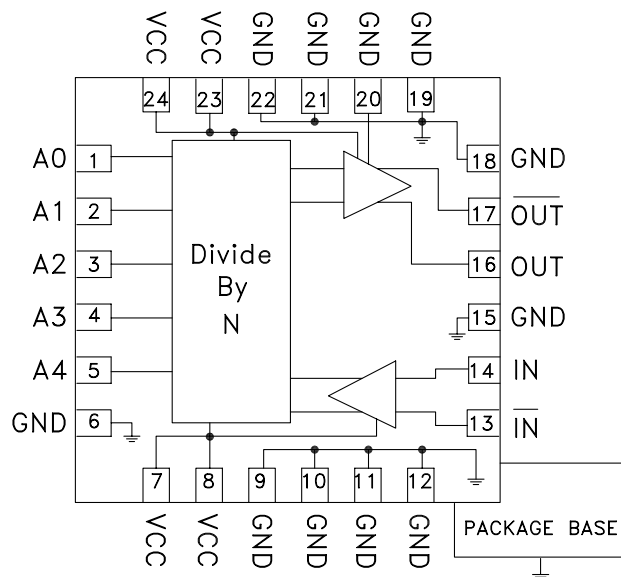
Programmable divider for offset synthesizer and variable divide by N applications:

- Satellite Communication Systems
- Point-to-Point and Point-to-Multi-Point Radios
- LMDS
- SONET

Features

- SSB Phase Noise: -153 dBc/Hz @ 100 kHz
- Selectable Division from 2 to 32
- Parallel 5-Bit Control
- Wide Input Power Range: -20 to +10 dBm
- 24 Lead 4x4mm QFN Package: 9 mm²

Functional Diagram



General Description

The HMC394LP4 & HMC394LP4E are low noise GaAs HBT programmable 5-bit counters in 4 x 4mm leadless surface mount packages. This device allows continuous division from N= 2 to 32 at input frequencies up to 2.2 GHz. The output voltage swing is 800 mV with a duty cycle inversely proportional to N. The low additive SSB phase noise of -153 dBc/Hz at 100 KHz offset makes this counter an excellent choice for low noise synthesizer applications.

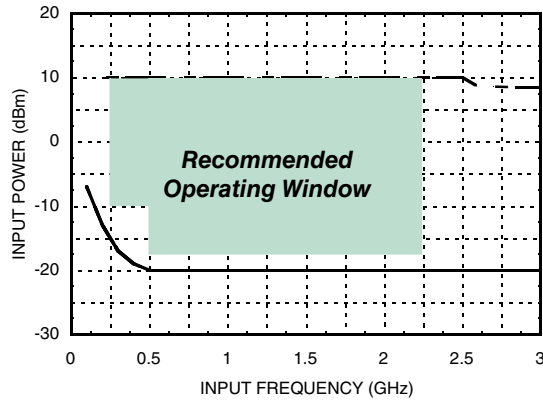
Electrical Specifications, $T_A = +25^\circ\text{C}$, 50 Ohm System, $V_{cc} = 5V$

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------|---------------------------|------|------|------|--------|
| Maximum Input Frequency | | 2.2 | | | GHz |
| Minimum Input Frequency | Sine Wave Input [1] | | | 0.1 | GHz |
| Input Power Range | $F_{in} = 0.1$ to 2.2 GHz | -15 | >-20 | +10 | dBm |
| Output Power | Divide-by-2 | | 4 | | dBm |
| SSB Phase Noise | $F_{in} = 1$ GHz, $N = 4$ | | -153 | | dBc/Hz |
| Output Transition Time | | | 100 | | ps |
| Supply Current (I_{cc}) | | | 194 | | mA |

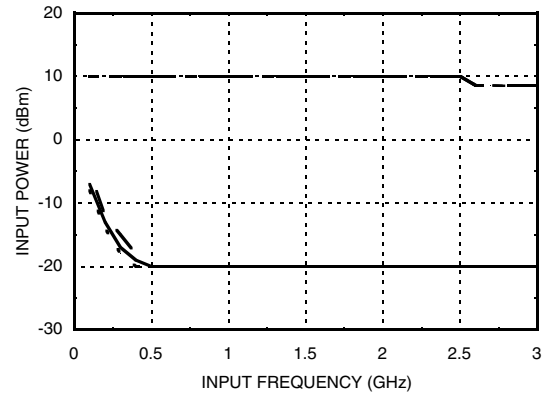
1. Divider will operate down to DC for square-wave input signal.



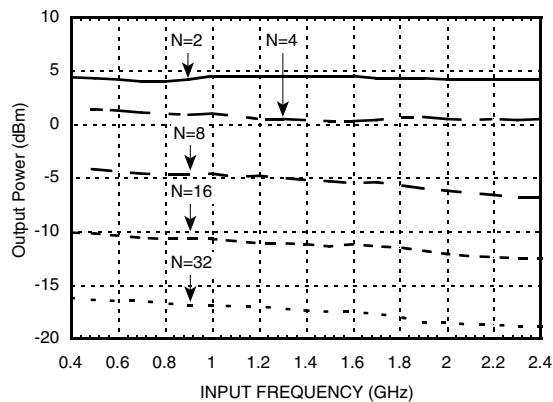
Input Sensitivity Window, 5 major Divide Ratio States, $T = 25\text{ }^\circ\text{C}$



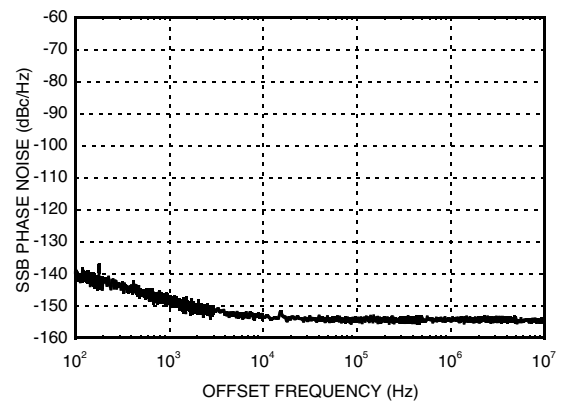
Input Sensitivity Window vs. Temperature, $N = 16$, $T = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$



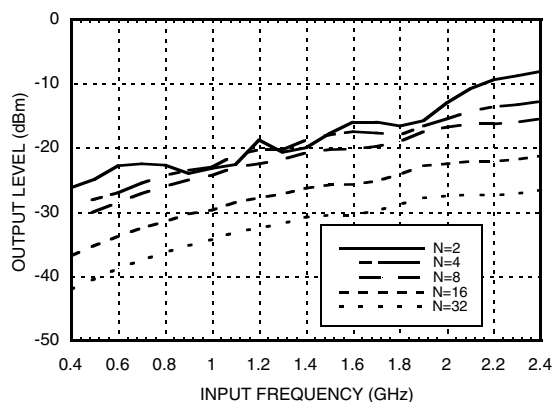
Output Power, 5 Major Divide Ratio States, $T = 25\text{ }^\circ\text{C}$



SSB Phase Noise Performance, $F_{in} = 1\text{ GHz}$, $N = 4$, $T = 25\text{ }^\circ\text{C}$



Fundamental Feedthru Power, $P_{in} = 0\text{ dBm}$, $T = 25\text{ }^\circ\text{C}$



Typical Supply Current vs. V_{cc}

| V_{cc} (V) | I_{cc} (mA) |
|--------------|---------------|
| 4.75 | 176 |
| 5.0 | 194 |
| 5.25 | 210 |

Note: Divider will operate over full voltage range shown above.

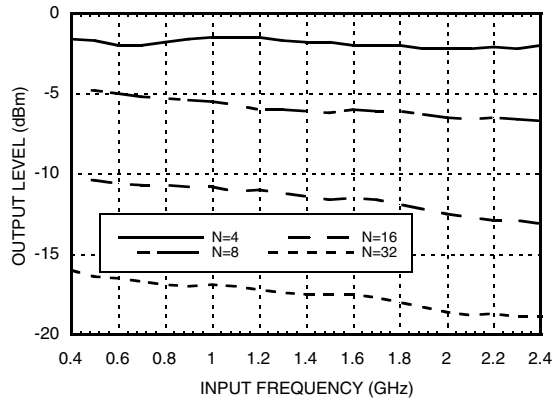
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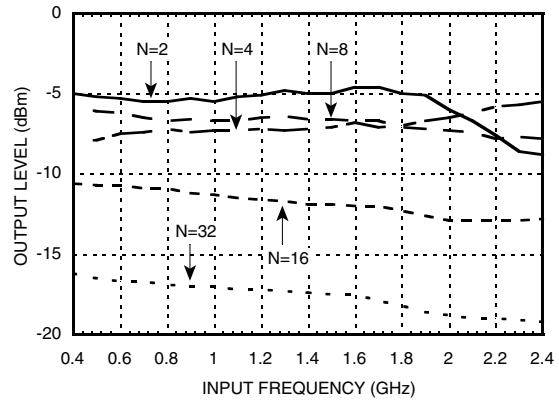
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5-BIT COUNTER, DC - 2.2 GHz**



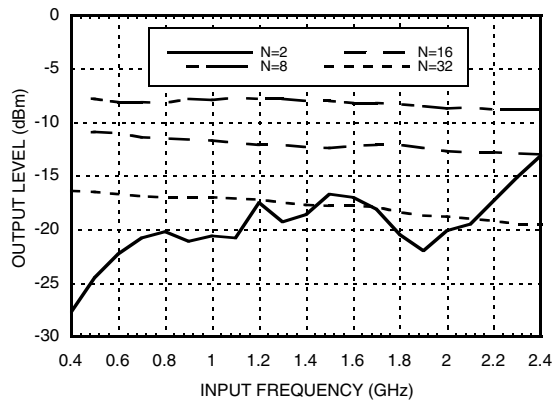
**2nd Harmonic,
Pin= 0 dBm, T= 25 °C**



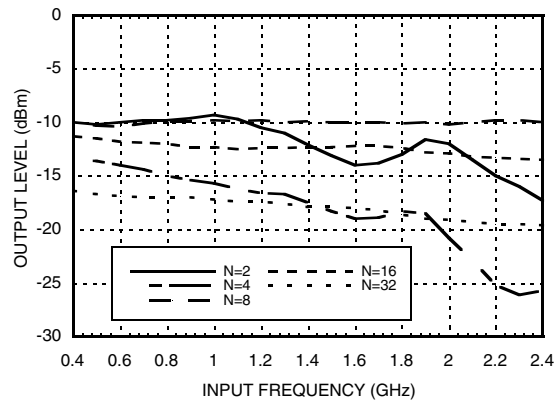
**3rd Harmonic,
Pin= 0 dBm, T= 25 °C**



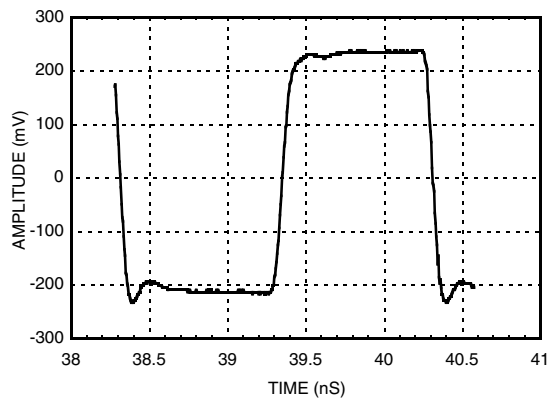
**4th Harmonic,
Pin= 0 dBm, T= 25 °C**



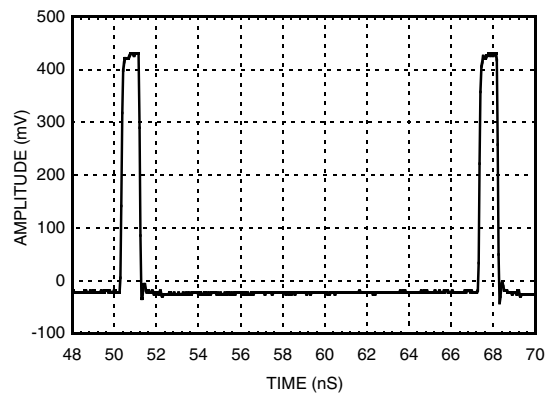
**5th Harmonic,
Pin= 0 dBm, T= 25 °C**



**Output Voltage Waveform, Fin= 1 GHz,
N= 2, Pin= 0 dBm, T= 25 °C**



**Output Voltage Waveform, Fin= 1 GHz,
N= 17, Pin= 0 dBm, T= 25 °C**



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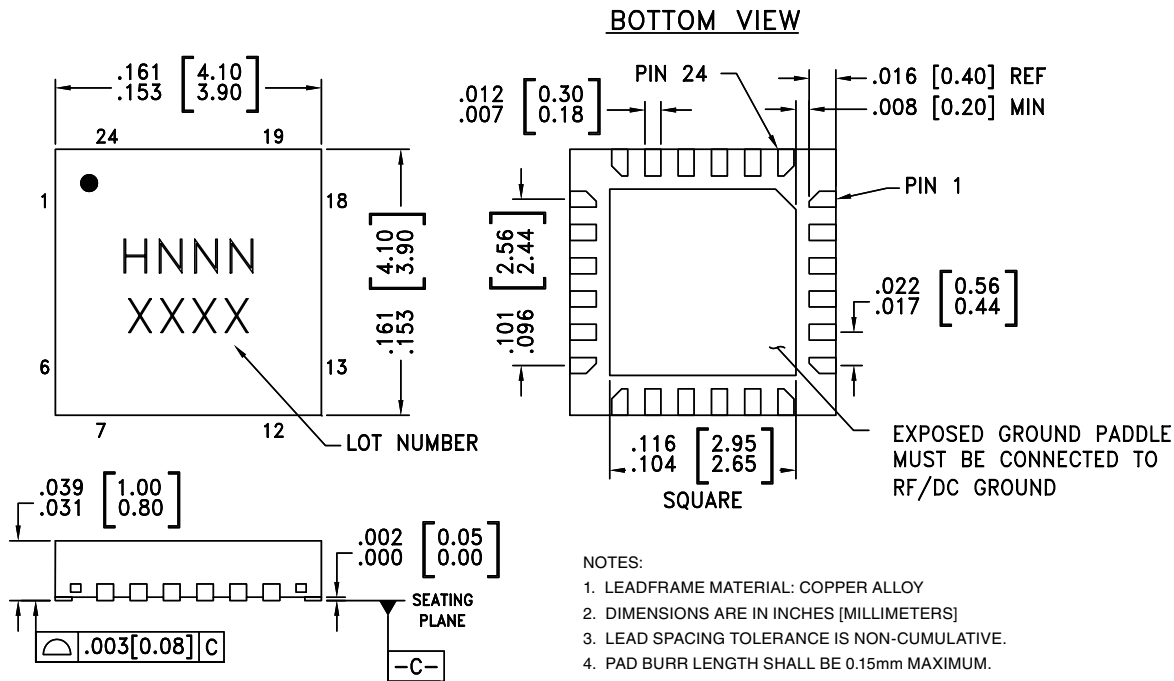


ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Absolute Maximum Ratings

| | |
|---|------------------|
| RF Input (Vcc = +5V) | +13 dBm |
| Vcc | +5.5V |
| VLogic | -1.6 to -1.2 Vcc |
| Maximum Channel Temperature | 135 °C |
| Continuous P _{diss} (T = 85 °C) (derate 55 mW/°C above 85 °C) | 1.155 W |
| Thermal Resistance (θ_{j-c}) Junction to Case (Ground Paddle) | 21.5 °C/W |
| Storage Temperature | -65 to +150°C |
| Operating Temperature | +55 to +85°C |

Outline Drawing



Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[3] |
|-------------|---|---------------|---------------------|--------------------------------|
| HMC394LP4 | Low Stress Injection Molding Plastic | Sn/Pb Solder | MSL1 ^[1] | H394 XXXX |
| HMC394LP4E | RoHS-compliant Low Stress Injection Molding Plastic | 100% matte Sn | MSL1 ^[2] | H394 XXXX |

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX



Pin Description

| Pin Number | Function | Description | Interface Schematic |
|--|-------------------------|--|---------------------|
| 1 - 5 | AO - A4 | CMOS compatible control input bit 0 (LSB) - 4. | |
| 6, 9, 10, 11, 12, 15, 18, 19, 20, 21, 22 | GND | Ground: Backside of package has exposed metal ground slug which must be connected to ground. | |
| 7, 8, 23, 24 | VCC | Supply voltage 5V ± 0.25V must be applied to all four pins. | |
| 13 | $\overline{\text{IN}}$ | RF input 180° out of phase with pin 14 must be AC ground. | |
| 14 | IN | RF input must be DC blocked. | |
| 16 | OUT | Divided output pulse. | |
| 17 | $\overline{\text{OUT}}$ | Divided output pulse 180° out of phase with pin 16. | |

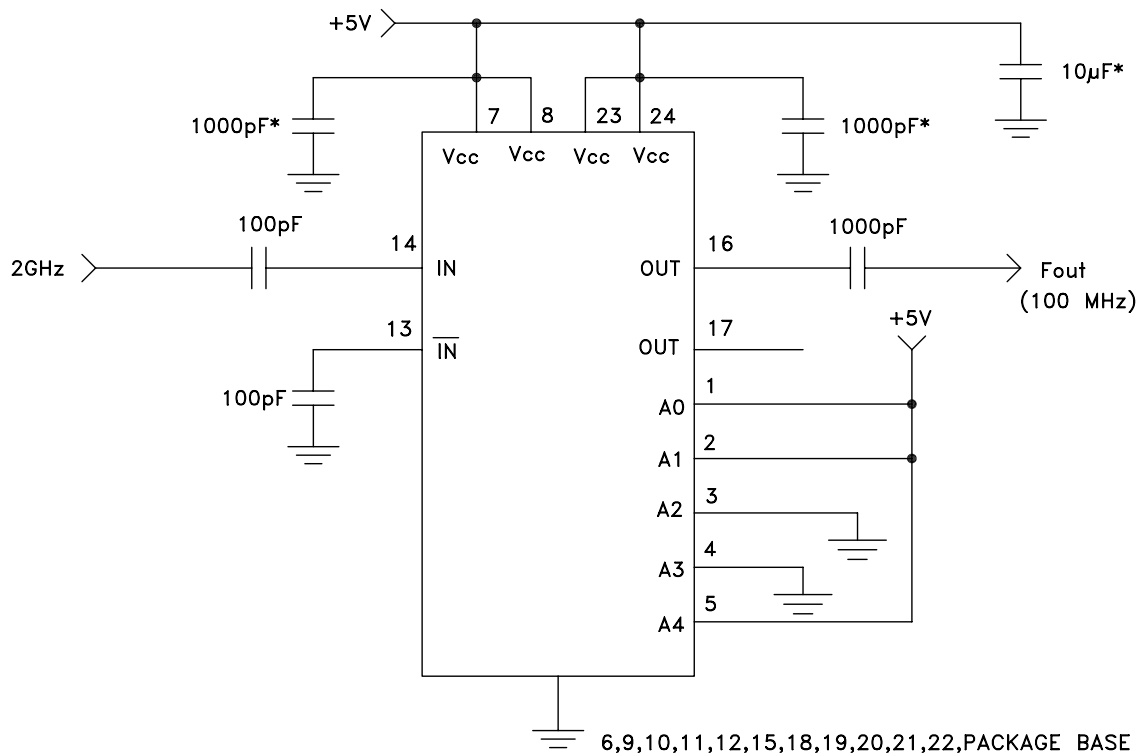


HMC394LP4 Programming Truth Table

| Function | (LSB) A0 | A1 | A2 | A3 | A4 |
|------------|-------------|----|----|----|----|
| Output Low | 0 | 0 | 0 | 0 | 0 |
| / 2 | 1 | 0 | 0 | 0 | 0 |
| / 3 | 0 | 1 | 0 | 0 | 0 |
| / 4 | 1 | 1 | 0 | 0 | 0 |
| - | - | - | - | - | - |
| / 32 | 1 | 1 | 1 | 1 | 1 |

Note: A0 through A4 are CMOS compatible logic control inputs.

Application Circuit, (2 GHz - Divide-by-20)



* Note: Mount bypass capacitors as close to pins as possible.

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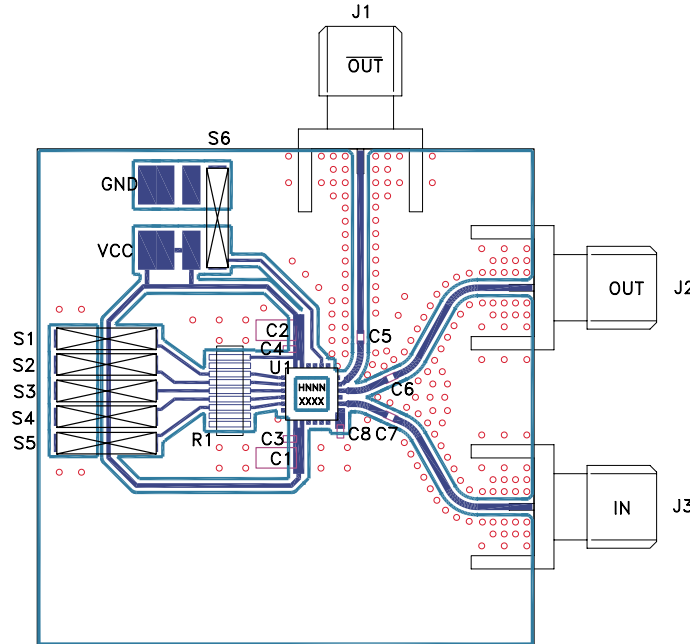
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Evaluation PCB

4

FREQUENCY DIVIDERS & DETECTORS - SMT



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and backside ground slug should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

**List of Materials for
Evaluation PCB 104898 [1]**

| Item | Description |
|-------------|---|
| J1 - J3 | PCB Mount SMA RF Connector |
| C1 - C2 [2] | 1.0 μ F Tantalum Capacitor |
| C3 - C4 [2] | .01 μ F Capacitor, 0603 Pkg. |
| C5 - C8 | 1000 pF Capacitor, 0603 Pkg. |
| R1* | Resistor SIP 10 K ohm |
| S1 - S6 | Jumper (shunt) 2mm |
| U1 | HMC394LP4 / HMC394LP4E 5-Bit Counter |
| PCB | 104435 Eval Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Optional components.

**HMC394LP4 Evaluation
PCB Truth Table**

| Function | S1 | S2 | S3 | S4 | S5 |
|------------|----|----|----|----|----|
| Output Low | 0 | 0 | 0 | 0 | 0 |
| / 2 | 1 | 0 | 0 | 0 | 0 |
| / 3 | 0 | 1 | 0 | 0 | 0 |
| / 4 | 1 | 1 | 0 | 0 | 0 |
| - | - | - | - | - | - |
| / 32 | 1 | 1 | 1 | 1 | 1 |

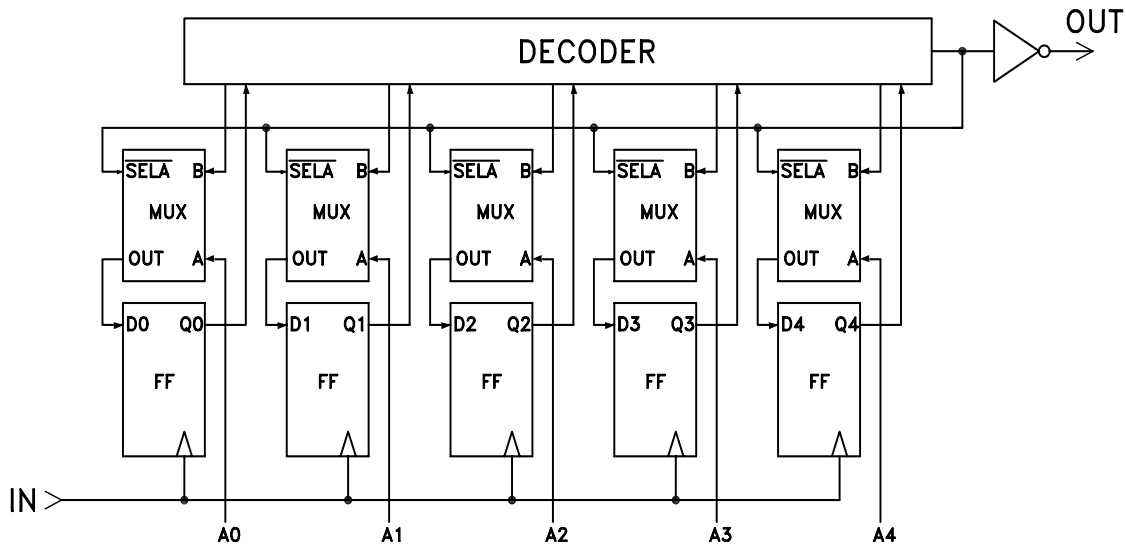
Note: 0 = Jumper Installed.
1 = Jumper Not Installed.

Note: The evaluation PCB for the HMC394LP4 contains 10K Ohm pull up resistors for each of the five control inputs A0 through A4. Programming the 31 distinct division ratios consists of installing or removing jumpers S1 through S5, as shown above. Jumper S6 must always be installed to provide ground to pin 20.



Applications Information

Simplified Block Diagram



Asynchronous Programming

The 5-Bit programmable counter counts-down from the programmed value of the data bits to zero and issues an output pulse at the end of each cycle. Settling time of the programmable 5-Bit counter is defined as the maximum time required for the counter to change the division ratio N to a new value after the data bits have settled. The worst case settling time occurs if the data bits A0 thru A4 are changing during the load cycle. Under this condition, the data bits may potentially be erroneous when they are clocked in and in the worst case could be all 1's, requiring 32 clock cycles until the correct data is re-loaded into the flip flops. The worst case asynchronous settling time can be calculated as follows:

$$T_{\text{SETTLING MAX}} = 32/f_{\text{IN}} \text{ (For Asynchronous Programming)}$$

As an example, if the input frequency is 1 GHz, the maximum settling time is 32 nS



Synchronous Programming

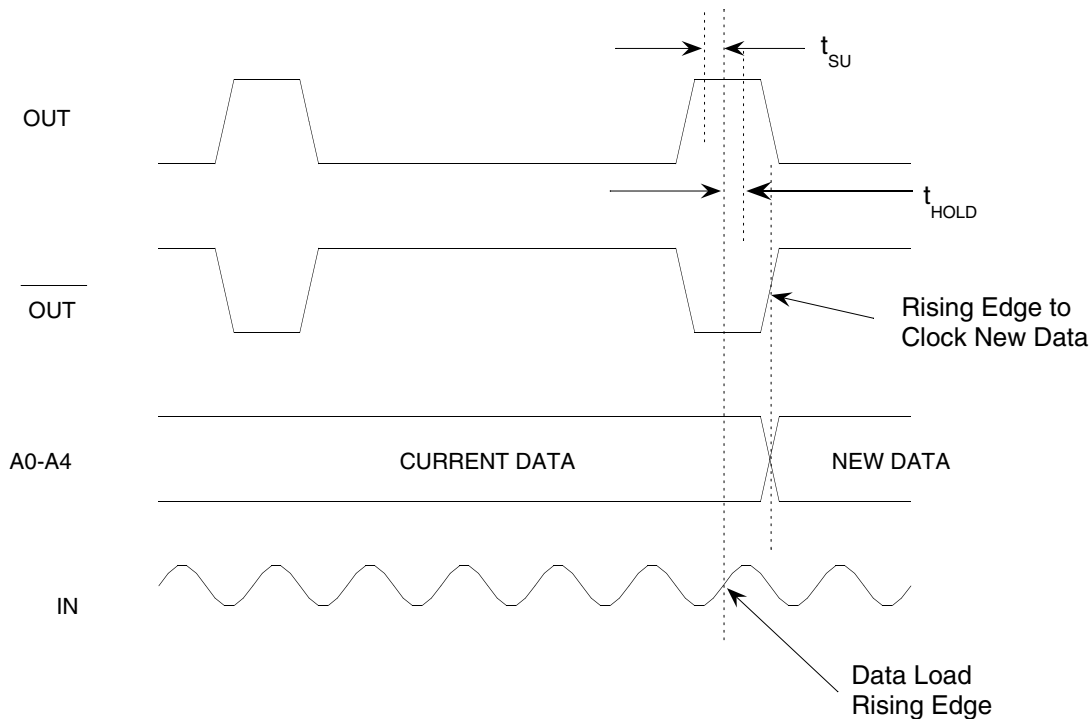
For applications which can not tolerate a momentary undefined division ratio, which normally occurs while changing the data bits (A0-A4) at random, synchronous programming can be used. Data is loaded into the counter on every rising edge of the clock which occurs while the output (OUT) is "HIGH". The typical minimum setup and hold times are shown in the table below as a function of frequency. For precision applications, the rising edge of the complementary output may be used to latch the new data bits (A0-A4), so that all bits are settled before the next load cycle.

$$T_{\text{SETTLING MAX}} = N/f_{\text{IN}} \text{ (For Synchronous Programming)}$$

Where N is the desired division ratio, and f_{IN} = Input Frequency (Hz)

| Parameter | 0.5 GHz | 1 GHz | 2 GHz |
|--------------------|---------|--------|--------|
| t_{SETUP} | 200 ps | 200 ps | 200 ps |
| t_{HOLD} | 700 ps | 300 ps | 120 ps |

**Programmable Divider Timing Requirements
for Synchronous Programming**



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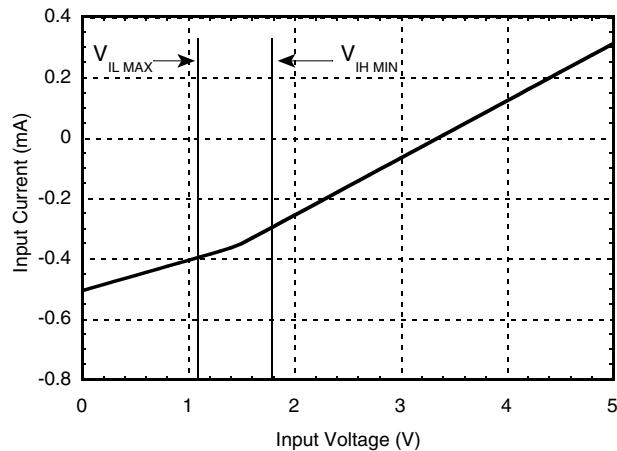


CMOS/TTL Input Characteristics

Maximum Input Logic "0" Voltage ($V_{IL\ MAXIMUM}$) = 1.1V @ 10 uA.

Minimum Input Logic "1" Voltage ($V_{IH\ MINIMUM}$) = 1.8V @ 500 uA.

Input IV characteristics for the logic inputs (A0-A4) are shown below:



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