

LT3095

Dual-Channel Low Noise Bias Generators

DESCRIPTION

Demonstration circuit 2270A is a dual-channel low noise bias generator featuring [LT3095](#). The LT3095 generates two low noise bias supplies from a common input voltage range from 3V to 20V. Each channel includes a fixed frequency, peak current mode step-up switching regulator and a low noise, single resistor programmable linear regulator. The maximum load current is 50mA for each channel.

Each boost regulator adjusts its output voltage to 2V above the corresponding linear regulator's output voltage, optimizing power dissipation, PSRR and transient response. The integrated boost regulator, frequency compensation and Schottky diodes minimize the external component count and simplify system design.

The switching frequency can be programmed either via oscillator resistor or an external clock from 450kHz to

2MHz. The SYNC pin on the demo board is grounded by default. To synchronize to an external clock, move JP1 to SYNC and apply the external clock to the SYNC turret. The R_T resistor (R2) should be chosen to set the LT3095 internal switching frequency to the SYNC frequency.

The LT3095 is available in a thermally enhanced 24-Lead 3mm × 5mm QFN package.

The LT3095 data sheet gives a complete description of the device, operation and application information. The data sheet must be read in conjunction with this quick start guide for demo circuit 2270.

Design files for this circuit board are available at <http://www.linear.com/demo/DC2270A>

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PERFORMANCE SUMMARY Specifications are at $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		3		20	V
V_{OUT1}	Channel1 Output Voltage		4.9	5	5.1	V
V_{OUT2}	Channel2 Output Voltage		14.7	15	15.3	V
I_{OUT1}	Channel1 Max Output Current		50			mA
I_{OUT2}	Channel2 Max Output Current		50			mA
f_{SW}	Switching Frequency	$R_T = 100\text{k}\Omega$	0.95	1	1.05	MHz
$V_{OUT,P-P}$	Output Voltage Peak-to-Peak Noise	$V_{IN} = 5\text{V}$, $V_{OUT} = 15\text{V}$, $I_{OUT} = 50\text{mA}$, $f_{SW} = 1\text{MHz}$ 20MHz BW		65		μV

QUICK START PROCEDURE

Demonstration circuit 2270 is easy to set up to evaluate the performance of the LT3095. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below:

1. Place JP1 on RT position.
2. With power off, connect the input power supply to V_{IN} and GND. Make sure that the input voltage does not exceed 20V.
3. With power off, connect loads from V_{OUT1} to GND, and V_{OUT2} to GND.
4. Turn on the power at the input.
5. Check for the proper output voltages (5V and 15V).

NOTE: If there is no output, temporarily disconnect the load to make sure that the load is not set too high or is shorted.

6. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation and other parameters.
7. An external clock can be added to the SYNC terminal when SYNC function is used (JP1 on the SYNC position). The set switching frequency should be programmed to the SYNC frequency. See the data sheet section Programming the Switching Frequency for details.
8. The output noise can be measured by J1 and J2. Please refer to Application Notes 70 for details.

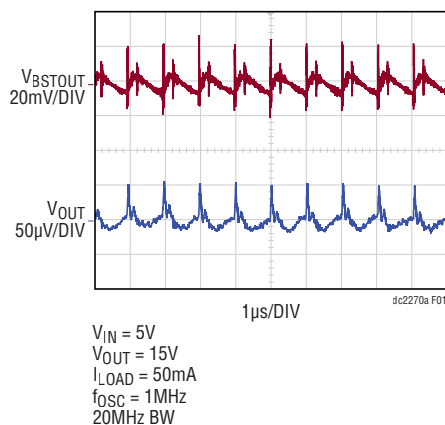
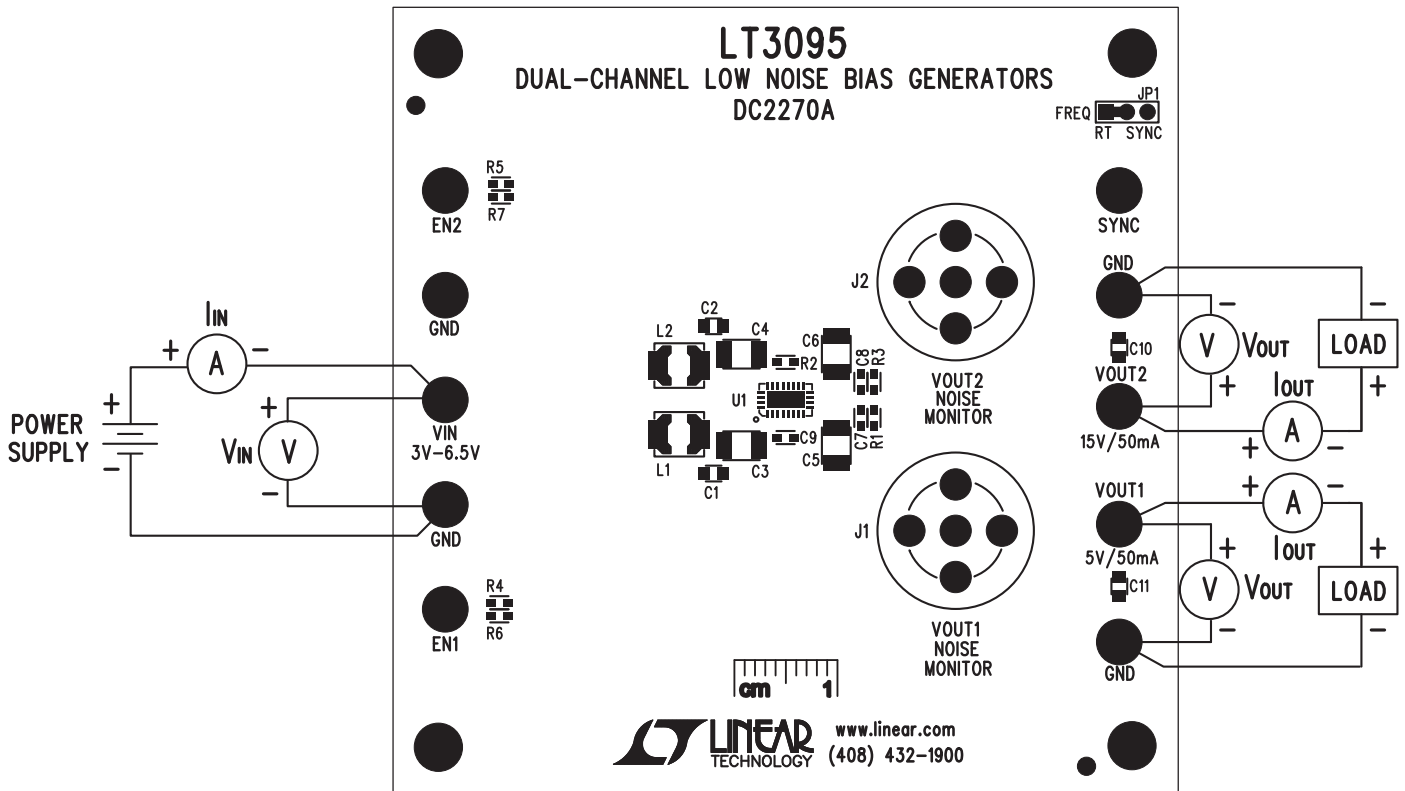


Figure 1. Transient Output Ripple

QUICK START PROCEDURE



*J1 AND J2 ARE THE BNC CONNECTORS TO COAXIAL CABLE FOR NOISE MEASUREMENT. PLEASE REFER TO AN70 APPENDIX B FOR DETAILS

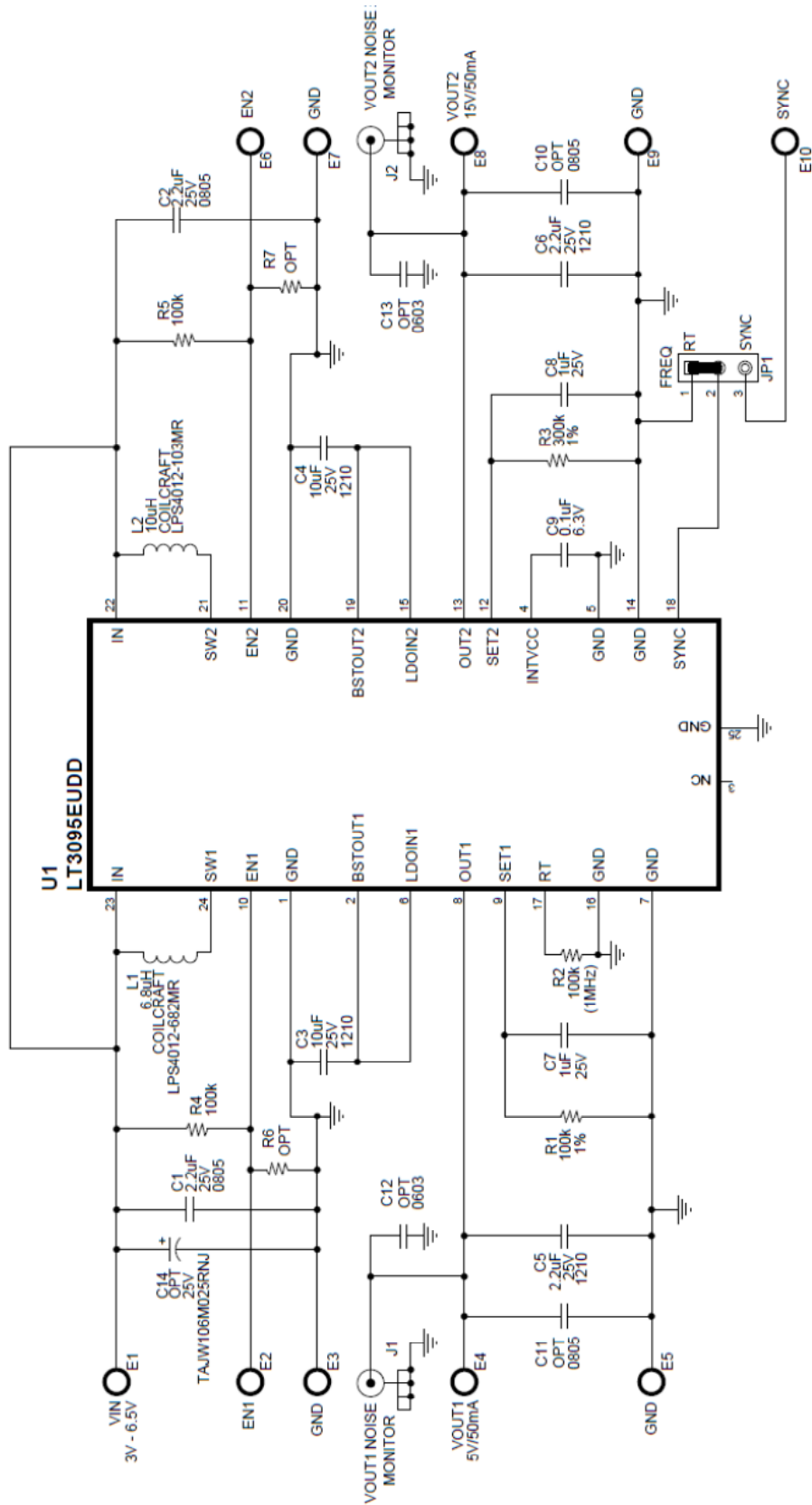
Figure 2. Proper Measurement Equipment Setup

DEMO MANUAL DC2270A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C1, C2	CAP., 2.2 μ F, X7R, 25V, 10%, 0805	MURATA, GRM21BR71E225KA73L
2	2	C3, C4	CAP., 10 μ F, X7R, 25V, 10%, 1210	MURATA, GRM32DR71E106KA12L
3	2	C5, C6	CAP., 2.2 μ F, X7R, 25V, 10%, 1210	AVX, 12103C225KAT2A
4	2	C7, C8	CAP., 1 μ F, X7R, 25V, 10%, 0603	MURATA, GRM188R71E105KA12D
5	1	C9	CAP., 0.1 μ F, X7R, 6.3V, 10%, 0603	AVX, 06036D104KAT2A
6	1	L1	INDUCTOR, 6.8 μ H	COILCRAFT LPS4012-682MR
7	1	L2	INDUCTOR, 10 μ H	COILCRAFT LPS4012-103MR
8	4	R1, R2, R4, R5	RES., CHIP, 100k, 1/10W, 1%, 0603	VISHAY, CRCW0603100KFKEA
9	1	R3	RES., CHIP, 300k, 1/10W, 1%, 0603	VISHAY, CRCW0603300KFKEA
10	1	U1	I.C., REGULATOR, QFN24-3X5-UDD	LINEAR TECH., LT3095EUDD#PBF
Additional Demo Board Circuit Components				
1	0	C10, C11 (OPT)	CAP., 0805	
2	0	C12, C13 (OPT)	CAP., 0603	
3	0	R6, R7 (OPT)	RES., 0603	
4	0	C14 (OPT)	CAP, TANT., 10 μ F, 25V, 20%, 2312	AVX, TAJW106M025RNJ
Hardware: For Demo Board Only				
1	10	E1-E10	TESTPOINT, TURRET, 0.094" pbf	MILL-MAX, 2501-2-00-80-00-00-07-0
2	1	JP1	HEADER 3 PIN 0.079 SINGLE ROW	WURTH, 620 003 111 21
3	1	XJP1	SHUNT, 0.079" CENTER	WURTH, 608 002 134 21
4	2	J1-J2	CONN, BNC, 5 PINS	CONNEX, 112404

SCHEMATIC DIAGRAM



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Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

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