8V97003 EVB User Manual

Evaluation Board

The 8V97003 evaluation board is designed for customers to evaluate the functionality and performance of the 8V97003 RF/Microwave Wideband Synthesizer. On the evaluation board, the 8V97003 device can be programmed and configured with Timing Commander, a PC-based GUI that generates output frequency from 187.5MHz to 18GHz with a very low phase noise and RMS phase jitter. This user manual details the setup of the EVB and the programming of the 8V97003 using Timing Commander.

Contents

Figures

Tables

1. Overview

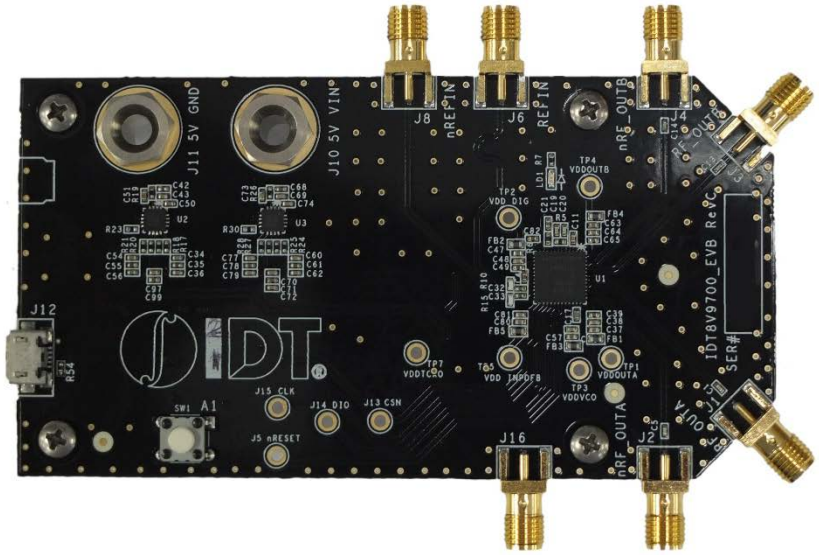


Figure 1. 8V97003 EVB – Top View

Kit Contents

- 8V97003 Evaluation Board
- Micro USB cable

Required Software

- IDT Timing Commander Software Installer (available at www.idt.com/timingcommander)
- Network access during installation if the .NET framework is not currently installed on the system
- 8V97003 GUI (available at www.idt.com/8V97003)
- USB 2.0 or USB 3.0 interface

2. Functional Description

This section provides an overview of the different components on the evaluation board, and discusses the necessary bench equipment, the hardware connection, and the power-up sequence.

2.1 Evaluation Board Overview

The following diagram identifies various components of the board: power supply jacks, input and output SMA connectors, USB interface port, and lock indicator LED.

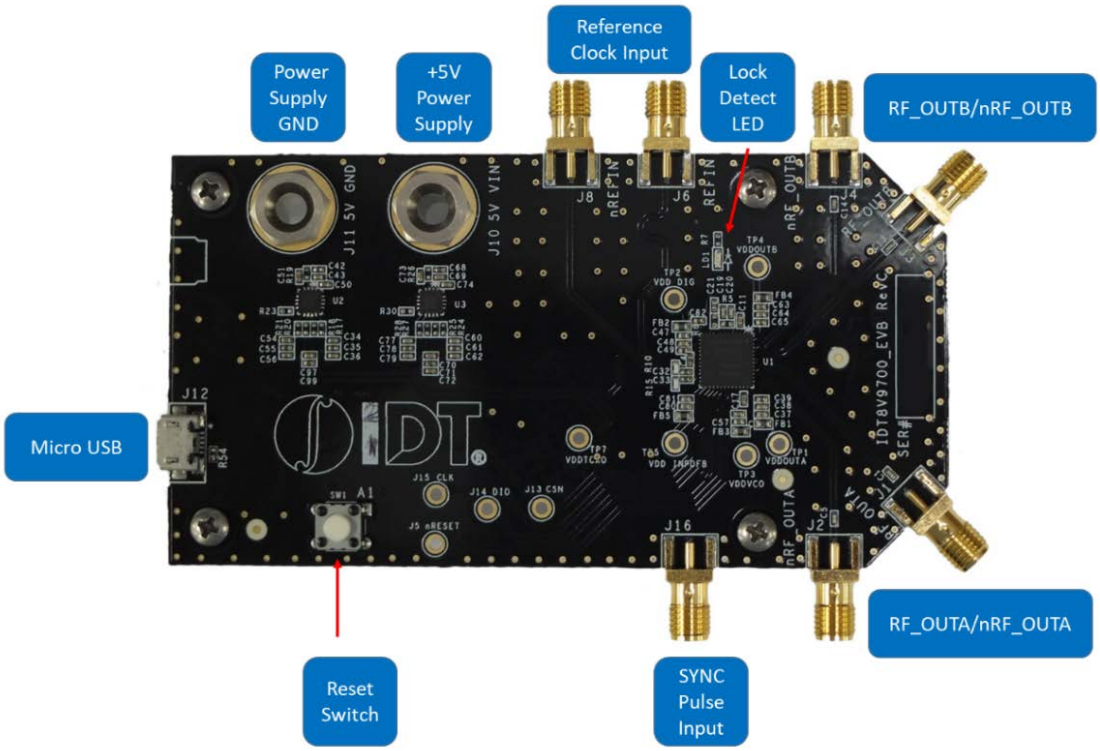


Figure 2. Evaluation Board Overview

Detailed descriptions of these components are as followed (clock-wise from upper left):

- Power Supply (Banana) Jacks: +5V DC at J10, GND at J11
- PCB Layout Revision: for RF Transmission Line Loss information
- Reference Clock Input SMA connectors: use J6 and J8 for differential reference clock input; use J6 for single-ended reference clock input
  - Maximum Vpp = 3.3V
  - f_max = 1000MHz when input reference doubler is disabled
  - f_max = 250MHz when input reference doubler is enabled
- Lock Detect LED: LED indicator of PLL Lock status
- RF_OUTB/nRF_OUTB output SMA connectors: differential RF/Microwave outputs at J3, J4
- RF_OUTA/nRF_OUTA output SMA connectors: differential RF/Microwave outputs at J1, J2
- SYNC input: J16
- Reset Push Button: SW1
- Micro USB: J12

2.2 Required Equipment

Several bench equipment are required for the evaluation of the 8V97003. This section describes the functions of each required equipment.

2.2.1. Power Supply

The evaluation board uses a single +5V DC supply for its power supply. When running the board, set the bench power supply at 5V/1A. The +5V terminal is connected to J10, and the Ground terminal is connected to J11. Multiple LDOs on board are used to generate 3.3V to 8V97003 device.

2.2.2. Signal Generator

A signal generator is necessary to generate the reference clock to the 8V97003 RF/Microwave Synthesizer. Single-ended reference clock is connected to J6, while J8 can be left unconnected. When differential reference clock is available, connect them to J6 and J8.

Oscillators such as Oven Controlled Oscillators (OCXO) from Wenzel Associates, Inc. can also be used to generate reference clock to the 8V97003 RF/Microwave Synthesizer. Some examples of these Wenzel Oscillators are the VHF ULN OCXO (for frequencies from 15MHz to 160MHz) or MXO-FR OCXO (for frequencies greater than 200MHz). However, a signal generator is recommended for the flexibility to experiment with different reference clock frequencies.

2.2.3. Phase Noise Analyzer/Spectrum Analyzer

A phase noise analyzer is necessary to evaluate phase noise performance of the 8V97003 RF/Microwave Synthesizer. A spectrum analyzer is necessary to evaluate harmonic performance. Both of these equipment have (output) power measurement capability.

2.2.4. Balun

Balun is optional. A balun is used to convert single-ended output of a signal generator to differential output, which is used to provide reference clock to the 8V97003 RF/Microwave Synthesizer. Another balun can be used to combine the differential outputs of the 8V97003 to a single-ended signal for measurement with a phase noise analyzer/spectrum analyzer.

2.2.5. PC

A PC is required to run IDT Timing Commander GUI.

2.3 Hardware Connection

Follow these procedures to set up the evaluation board:

1. Without connecting the bench power supply to the EVB, turn on the bench power supply to make sure the output voltage and current clamp are set to +5V/1A respectively. Then turn off the bench power supply.
2. Connect bench power supply to EVB: +5V to J10, GND to J11.
3. Connect Signal Generator's output to J6 if single-ended reference input clock configuration is desired. If differential reference input clock configuration is desired, connect Signal Generator's output to a balun's unbalanced port – then connect balun's balanced ports to J6 and J8.
4. Connect RF outputs to measurement equipment.
5. Terminate unused outputs.
6. Connect micro-USB cable: micro-B end of the cable is connected to J12, A-plug is connected to PC.

Table 1. Evaluation Board Connection Descriptions

Equipment Type	Connection on EVB	Description
(DC) Power Supply	+5V at J10 / GND at J11	5V/1A power supply
Signal Generator	J6 (for single-ended)/balun (for differential)	Reference clock input to 8V97003
Phase Noise Analyzer	J1, J2, J3, J4	Measure phase noise at RF outputs
Spectrum Analyzer	J1, J2, J3, J4	Measure output power or harmonic performance at RF outputs
Balun (Macom H-183-4)	J6, J8	Differential reference clock input to 8V97003
Balun (Marki BAL 0026)	J1, J2, J3, J4	Convert differential outputs to single-ended signal for measurements
Micro-USB	J12	

2.4 Power-up Procedures

Follow the steps below to power up the evaluation board once the hardware connections shown in 1.3 have been completed:

1. Turn bench power supply on. Initial current consumption of the whole EVB should be around 500mA
2. Set reference clock input frequency and amplitude on Signal Generator – enable Signal Generator output
3. Program 8V97003 RF/Microwave Synthesizer using IDT's Timing Commander GUI

3. Working with Timing Commander™ for Programming/Configuration

3.1 Opening an Existing Configuration

When a customer's user case information is provided to IDT prior to EVB is sampled, an optimized configuration is usually provided to the customer for the evaluation. Follow the procedure below to open a setting file:

1. Power up the evaluation board
2. Start the Timing Commander software. You will see options of **New Setting File** and **Open Setting File**. Select **Open Setting File**.

Figure 3. Starting up Timing Commander GUI

3. At **Open Settings File** dialog box, browse to select the setting file (*.tcs) and the personality file (*.tcp) – Click **Open**.

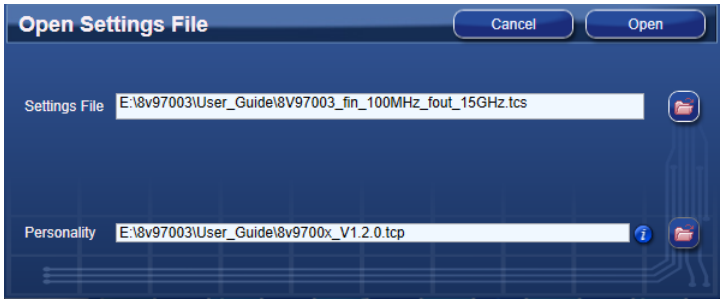


Figure 4. Open Settings File Dialog Box

4. The GUI window with the 8V97003 block diagram opens to show the existing configuration; all configured values display. To connect the board with Timing Commander (PC), click the Connect button (chip symbol) at the upper right corner of the GUI to set up the communication interface.

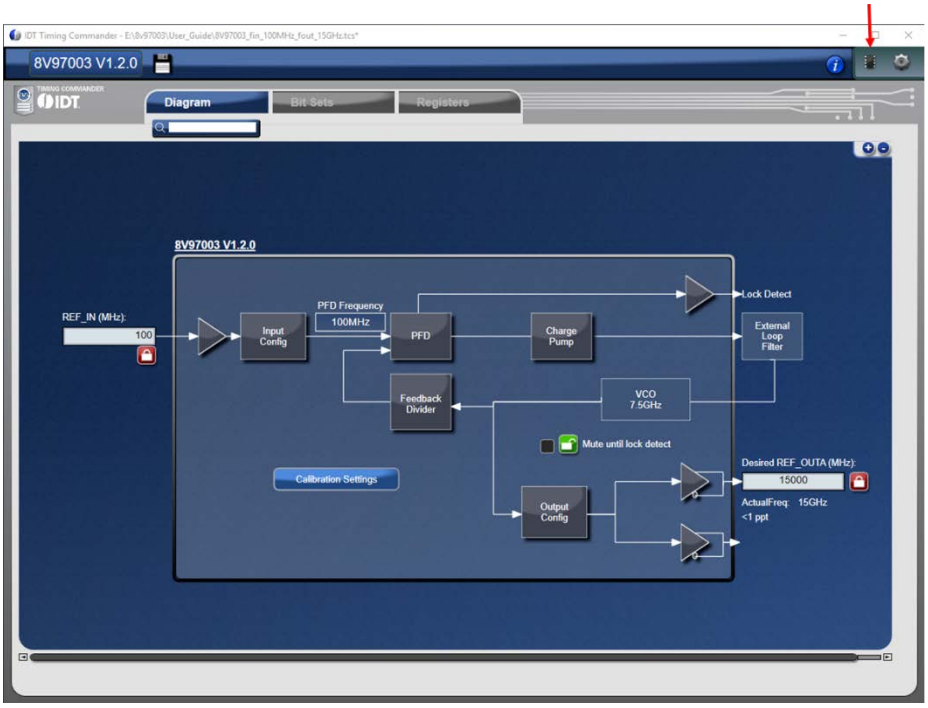


Figure 5. Connect to 8V97003 Device

5. The connection will be established if a valid 8V97003 is detected, and a green band appears at the upper right corner of the GUI window.
6. Click **Write All** to program 8V97003 device.

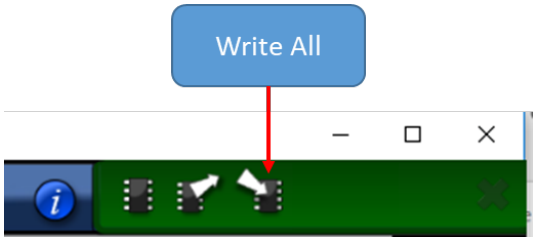


Figure 6. Program 8V97003 Device

7. The 8V97003 is now configured. If the lock detection function is properly configured, Lock Detect LED should light when the PLL locked status is achieved, and the output frequency displayed in the Desired REF_OUTA/B box should be available for measurements.

3.2 Making Changes to an Existing Configuration

When changes to an existing configuration is necessary, make sure none of the settings in the affected signal path is locked as to allow the GUI to make appropriate calculation for optimal settings. A locked setting is indicated by a white lock symbol in a red box ( ). Follow steps a. through c. from Opening an Existing Configuration before making changes to the existing configuration.

For example, when changing the input reference frequency, make sure the input doubler enable and the input reference divider settings are unlocked, as shown in Figure 7.

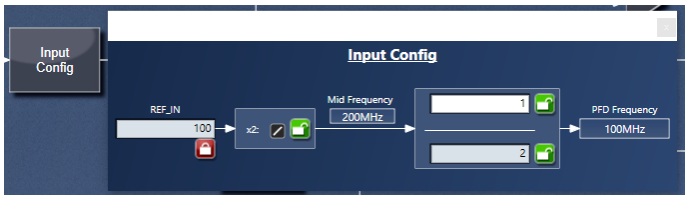


Figure 7. Input Configuration Settings

Another example is when changing the desired output frequency, make sure the Feedback Divider settings are unlocked, as shown in Figure 8.

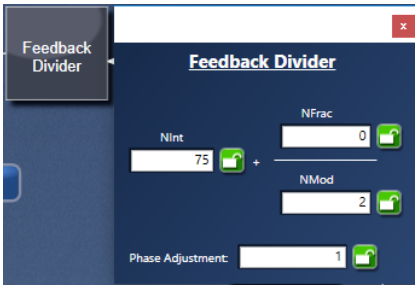


Figure 8. Feedback Divider Settings

A quick way to view all “Locked” settings in an existing configuration is to select “Locked” option in “Bit Sets” tab, as shown in Figure 9.

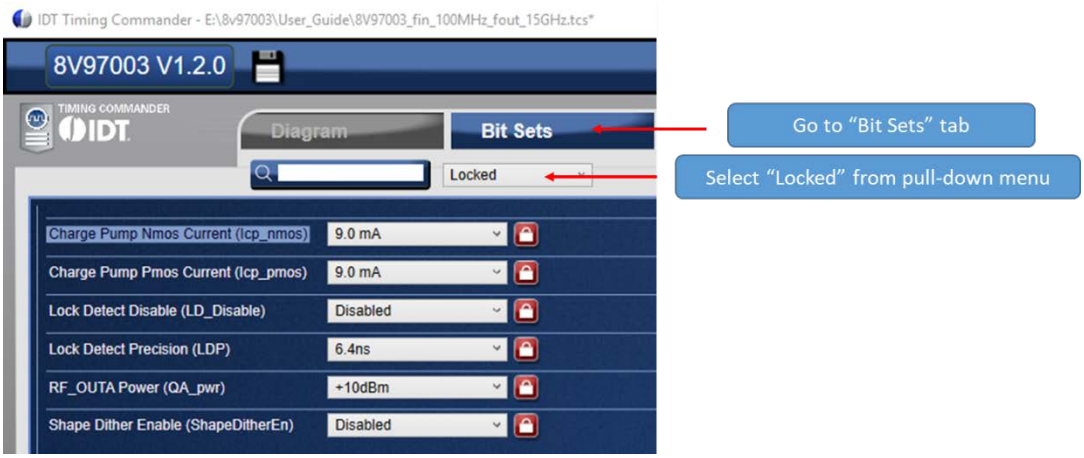


Figure 9. Locked Settings View in Bit Sets Tab

3.3 Creating a New Configuration

Follow the procedure below to create a new setting file:

1. Power up the evaluation board.
2. Start the Timing Commander software. You will see options of “New Setting File” and “Open Setting File”. Select “New Setting File”.
3. In the “New Settings File” dialog box, select “8V97003” and click OK
4. The GUI window with the 8V97003 block diagram will open with no setting on any of the blocks

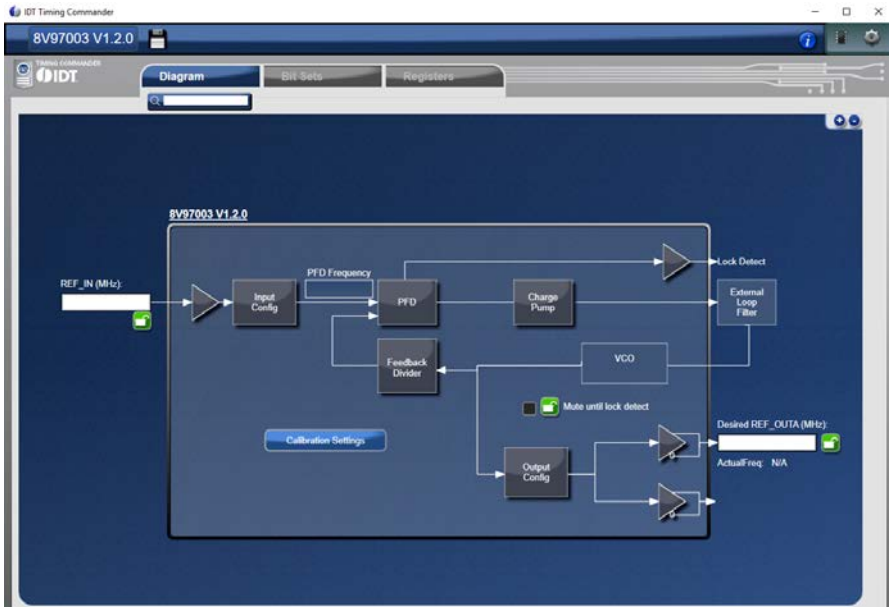


Figure 10. New Settings GUI

5. Click on each functional blocks of the block diagram to enter the desired settings/configuration or to check automatically calculated settings/configuration. An invalid setting/configuration will result in an **Error**. Settings/configurations that are not invalid, but not optimum will result in **Warning**. Error must be resolved before proceeding.
6. Once all settings have valid values, click the Connect button (chip symbol) at the upper right corner of the GUI to set up the communication interface.
7. The connection will be established if a valid 8V97003 is detected, and a green band appears at the upper right corner of the GUI window.
8. Click **Write All** to program 8V97003 device.

See Appendix A for examples of creating New Configurations for 8V97003 device.

4. Performance Evaluation with the 8V97003 EVB

As the 8V97003 RF/Microwave Synthesizer covers a very wide range of output frequencies, careful considerations must be given to component selection and termination to ensure signal integrity, especially at high output frequencies. In addition, because impedance is a function of frequency, (amplitude) loss of transmission line should also be characterized over frequency to ensure accurate de-embed of trace loss. This section discusses the following topics when evaluating performance of 8V97003 device:

- Output Matching
- AC-coupling (series) capacitor
- Proper termination when making measurements on single-ended output
- Transmission line loss

4.1 Output Matching

The 8V97003 devices provides two differential outputs of CML type. The outputs are “open collector outputs” and can be matched in different ways. By default, a simple resistive matching is used on the 8V97003 EVB. This resistive matching consists of a 50Ω resistor to VDD, with a series AC coupling capacitor. This matching scheme gives the output amplitude a “broadband” response, but it is not ideal to achieve maximum output power transmission, especially for high frequencies.

An inductive matching is recommended for better performance and optimal power transmission. For the inductive matching scheme, the 50Ω resistors connected to VDD are replaced by inductors. The inductor value is frequency dependent.

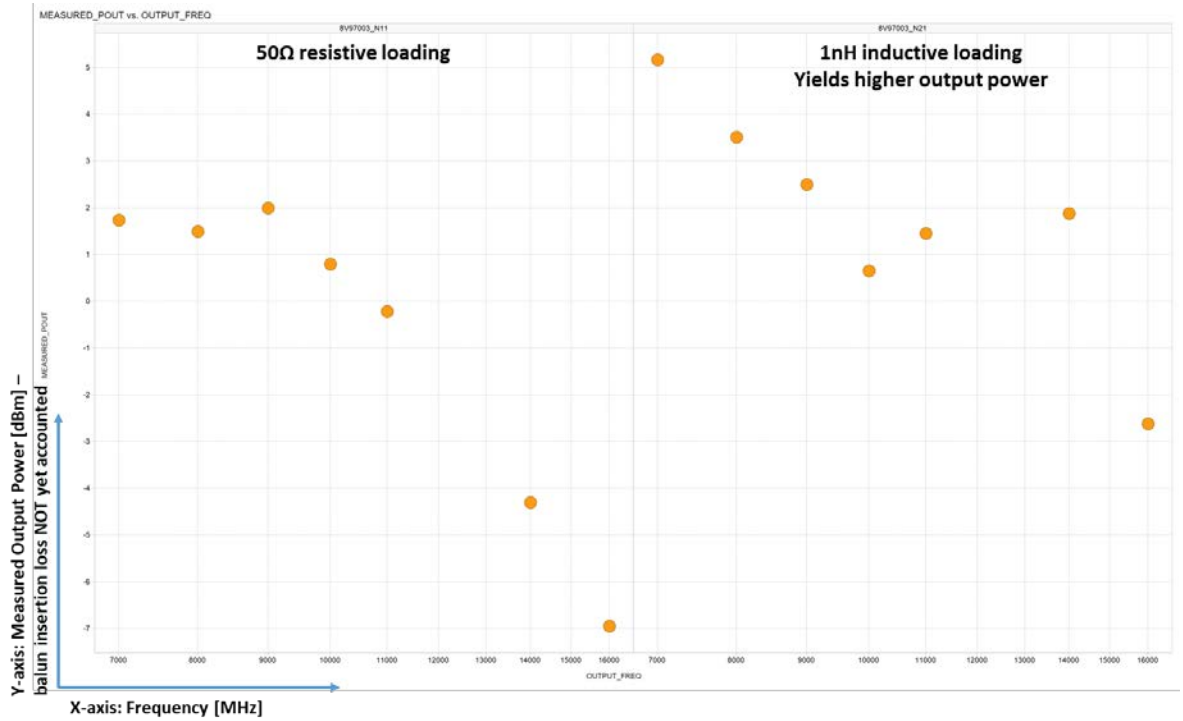


Figure 11. 8V97003 Output Power Over Frequencies – Resistive vs. Inductive Matching

For impedance matching of 50Ω, the inductor value can be calculated as L = 50 ÷ (2 x π x f) where f is the operating frequency. In the data shown in Figure 11 above, a 1nH would provide a 50.24Ω match at f = 8GHz. Therefore, for the same output power setting, the measured output power with the 1nH inductive matching is 2dB higher than that with 50Ω resistive match at 8GHz.

When selecting the inductors for output matching, it is critical to select inductors whose self-resonant frequency is higher than the operating frequency.

4.2 AC-coupling Capacitor

AC-coupling capacitors are populated on 8V97003 EVB to ensure 0V DC on the output signals when they are connected to the input of (RF) measurement equipment. The part number of the (series) AC-coupling capacitor used on 8V97003 EVB is 520L103KT16T which is specified for operation up to 16GHz. The same consideration regarding self-resonant frequency also applies when selecting this capacitor.

For output frequencies above 16GHz, IDT recommends these AC-coupling capacitors be replaced with 0Ω resistors, and a high performance external DC-block be used to ensure 0V DC input to (RF) measurement equipment.

4.3 Termination

As mentioned in the Output Matching section, the outputs of the 8V97003 are “open collector outputs”. Therefore, when making single-ended measurements on one branch of the differential pair, it is critical to properly terminate the unused port to minimize distortion (due to reflection) of the output signal.

Because the built-in load of most (RF) measurement equipment is 50Ω, when making single-ended measurements on one branch of the differential pair, terminate the unused port with a 50Ω load. At high frequencies, the mismatch in electrical length at which each branch of the differential pair is terminated could result in reflection that would distort the output signal. IDT recommended that at high frequencies, each branch of the differential pair is terminated at the same electrical length. This means when making single-ended measurements on one branch of the differential pair at high frequency, connect the unused port to a cable of the same length with the cable connecting the port being measured, and terminate that cable with 50Ω load.

4.4 Transmission Line Loss

To accurately characterize the output power of the 8V97003 RF/Microwave Synthesizer, insertion loss of all components in the measurement path should be accurately accounted. Besides the insertion loss of the RF cables, and balun (if applicable), loss across frequencies due to transmission line on the EVB must also be characterized.

To assist customer with the measurement of trace loss on 8V97003 EVB, a test “coupon” is included in the same PCB manufacturing panel with the main EVB. This test “coupon” consists of the exact copy of the transmission lines on the board and the SMA connectors.

The insertion loss of the transmission lines on PCB version D is shown below. The measurement was taken on the test “coupon”, using a network analyzer, with $Z_{SOURCE} = Z_{LOAD} = 50\Omega$. On the actual EVB with 8V97003 as device-under-test (DUT), the source impedance (including output buffer, bond wire, package, and external matching components) is probably not a perfect 50Ω. Therefore, the mismatch between the source impedance and the transmission line could cause reflection that would likely present more loss to the output signal. The insertion loss measured on the test structure shown above should be used as the minimum loss or the output signal will suffer.

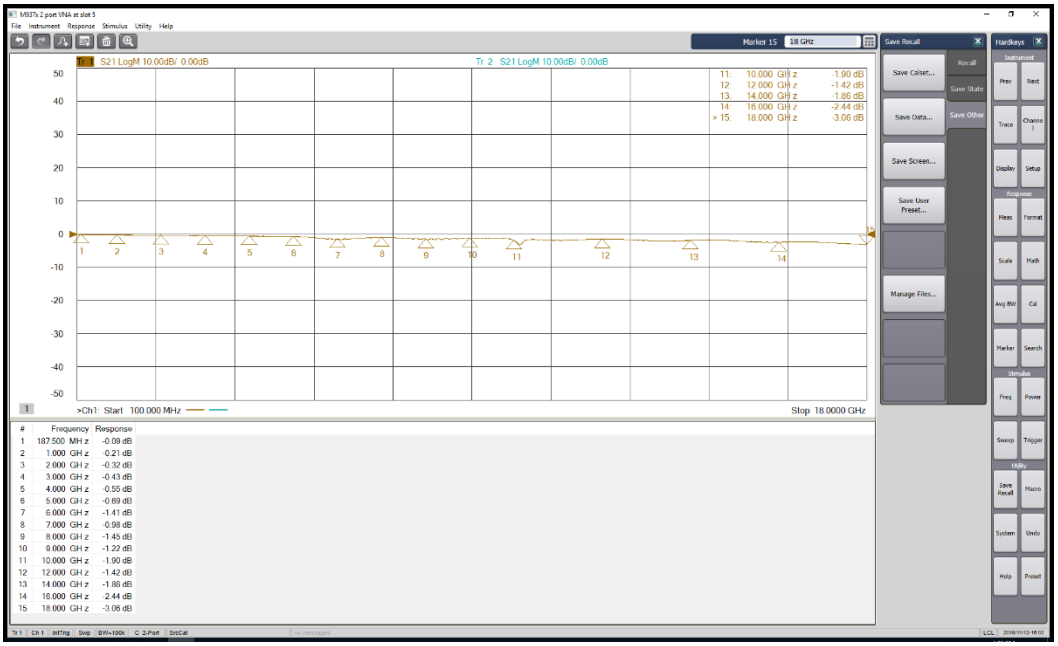


Figure 12. 8V97003 EVB Revision D Transmission Line Loss

The insertion loss of the transmission lines on PCB version C is shown below. The high insertion loss is caused by reflection along the transmission line which was due to larger-than-expected tolerance of the designed characteristic impedance of 50Ω. This issue causes performance degradation in output power, harmonic, and phase noise. If you are evaluating the 8V97003 RF/Microwave Synthesizer on IDT's EVB revision C, this trace loss should be taken into account.

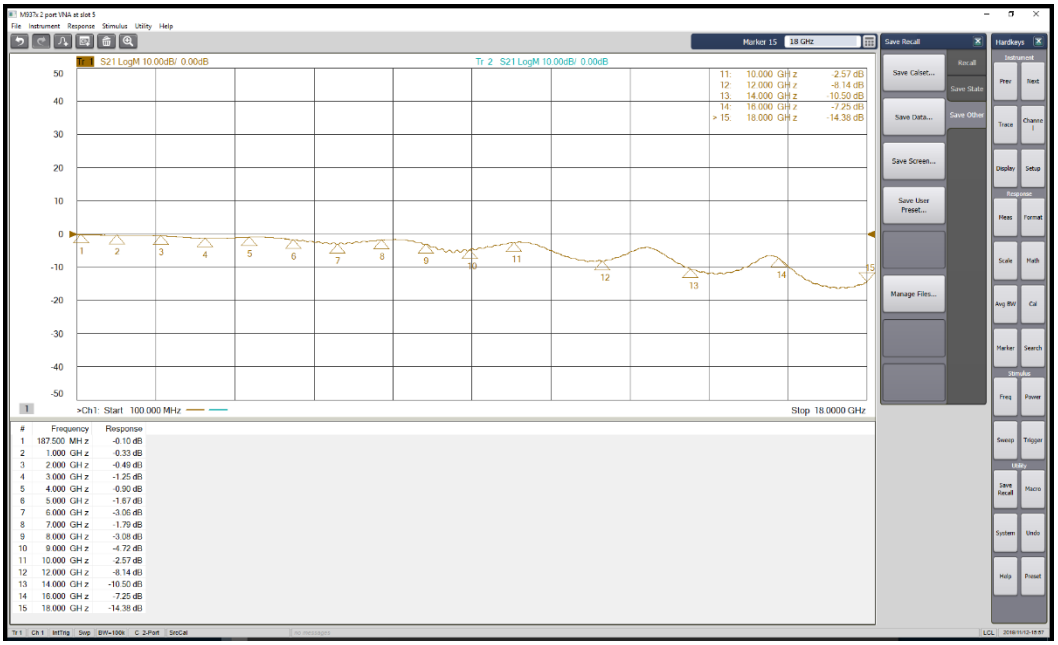


Figure 13. 8V97003 EVB Revision C Transmission Line Loss

5. PCB Layout Guidelines

5.1 8V97003 Evaluation Board Schematic

The 8V79003 evaluation board schematics are located at the end of this document.

6. Bill of Materials (BOM)

Item	Qty	Reference	Part	PCB Footprint	Manufacturer	Part Number
1	35	C2,C3,C4,C6,C7,C8,C9,C10,C32, C33,C35,C39,C40,C41,C42,C49, C52,C53,C55,C59,C61,C65,C66, C67,C68,C71,C75,C76,C78,C82, C83,C85,C87,C96,C99	0.1u	0402M	Murata Electronics NA	GRM155R61A104KA01D
2	8	C11,C12,C36,C56,C62,C72,C79,C86	0.01u	0402M	Taiyo Yuden	EMK105B7103KV-F
3	5	C15,C17,C22,C24,C26	22u	0402M		
4	1	C19	2.2nF	0402M		
5	1	C20	680pF	0402M		
6	1	C88	47nF	0402M		
7	14	C34,C38,C43,C48,C54,C58,C60, C64,C69,C70,C77,C81,C84, C97	10uF	402	Samsung	CL05A106MQ5NUNC
8	5	C37,C47,C57,C63,C80	22uF	0402M		
9	4	C50,C51,C73,C74	4.7uF	402		
10	2	C89,C90	33PF	603		
11	6	FB1,FB2,FB3,FB4,FB5,FB6	BLM18BB22 1SN1D	0603M		
12	6	J1,J2,J3,J4,J6,J8, J16	JACK,SMA,E DGE MOUNT	edge_mount	Samtec	sma-j-p-x-st-em1
13	2	J10,J11	3V3	BANANA_PCB_H_164	Emerson Network Power	108-0740-001
14	1	J12	USB PORT	CONN RCPT USB2.0 MICRO B SMD R/A	Hirose Electric Co Ltd	ZX62-B-5PA(33)
15	4	J5,J13,J14,J15	Test_Point	TP		
16	2	LD1,LD2	LED_0603_120 6_H_GREEN	LED_0603_1206_H	Panasonic	LNJ616C8WRA
17	1	L1	600 ohm 500mA	603	TDK Corporation	MMZ1608Y601B
18	2	L2,L3	18nH,0.4A,36 0mOhm	402	Murata Electronics NA	LQG15HS18NJ02
19	2	R10,R15	50	0402M	Vishay-Dale	FC0402E50R0BST1
20	7	R7,R19,R26, R50, R51, R52, R53	1K	0402M	Panasonic	ERJ-2GEJ102X
21	1	R6	62	0402M		
22	4	R8,R9,R12,R13	2.2K	603		
23	12	R17,R18,R20,R21,R38,R39,R24, R25,R27,R28,R36,R37	0	0402M	Yageo	RC0402JR-070RL
24	4	R1,R2,R3,R4	50	201		
25	1	R16	DNP	603	Panasonic	ERJ-3GEYJ101V
26	2	R22,R29	74K	402		
27	2	R23,R30	DNP_50	402	Vishay-Dale	FC0402E50R0BST1
28	1	R31	680	603	Yageo	RC0603FR-07680FL
29	1	R32	470	603	Yageo	RC0603FR-07470RL
30	2	R34,R35	27	603	Yageo	RC0603FR-0727RL
31	1	R40	1.5K	603	Yageo	RC0603FR-071K5L
32	3	R41,R42,R43	10K	603	Yageo	RC0603FR-0710KL
33	1	SW1	Pushbutton_ EVQPAC04M	PB_EVQPAC04M	Panasonic	EVQ-PAC04M
34	6	TP1,TP2,TP3,TP4,TP5, TP7	VCC_D	TP		
35	1	U1	8V97002	QFN48	IDT	8V97002
36	2	U2,U3	HMC1060LP3E	QFN16	HITTITE	HMC1060LP3E
37	1	U4	ft2232_chip	lqfp48_l	FTDI	FT2232D
38	1	X1	6MHz	XTAL_5mmx7mm	Abracon Corporation	ABMM-6.000MHZ-B2-T
39	6	C1,C5,C13,C14,C91,C92	10000pF	402	AT Ceramics	520L103KT16T
40	1	R5	20	0402M	Panasonic	ERJ-2GEJ200X
41	1	C21	220nF	0402M		
42		U5, U7, R47, R46, R48, R44, R49, R45, C26, C27, C28, R54, R55	DNP			

7. Board Layout

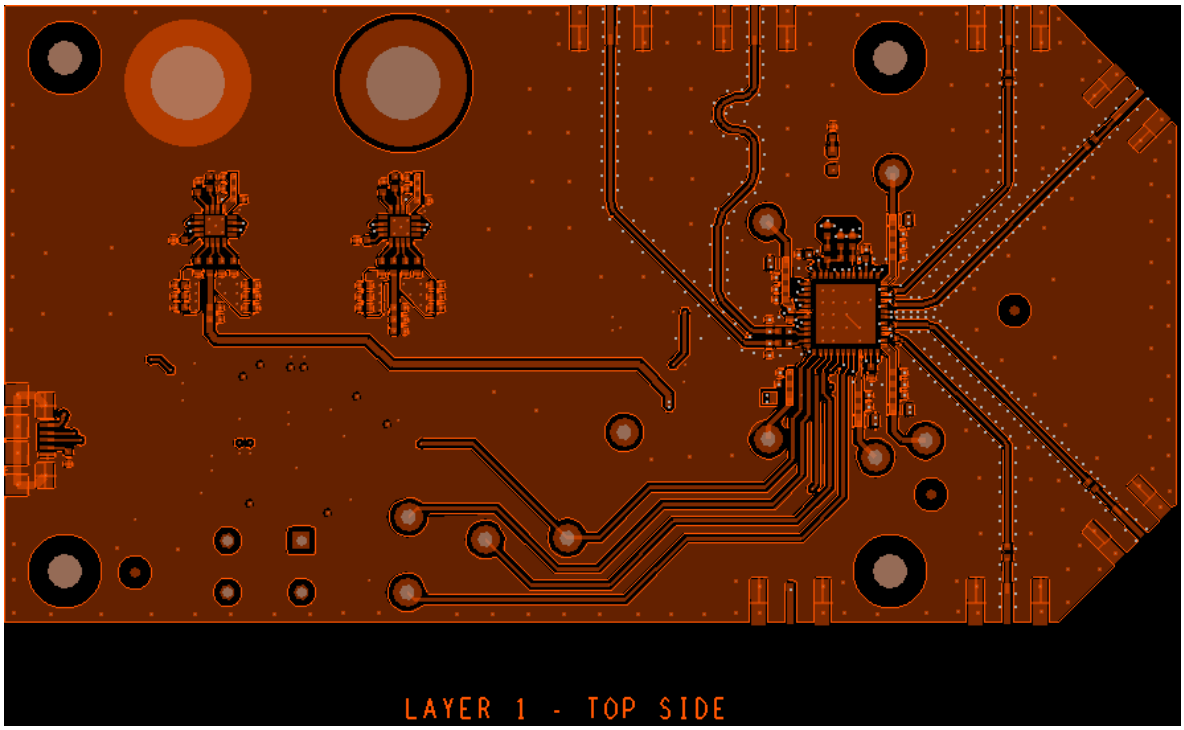


Figure 14. Evaluation Board – Top Layer

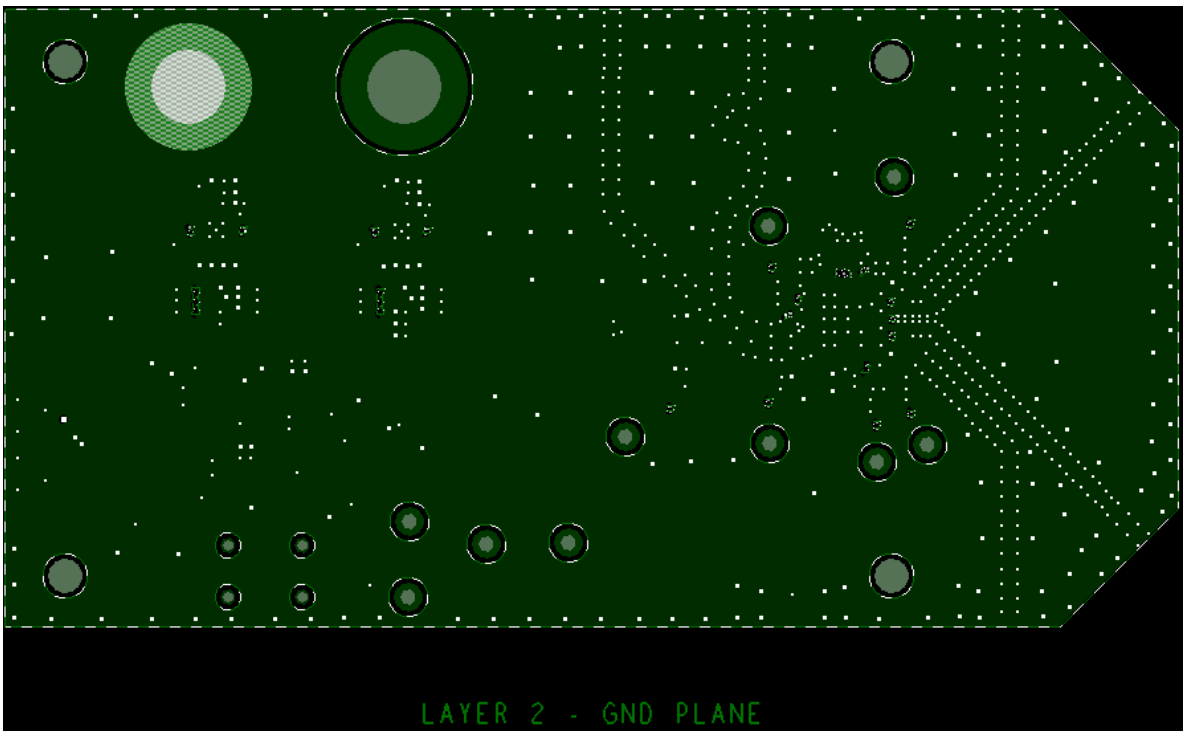


Figure 15. Evaluation Board – Second Layer

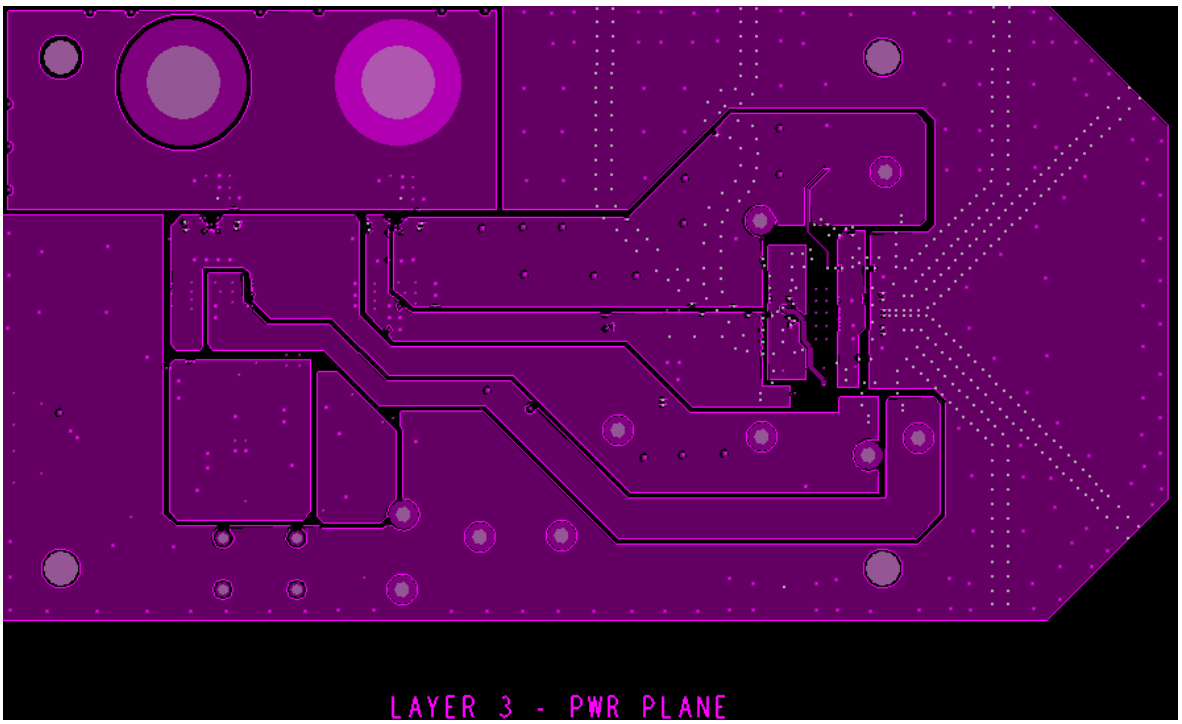


Figure 16. Evaluation Board – Third Layer

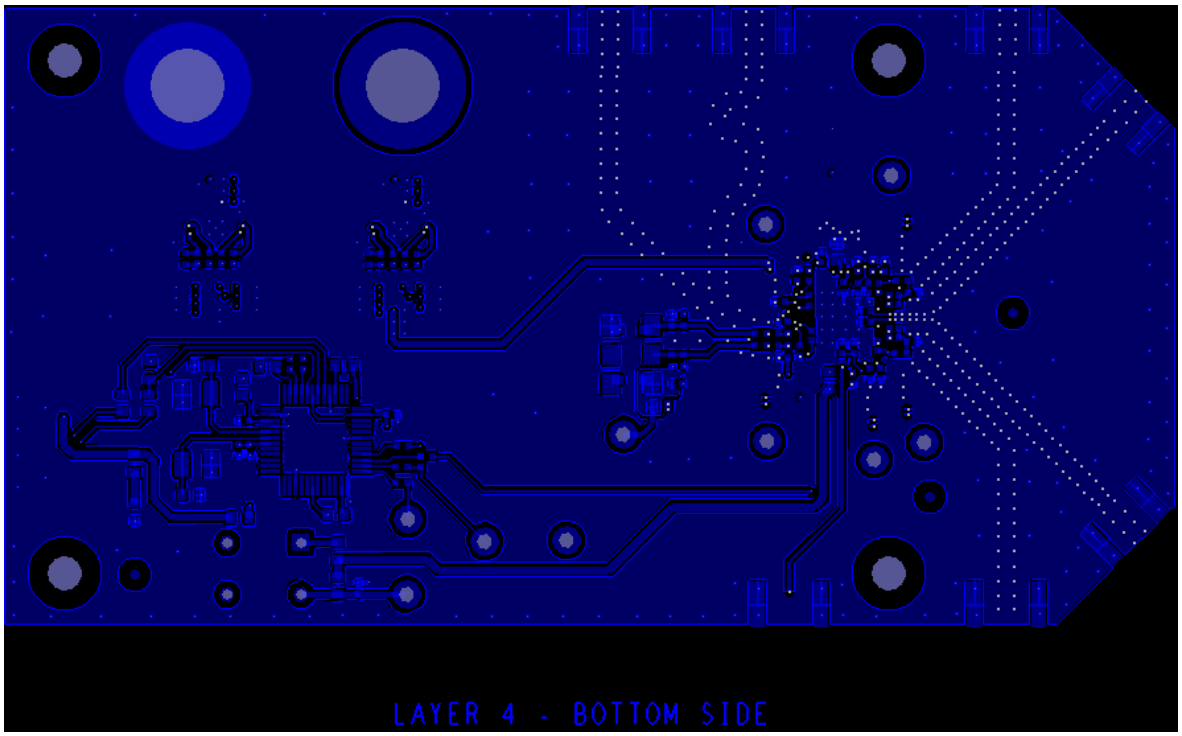


Figure 17. Evaluation Board – Bottom Layer

8. Ordering Information

Contact Renesas Sales at https://www.renesas.com/support.html.

9. Revision History

Revision	Date	Description
1.03	Nov.19.21	Updated 8V97003 Evaluation Board Schematic.
1.02	Sep.25.20	Updated the formatting.
1.01	Oct.22.19	Completed minor changes throughout.
1.0	Nov.15.19	Initial release.

Appendix A – New Configuration Example

Example 1 – New Configuration for Integer Mode of Operation

In this example, we will use Timing Commander GUI to create a new configuration for 8V97003 RF/Microwave Synthesizer device with the following operating parameters:

- Input reference frequency: 245.76MHz – Input signal Type: Differential
- Desired output frequency: 8110.08MHz – Desired Output Power: +2dBm

Follow instructions in section 3.2, steps a) through d) to bring up the GUI for a new configuration. Then enter the operating parameters as followed:

1. Enter Input reference frequency 245.76 to **REF_IN (MHz)** box.
2. Click on Input Buffer icon to open Input Buffer configuration - Check **Differential** box to specify differential input signal.
3. Click on **Input Config** box to open input path configuration to check the PFD frequency. The PFD frequency is automatically calculated based on the REF_IN input and the Desired Output Frequency. Because the Desired Output Frequency is not yet entered, this PFD frequency may change.
4. Enter Desired Output Frequency 8110.08 to **Desired REF_OUTA (MHz)** box.
    a. With REF_IN frequency, input path configuration, and desired output frequency information, the GUI will automatically calculate the feedback divider.
    b. In this case, with REF_IN = 245.76, PFD Frequency = 245.76, RF_OUT = 8110.08, the feedback divider is calculated to be 33.
5. Click on Output driver icon to open RF_OUTA configuration.
    a. Select +2dBm from the Power pull-down menu.
    b. Make sure Power Down = **Regulator Enabled** and Enabled box is checked.
6. Click on Lock Detect icon to open Lock Detect Configuration.
    a. Set Pin Mode = **Digital Lock Detect** (already set by default)
    b. Precision = 6.4ns
7. Set operating Charge Pump current.
    a. By default, charge pump current is set to 5mA.
    b. Charge pump current can be used to vary the loop bandwidth, therefore optimize phase noise and/or integrated RMS jitter. Set Pmos = 8.5mA, Nmos = 8.5mA to get the performance shown in the phase noise plot in Figure 22.

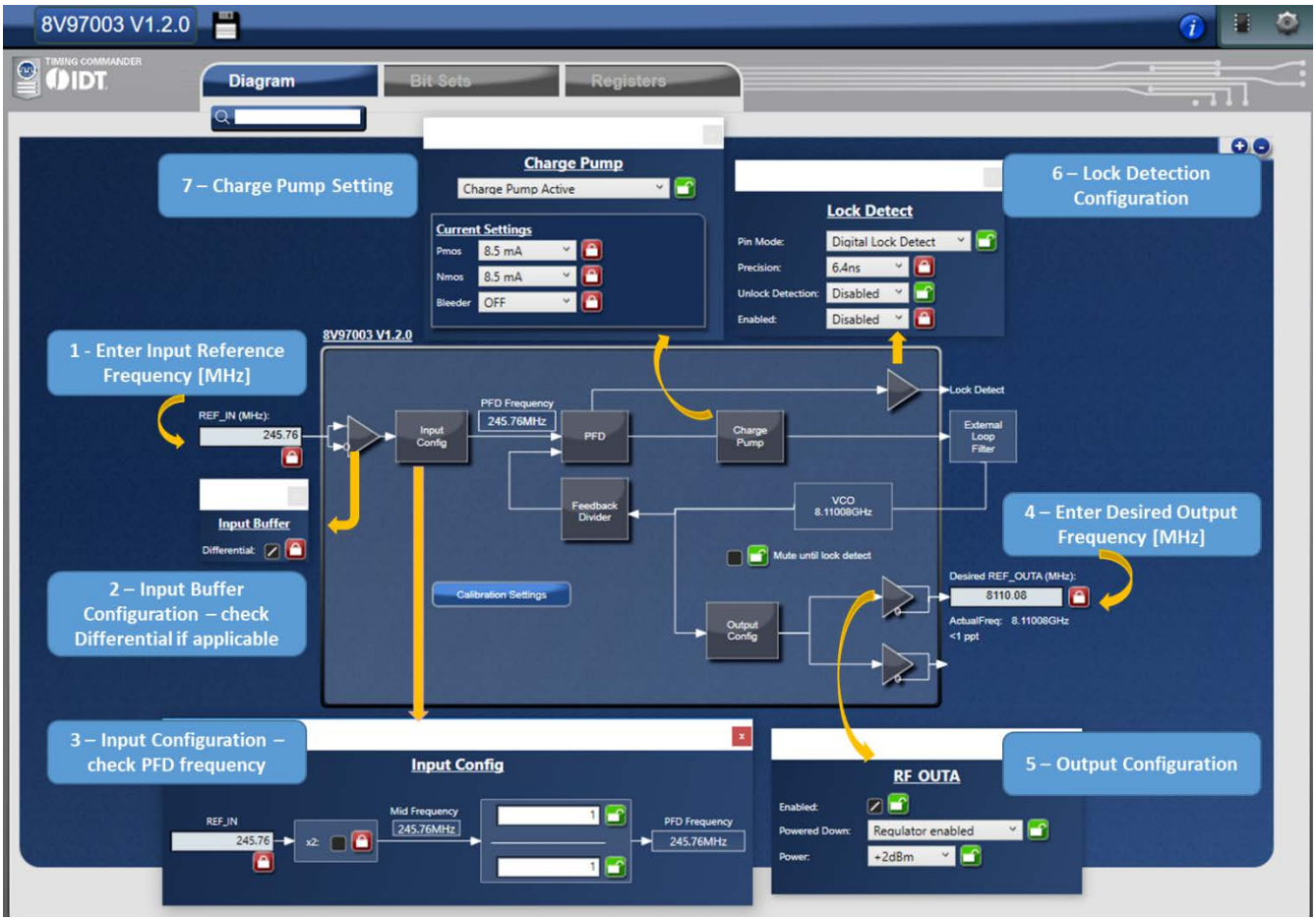


Figure 18. Timing Commander GUI for Creating New Integer Mode Configuration

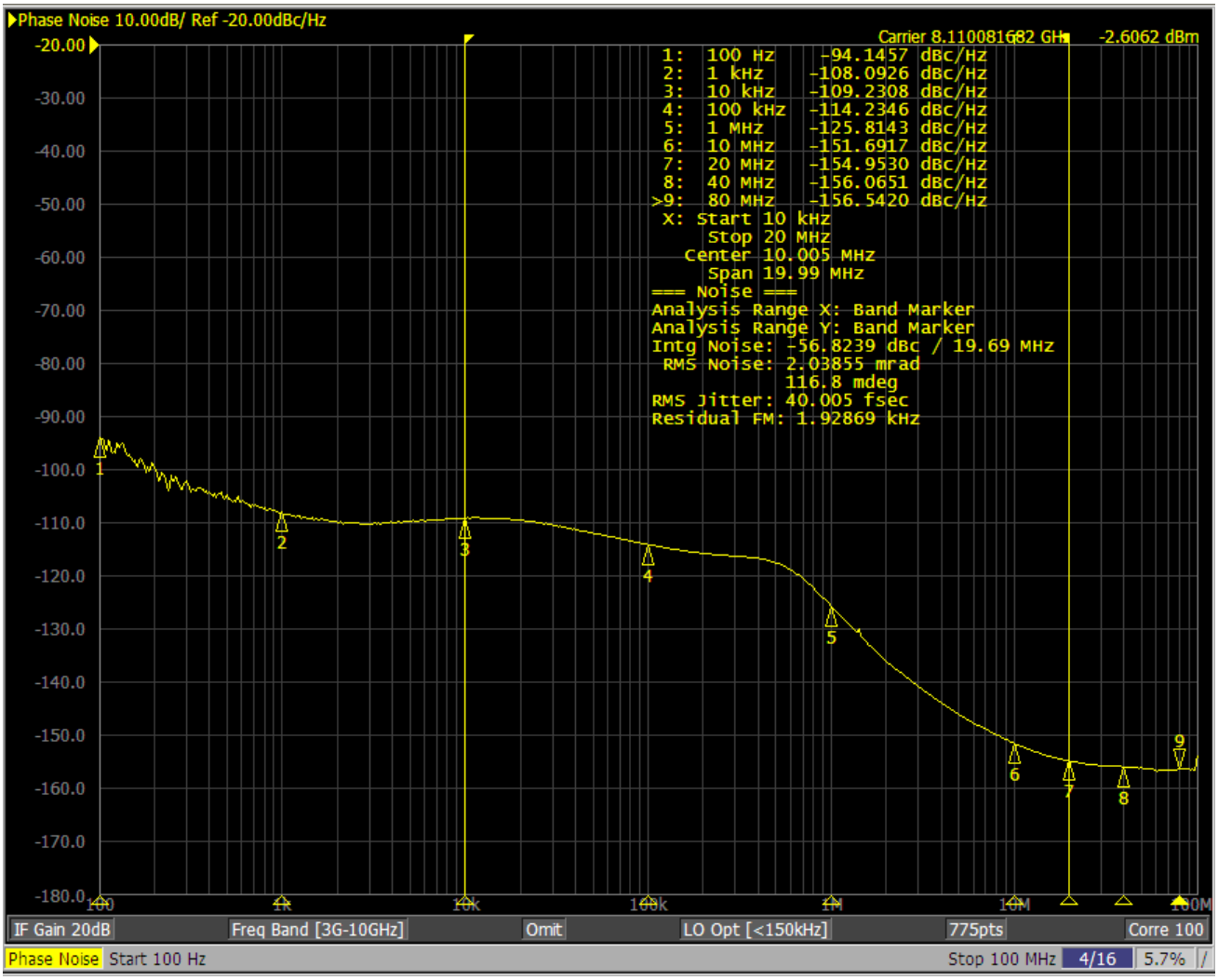


Figure 19. Expected Performance of 8110.08MHz Output from Example 1

Example 2 – New Configuration for Fractional Mode of Operation

In this example, we will use Timing Commander GUI to create a new configuration for 8V97003 RF/Microwave Synthesizer device with the following operating parameters:

- Input reference frequency: 245.76MHz – Input signal Type: Differential
- Desired output frequency: 8200MHz – Desired Output Power: +2dBm

Follow instructions in section 3.2, steps a) through d) to bring up the GUI for a new configuration. Then enter the operating parameters as followed:

1. Enter Input reference frequency 245.76 to **REF_IN (MHz)** box
2. Click on Input Buffer icon to open Input Buffer configuration - Check **Differential** box to specify differential input signal
3. Click on **Input Config** box to open input path configuration to check the PFD frequency. The PFD frequency is automatically calculated based on the REF_IN input and the Desired Output Frequency. Because the Desired Output Frequency is not yet entered, this PFD frequency may change.
4. Enter Desired Output Frequency 8200 to **Desired REF_OUTA (MHz)** box
    a. With REF_IN frequency, input path configuration, and Desired output frequency information, the GUI will automatically calculate the feedback divider
    b. In this case, with REF_IN = 245.76, PFD Frequency = 245.76, RF_OUT = 8200, the feedback divider is calculated to be 33.36588 = 33
5. Click on Output driver icon to open RF_OUTA configuration
    a. Select +2dBm from the Power pull-down menu
    b. Make sure Power Down = **Regulator Enabled** and Enabled box is checked
6. Click on Lock Detect icon to open Lock Detect Configuration
    a. Set Pin Mode = **Digital Lock Detect** (already set by default)
    b. Precision = 6.4ns
7. Set operating Charge Pump current
    a. By default, charge pump current is set to 5mA
    b. Charge pump current can be used to vary the loop bandwidth, hence optimize phase noise and/or integrated RMS jitter. Set Pmos = 8.5mA, Nmos = 8.5mA, Bleeder = OFF. With the Bleeder off, the noise from the modulator will degrade phase noise performance as shown in Figure 18
    c. Set Pmos = 8.5mA, Nmos = 8.5mA, Bleeder = 1100µA to improve phase noise performance as shown in Figure 19

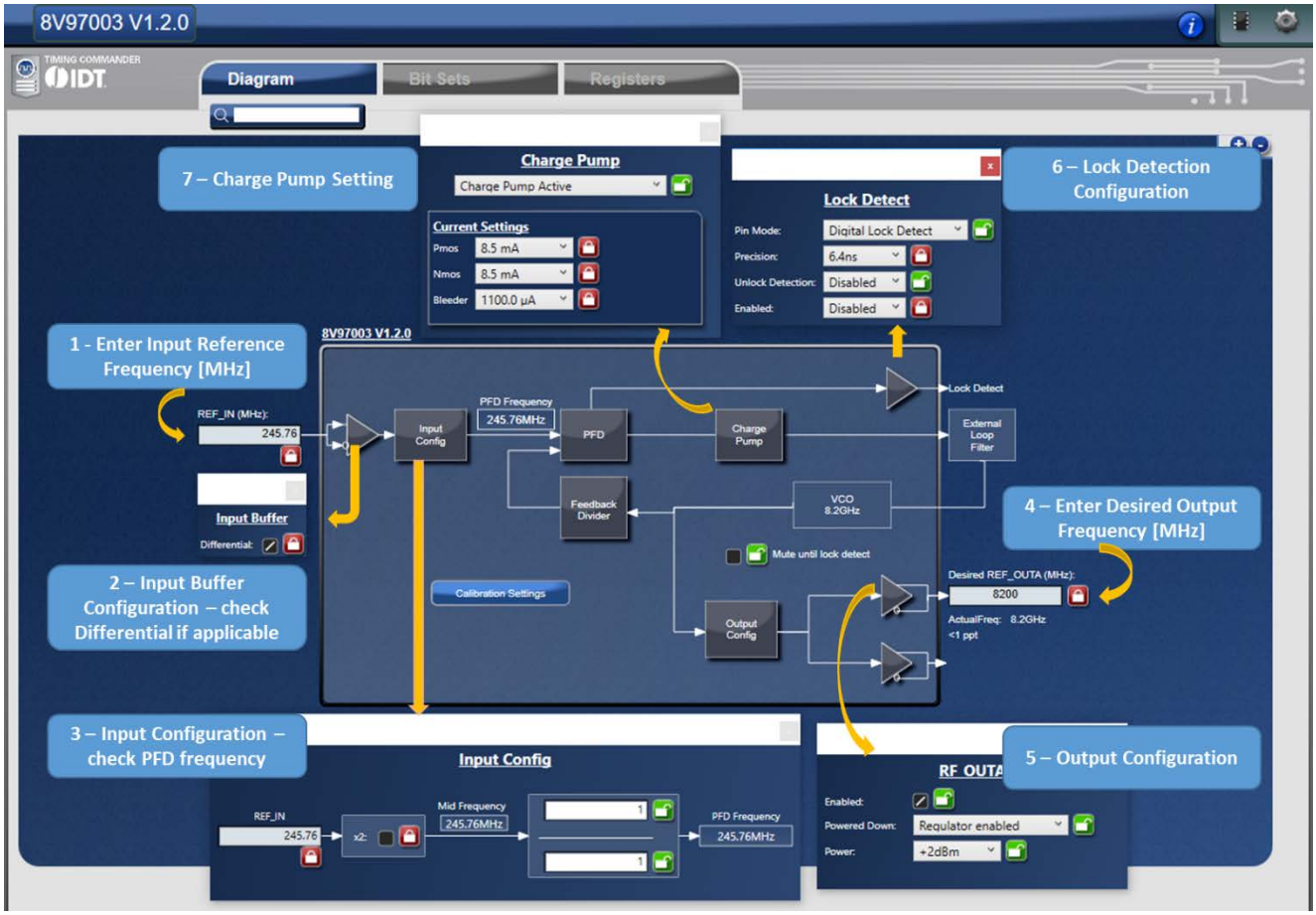


Figure 20. Timing Commander GUI for Creating New Fractional Mode Configuration

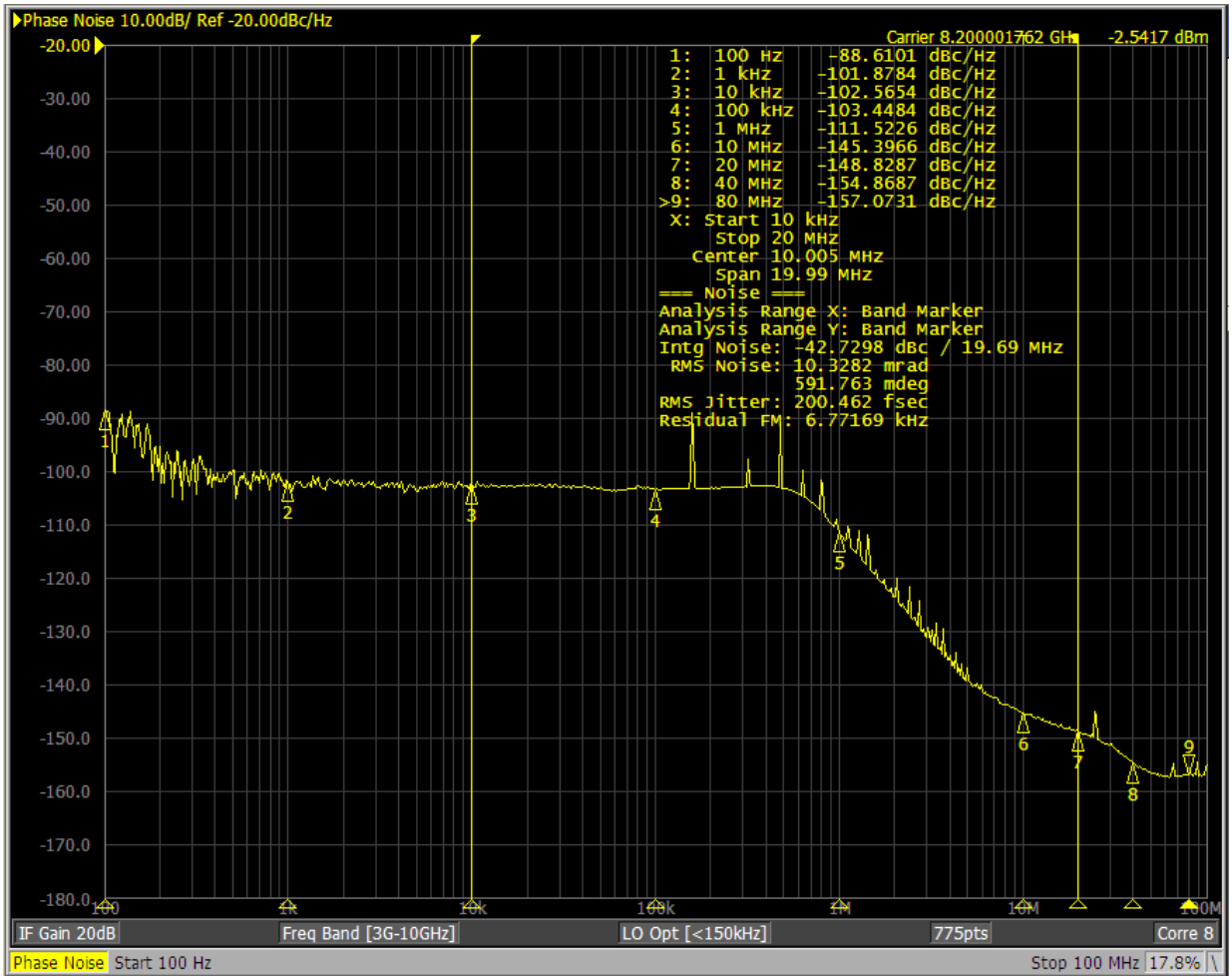


Figure 21. Expected Performance of 8200MHz Output without Bleeder Current from Example 2

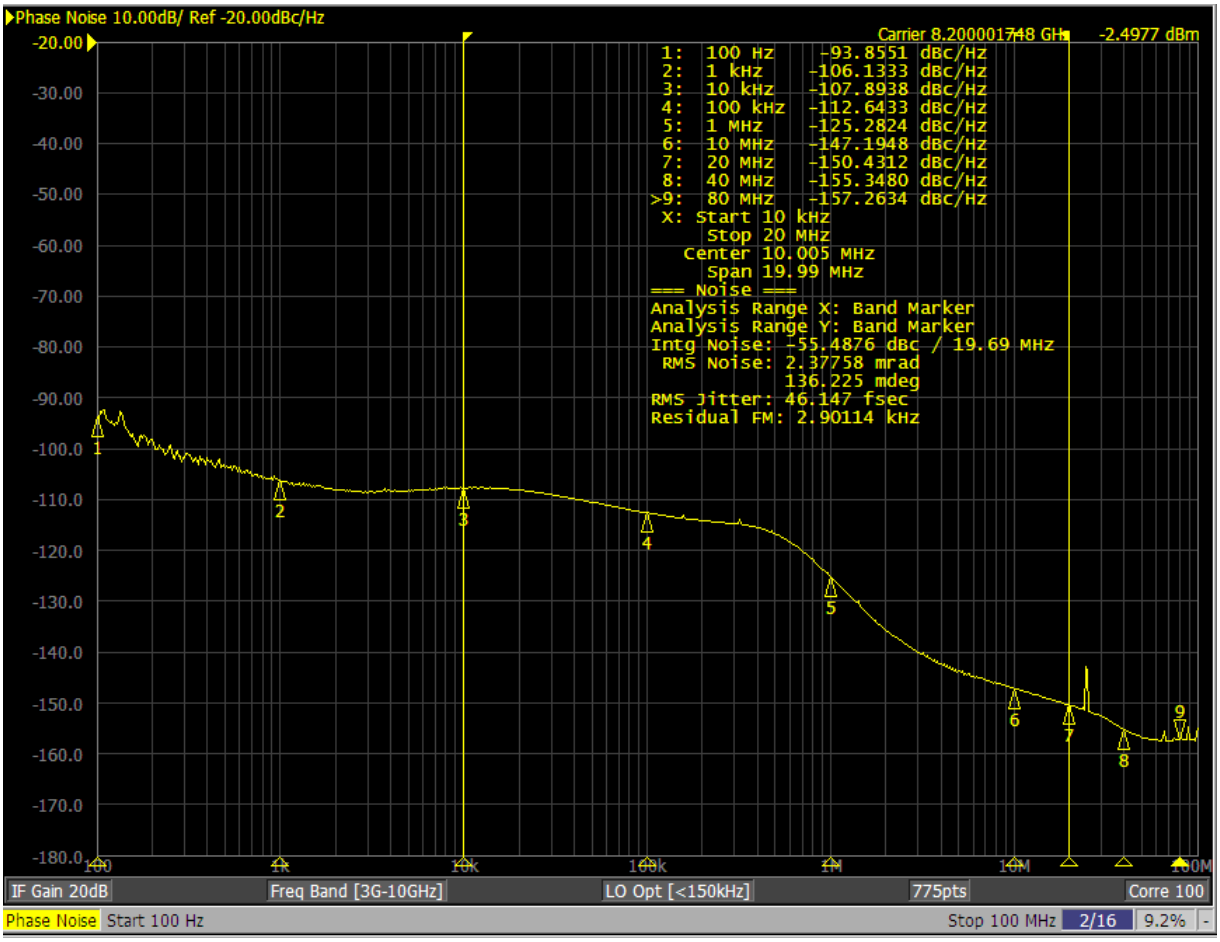


Figure 22. Expected Performance of 8200MHz Output with 1.1mA of Bleeder Current from Example 2

Appendix B – Input Reference Phase Noise Performance

Phase noise measurement results shown in Figure 22, Figure 24, and Figure 25 were obtained with the input reference clock from a bench signal generator. Because the in-band phase noise performance of 8V97003 RF/Microwave Synthesizer is dictated by the phase noise performance of the input reference, the input reference's phase noise performance is provided in Figure 26.

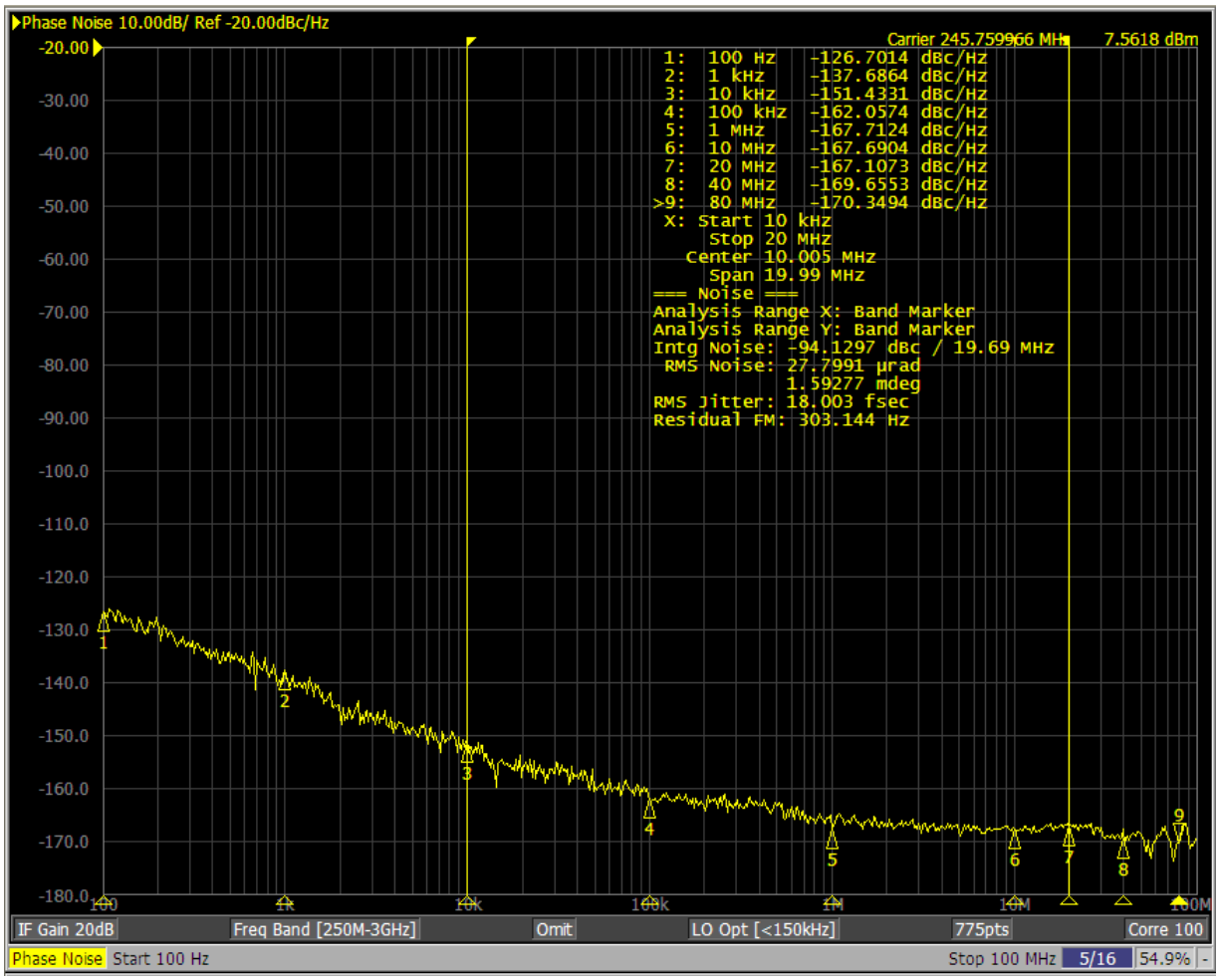
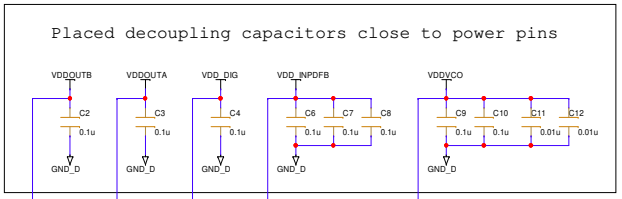
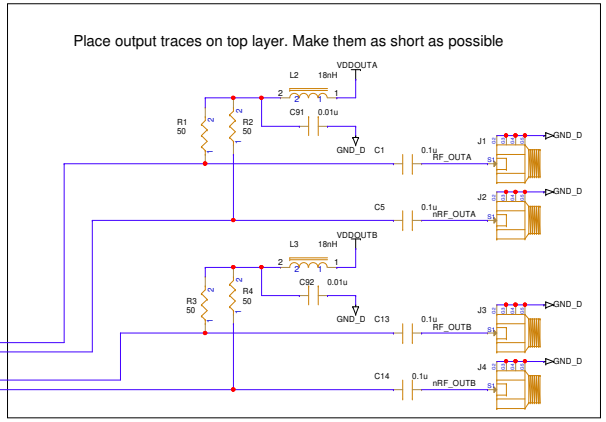


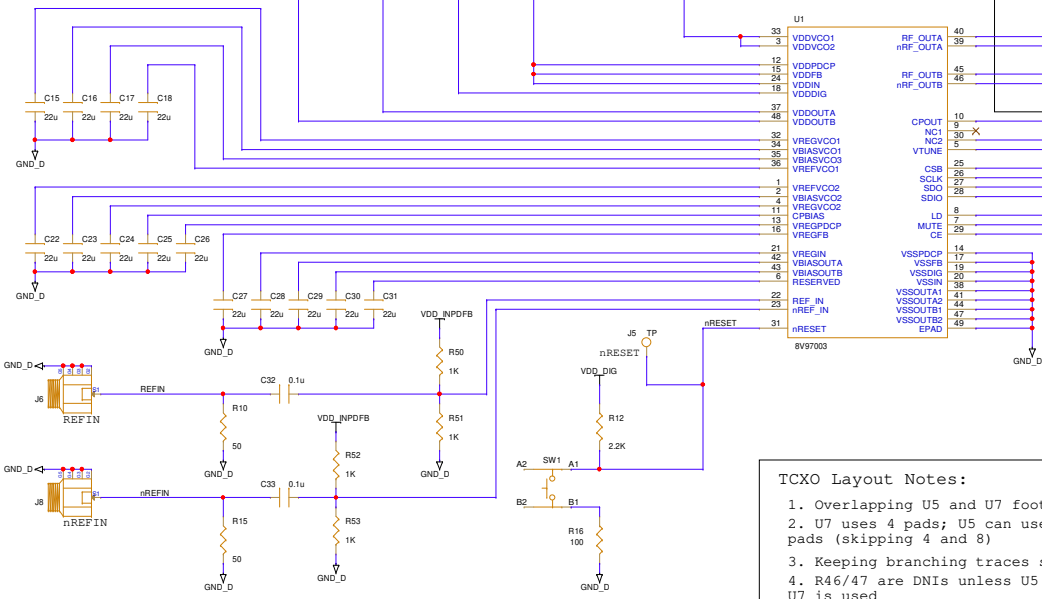
Figure 23. Phase Noise Performance of 245.76MHz Input Reference Clock

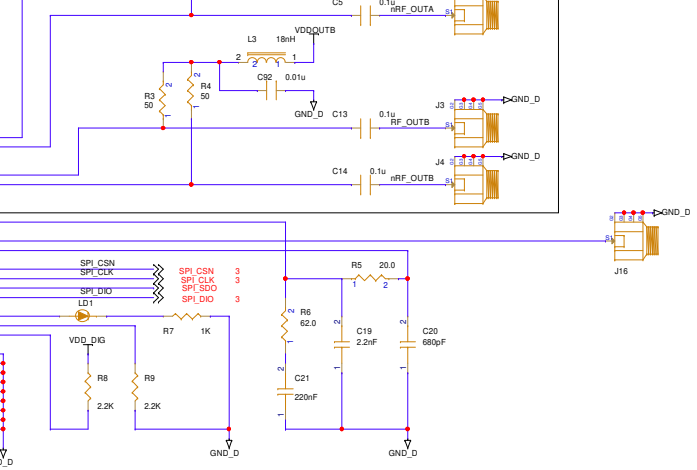
Board Layer Stack-up (62mil)

TOP LAYER 1oz COPPER
GROUND PLANE
POWER PLANE
BOTTOM LAYER 1oz COPPER



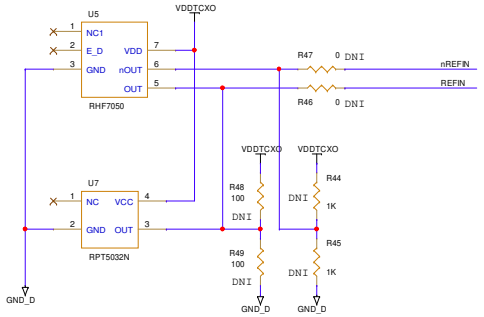






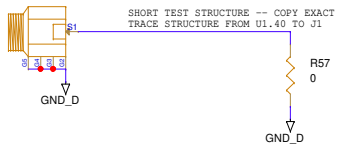
TCXO Layout Notes:

1. Overlapping U5 and U7 footprint
2. U7 uses 4 pads; U5 can use 6 pads (skipping 4 and 8)
3. Keeping branching traces short
4. R46/47 are DNIs unless U5 or U7 is used
5. R44/45 and R48/49 are used only when U7 is used
6. Place R46/R47 close to the branching point merging with SMA traces of the same net names.

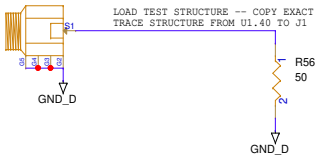


Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: 07/21/2021	Sheet 1 of 3		

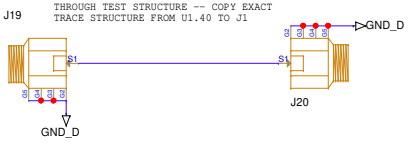
J17



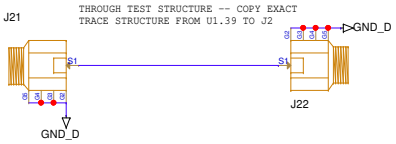
J18



J19



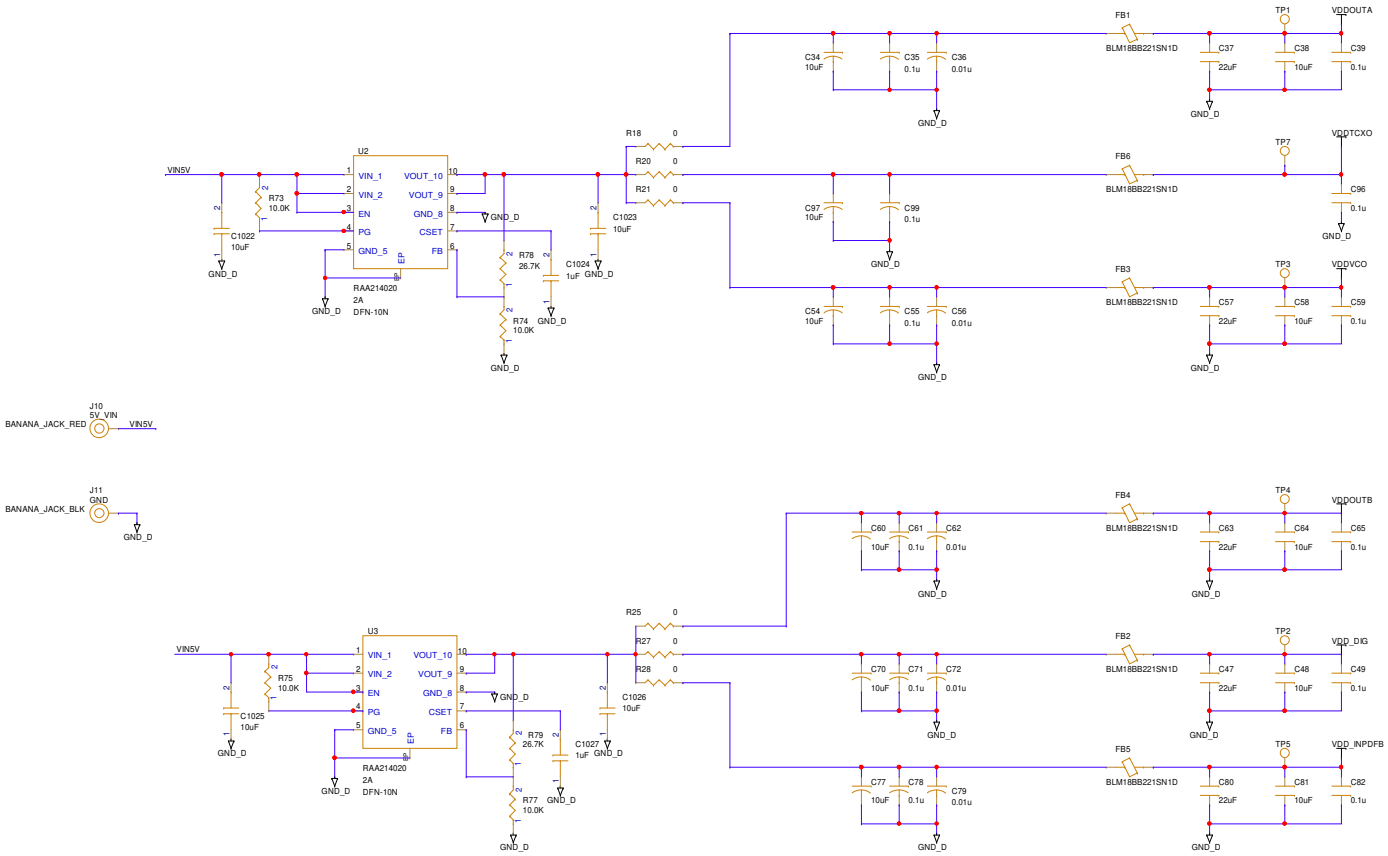
J21



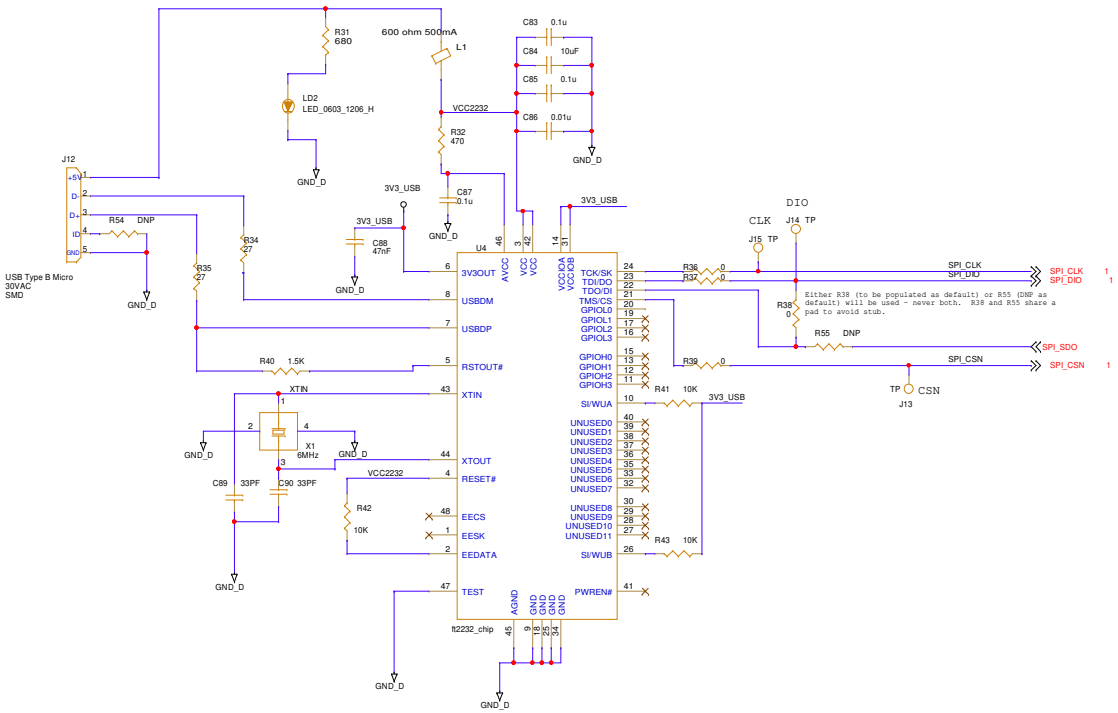
Integrated Device Technology
1140 West Warner Rd.
Tempe, AZ 85284

Title: HW-CLK-103

Size	Part Number:	Engineer:	Rev.
B	987456321587	LP	A
	Date: 07/19/2021	Sheet: 1 of 1	



Title	IDT8V97002_Char	
Size C	Document Number <Doc>	Rev <RevCode>
Date: 07/19/2021	Sheet 2 of 3	



Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: 07/19/2021	Sheet 3 of 3		

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.