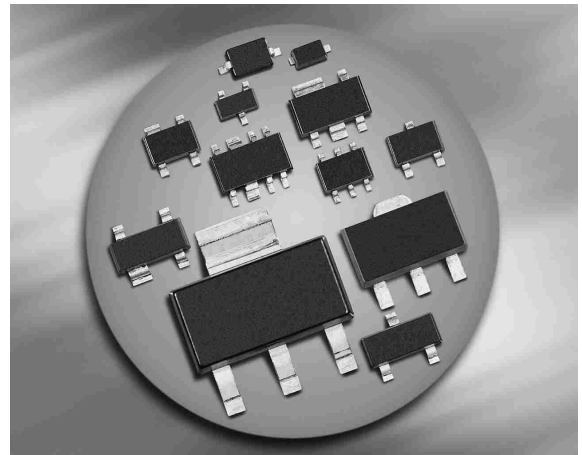
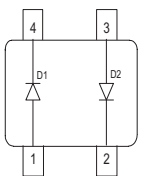
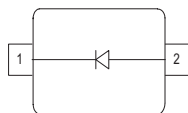
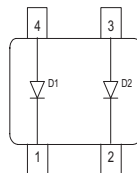
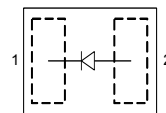
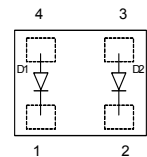
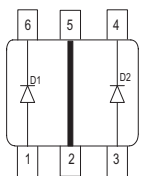


Silicon Schottky Diode

- Low barrier diode for detectors up to GHz frequencies
- Pb-free (RoHS compliant) package


BAT62

**BAT62-03W
BAT62-02V
BAT62-02W**

BAT62-07W

**BAT62-02L
BAT62-02LS**

BAT62-07L4

BAT62-09S


ESD (Electrostatic discharge) sensitive device, observe handling precaution!

| Type | Package | Configuration | L_S (nH) | Marking |
|-------------|-----------|-------------------------------|------------|---------|
| BAT62-02W** | SCD80 | single | 0.6 | 62 |
| BAT62 | SOT143 | anti-parallel pair | 2 | 62s |
| BAT62-02L | TSLP-2-1 | single, leadless | 0.4 | L |
| BAT62-02LS* | TSSLP-2-1 | single, leadless | 0.2 | U |
| BAT62-02V | SC79 | single | 0.6 | k |
| BAT62-03W | SOD323 | single | 1.8 | white L |
| BAT62-07L4 | TSLP-4-4 | parallel pair, leadless | 0.4 | 62 |
| BAT62-07W | SOT343 | parallel pair | 1.8 | 62s |
| BAT62-09S | SOT363 | parallel high, high isolation | 1.6 | 69s |

* Preliminary Data

** Not for new design

Maximum Ratings at $T_A = 25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Value | Unit |
|--|-----------|---------------------------------|------|
| Diode reverse voltage | V_R | 40 | V |
| Forward current | I_F | 20 | mA |
| Total power dissipation BAT62, $T_S \leq 85\text{ °C}$ BAT62-02L, -07L4, -03W, $T_S \leq 108\text{ °C}$ BAT62-02W, -02V, $T_S \leq 109\text{ °C}$ BAT62-07W, $T_S \leq 103\text{ °C}$ BAT62-09S, $T_S \leq 105\text{ °C}$ | P_{tot} | 100 100 100 100 100 | |
| Junction temperature | T_j | 150 | °C |
| Storage temperature | T_{stg} | -55 ... 150 | |

Thermal Resistance

| Parameter | Symbol | Value | Unit |
|---|------------|--|------|
| Junction - soldering point ¹⁾ BAT62 BAT62-02L, -07L4, -03W BAT62-02W, 02V BAT62-07W BAT62-09S | R_{thJS} | ≤ 650 ≤ 420 ≤ 410 ≤ 470 $\leq tbd$ | |

Electrical Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit |
|---|--------------|--------|------|------|---------------|
| | | min. | typ. | max. | |
| Reverse current $V_R = 40\text{ V}$ | I_R | - | - | 10 | μA |
| Forward voltage $I_F = 2\text{ mA}$ | V_F | - | 0.58 | 1 | V |
| Forward voltage matching ²⁾ $I_F = 2\text{ mA}$ | ΔV_F | - | - | 20 | mV |

¹⁾For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)

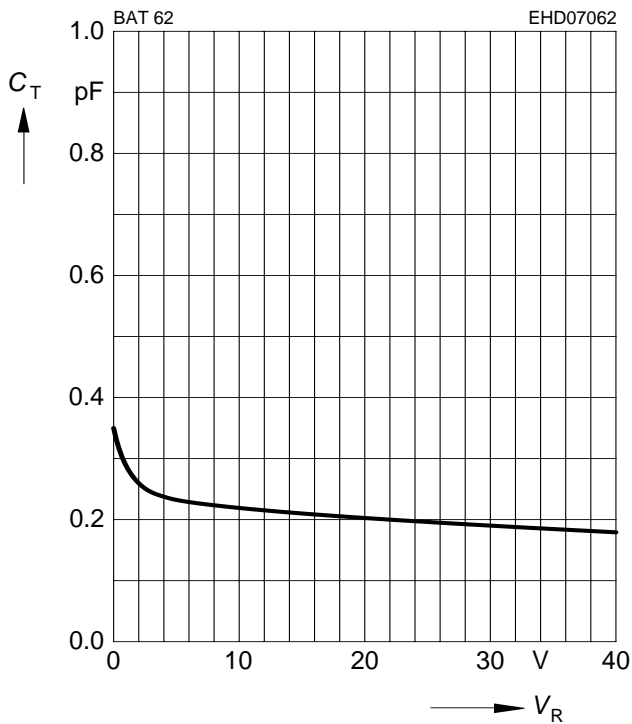
²⁾ ΔV_F is the difference between lowest and highest V_F in a multiple diode component.

Electrical Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit |
|---|--------|--------|------|------|------------|
| | | min. | typ. | max. | |
| AC Characteristics | | | | | |
| Diode capacitance $V_R = 0\text{ V}$, $f = 1\text{ MHz}$ | C_T | - | 0.35 | 0.6 | pF |
| Differential resistance $V_R = 0\text{ V}$, $f = 10\text{ kHz}$ | R_0 | - | 225 | - | k Ω |

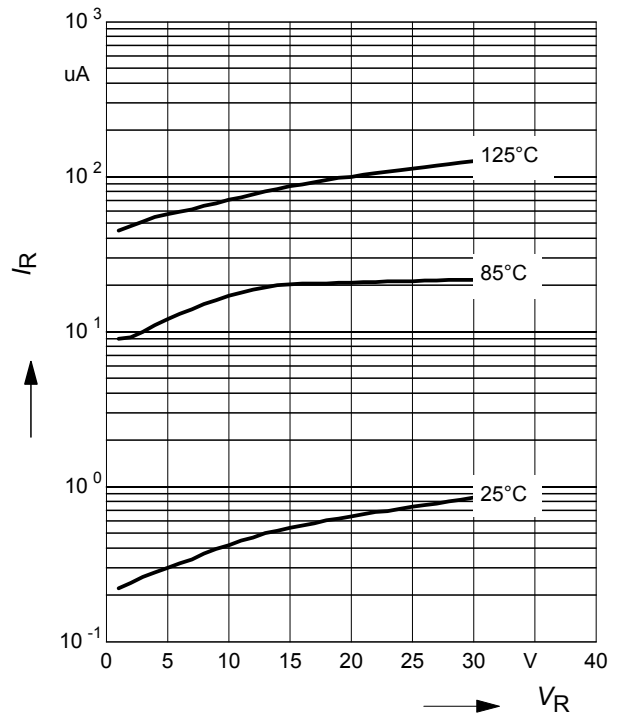
Diode capacitance $C_T = f(V_R)$

$f = 1\text{MHz}$



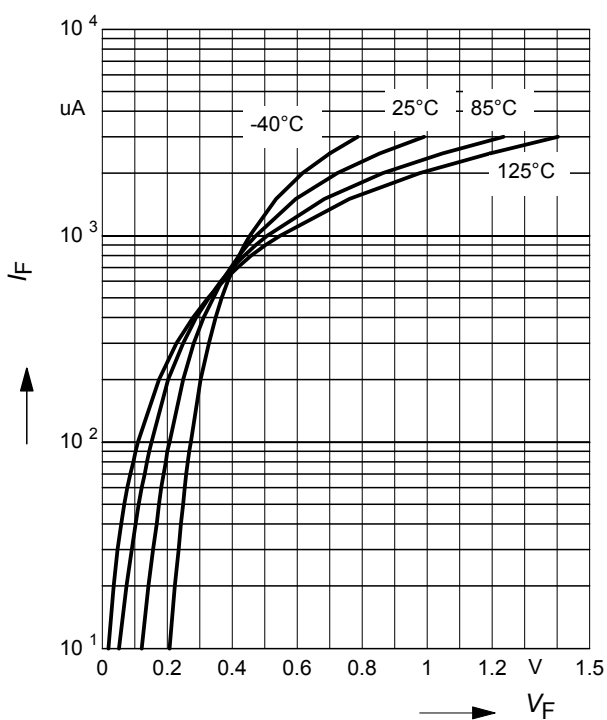
Reverse current $I_R = f(V_R)$

$T_A = \text{Parameter}$



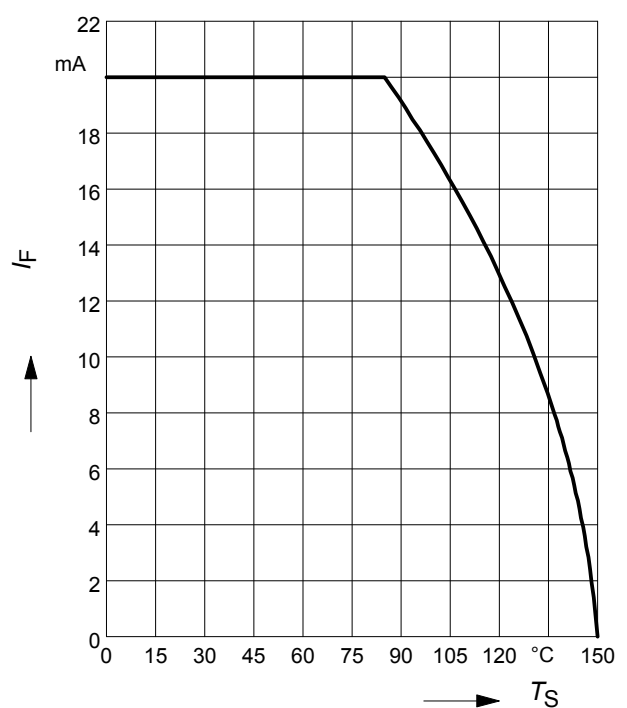
Forward current $I_F = f(V_F)$

$T_A = \text{Parameter}$



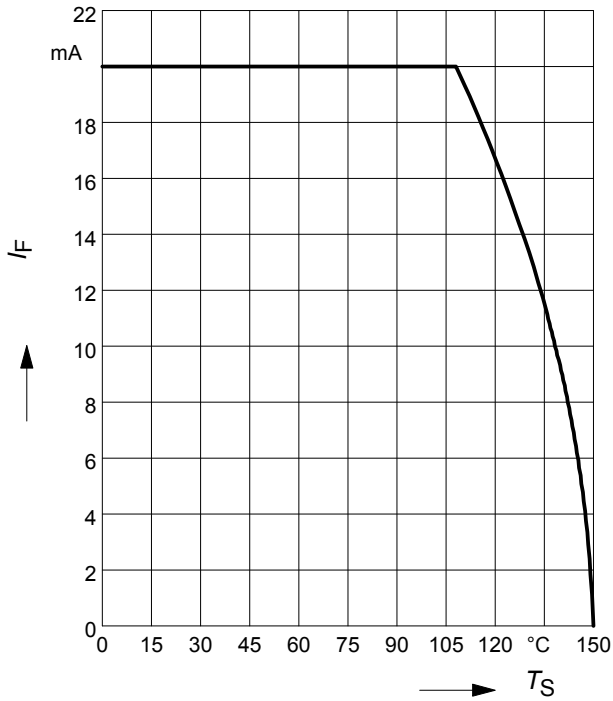
Forward current $I_F = f(T_S)$

BAT62



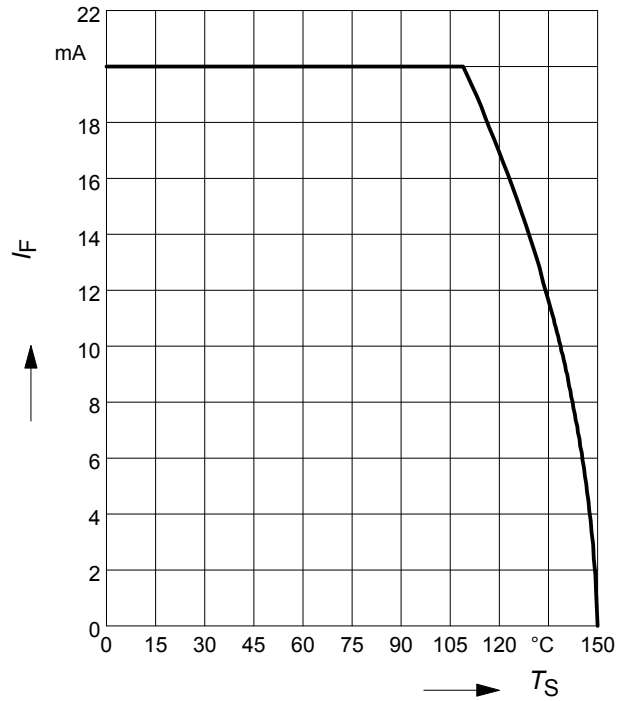
Forward current $I_F = f(T_S)$

BAT62-02L, -07L4



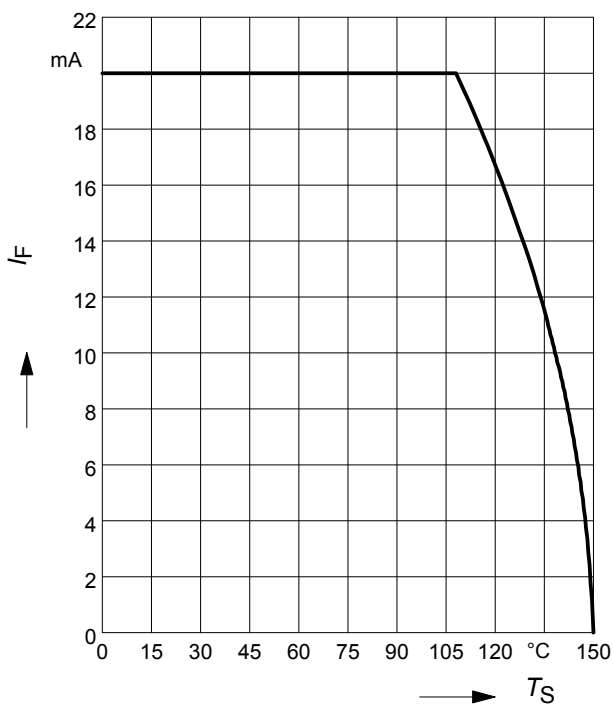
Forward current $I_F = f(T_S)$

BAT62-02W, -02V



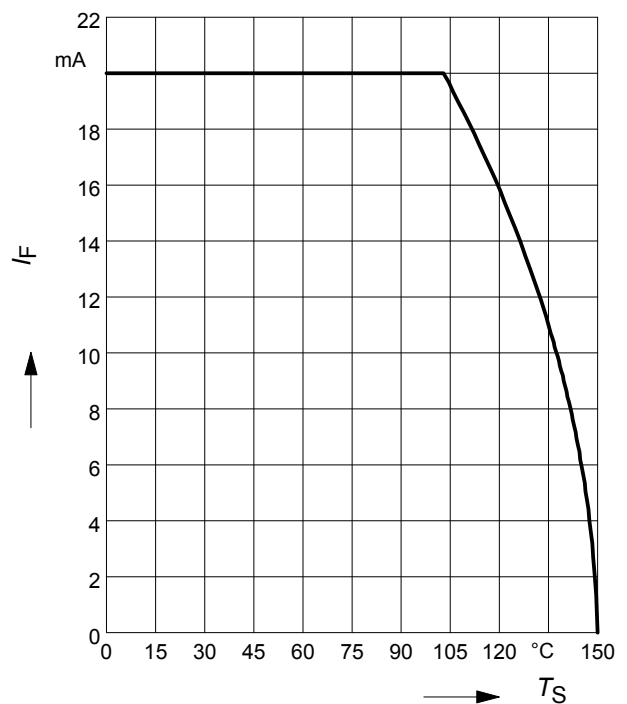
Forward current $I_F = f(T_S)$

BAT62-03W



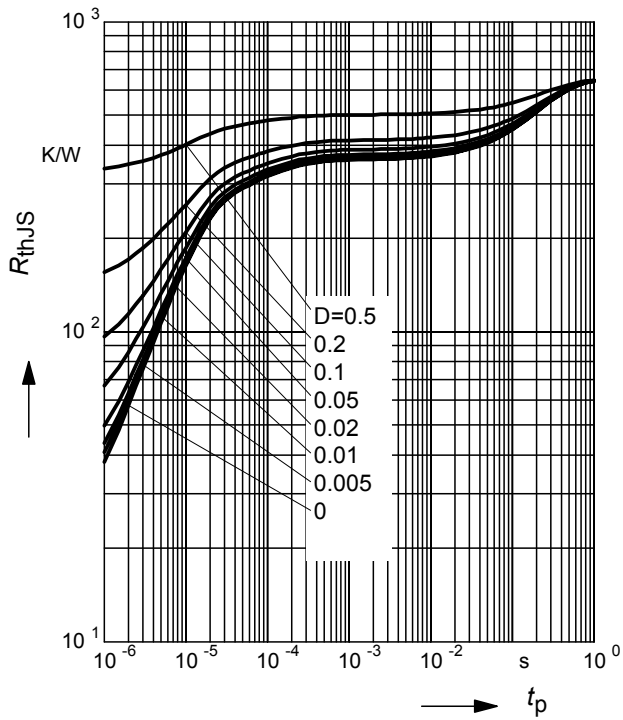
Forward current $I_F = f(T_S)$

BAT62-07W



Permissible Puls Load $R_{thJS} = f(t_p)$

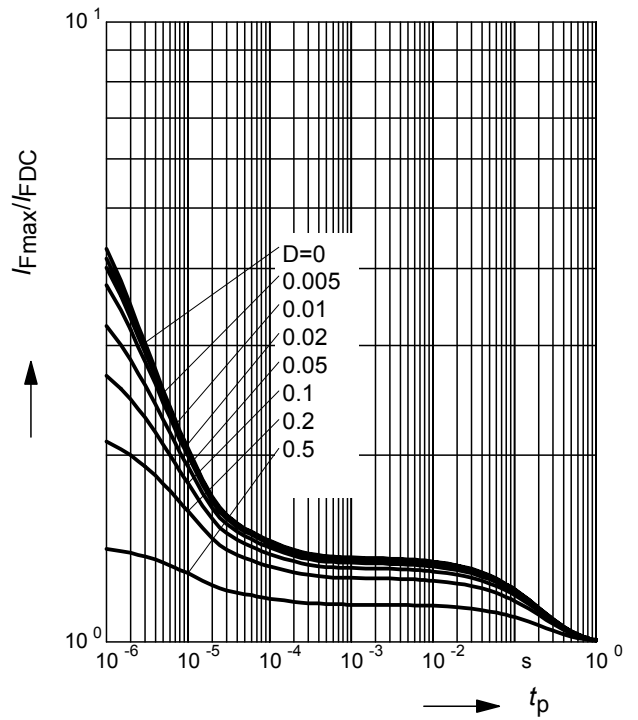
BAT62



Permissible Pulse Load

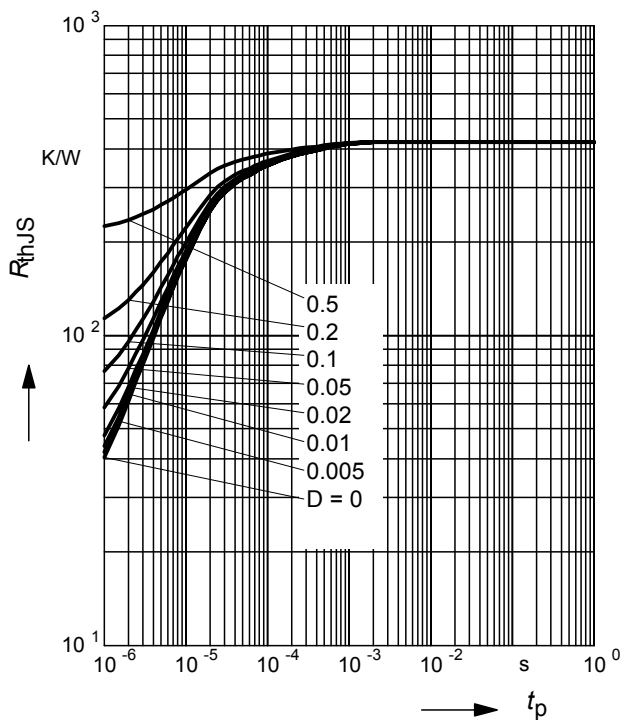
$I_{Fmax} / I_{FDC} = f(t_p)$

BAT62



Permissible Puls Load $R_{thJS} = f(t_p)$

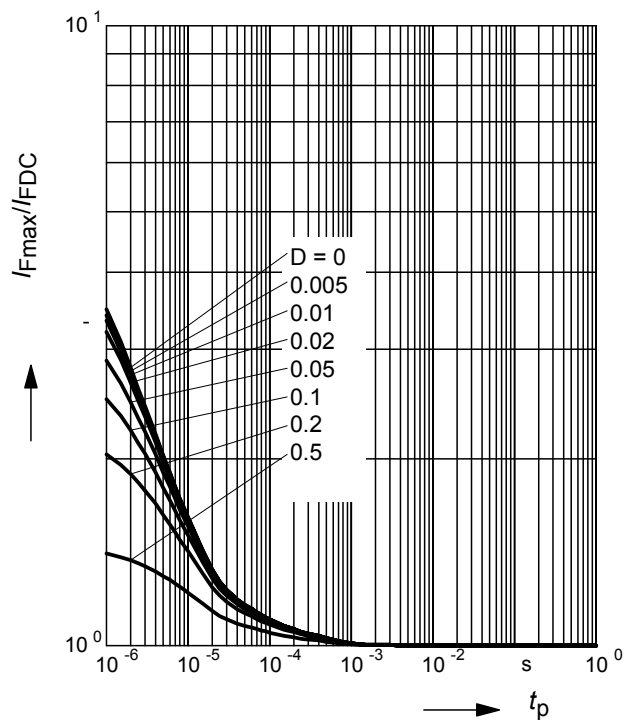
BAT62-02L, -07L4



Permissible Pulse Load

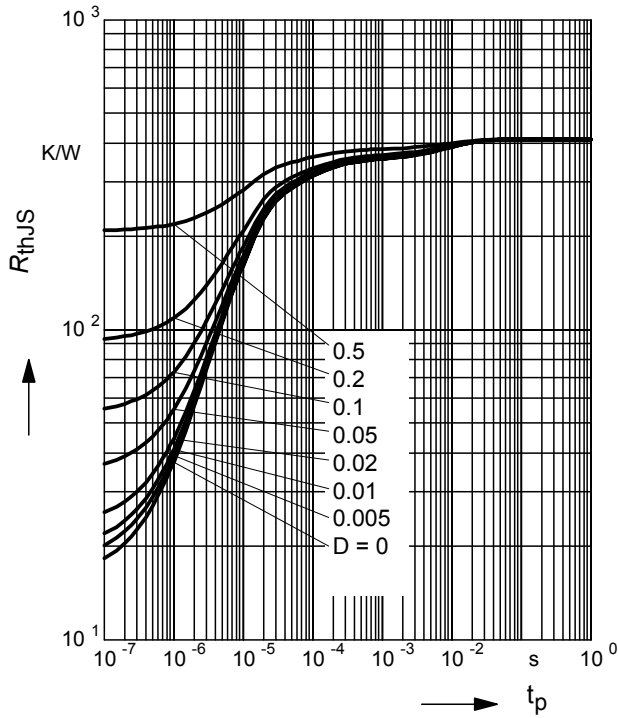
$I_{Fmax} / I_{FDC} = f(t_p)$

BAT62-02L, -07L4



Permissible Puls Load $R_{thJS} = f(t_p)$

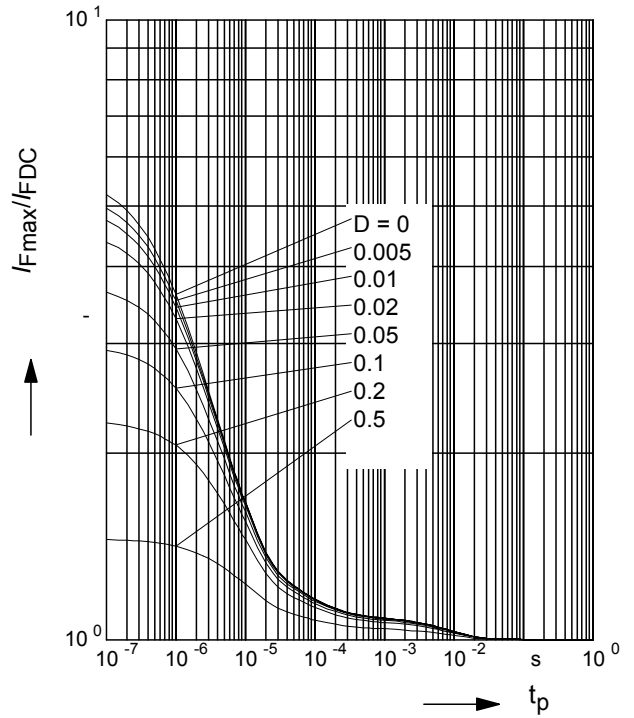
BAT62-02W, 02V



Permissible Pulse Load

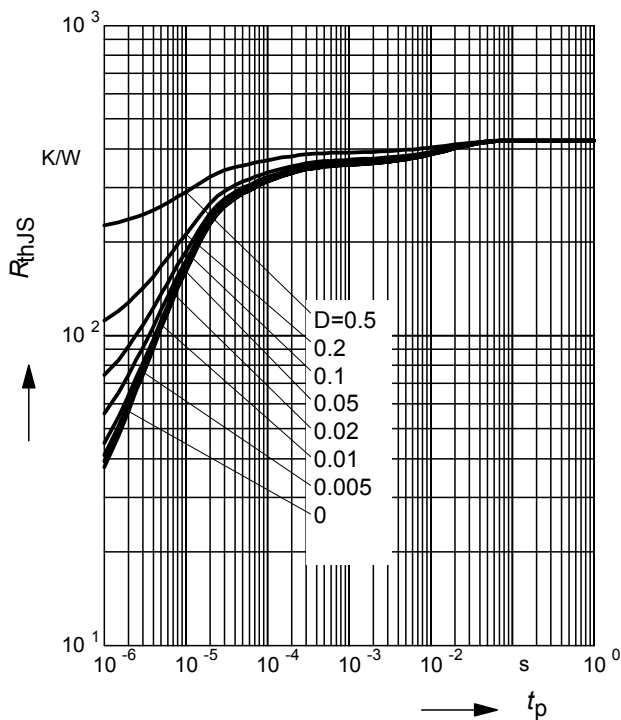
$I_{Fmax} / I_{FDC} = f(t_p)$

BAT62-02W, -02V



Permissible Puls Load $R_{thJS} = f(t_p)$

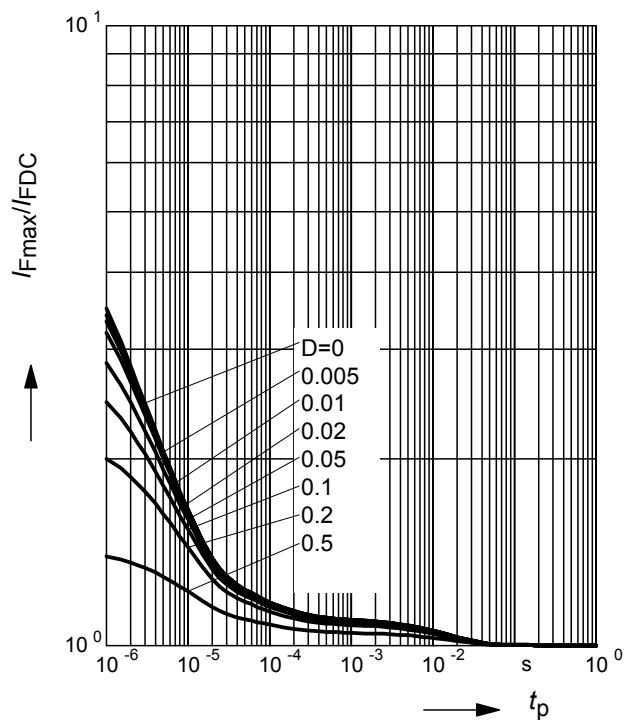
BAT62-03W



Permissible Pulse Load

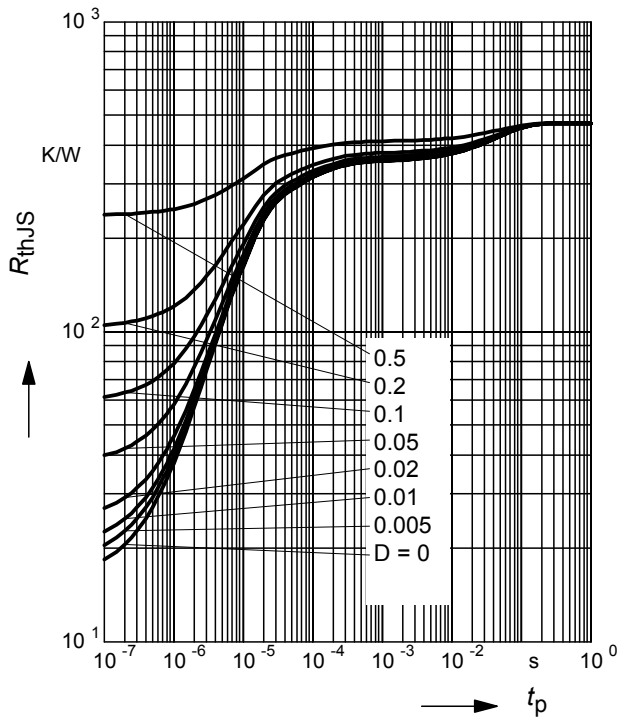
$I_{Fmax} / I_{FDC} = f(t_p)$

BAT62-03W



Permissible Puls Load $R_{thJS} = f(t_p)$

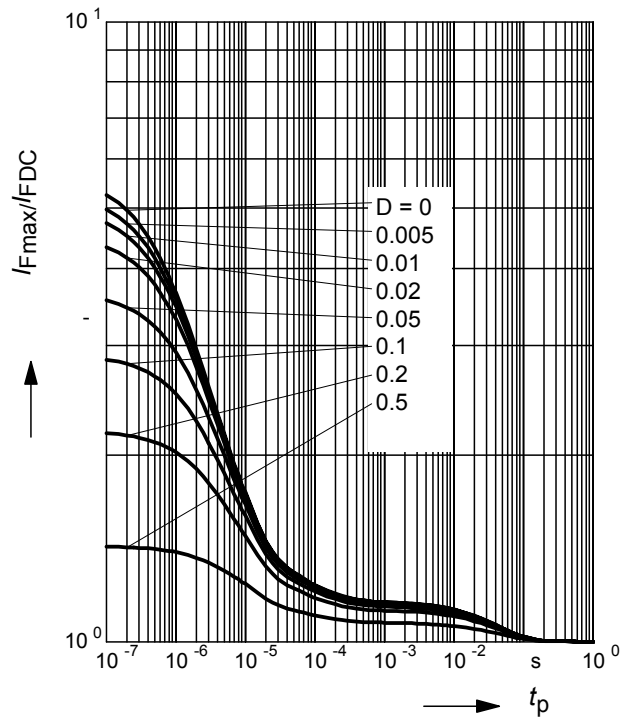
BAT62-07W



Permissible Pulse Load

$I_{Fmax} / I_{FDC} = f(t_p)$

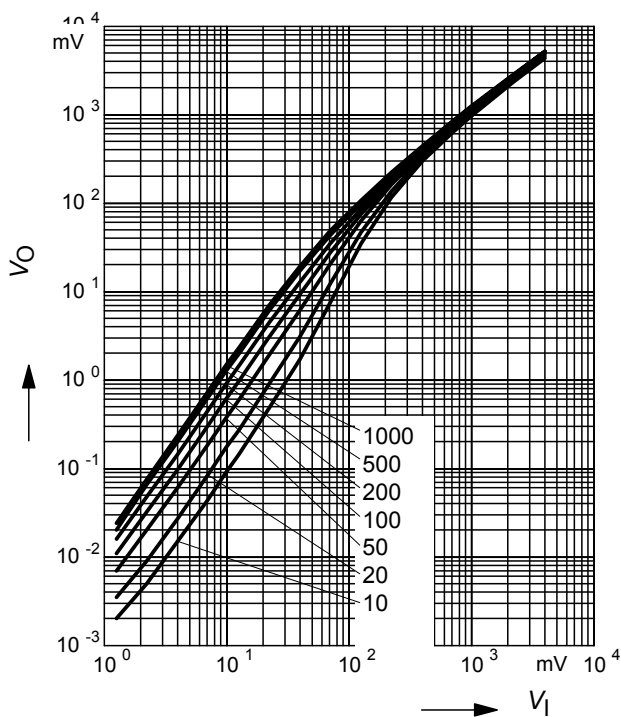
BAT62-07W



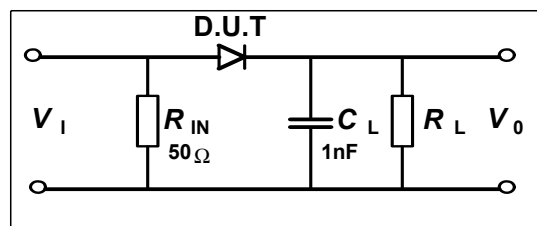
Rectifier voltage $V_{out} = f(V_{in})$

$f = 900\text{MHz}$

$R_L = \text{Parameter in } k\Omega$



Testcircuit



Package Outline



Foot Print



Marking Layout (Example)



Standard Packing

- Reel \varnothing 180 mm = 3.000 Pieces/Reel
- Reel \varnothing 180 mm = 8.000 Pieces/Reel (2 mm Pitch)
- Reel \varnothing 330 mm = 10.000 Pieces/Reel



Package Outline



Foot Print

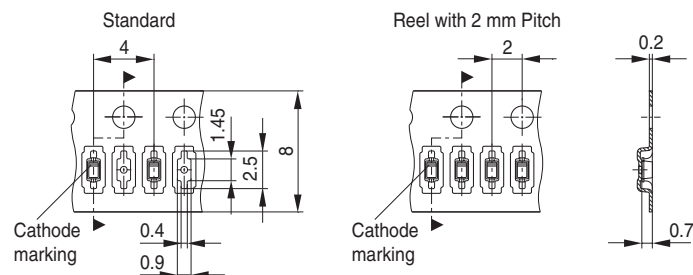


Marking Layout (Example)



Standard Packing

Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 180 mm = 8.000 Pieces/Reel (2 mm Pitch)
 Reel \varnothing 330 mm = 10.000 Pieces/Reel



Date Code marking for discrete packages with one digit (SCD80, SC79, SC75¹⁾) CES-Code

| Month | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 |
|-------|------|------|------|------|------|------|------|------|------|------|------|------|
| 01 | a | p | A | P | a | p | A | P | a | p | A | P |
| 02 | b | q | B | Q | b | q | B | Q | b | q | B | Q |
| 03 | c | r | C | R | c | r | C | R | c | r | C | R |
| 04 | d | s | D | S | d | s | D | S | d | s | D | S |
| 05 | e | t | E | T | e | t | E | T | e | t | E | T |
| 06 | f | u | F | U | f | u | F | U | f | u | F | U |
| 07 | g | v | G | V | g | v | G | V | g | v | G | V |
| 08 | h | x | H | X | h | x | H | X | h | x | H | X |
| 09 | j | y | J | Y | j | y | J | Y | j | y | J | Y |
| 10 | k | z | K | Z | k | z | K | Z | k | z | K | Z |
| 11 | l | 2 | L | 4 | l | 2 | L | 4 | l | 2 | L | 4 |
| 12 | n | 3 | N | 5 | n | 3 | N | 5 | n | 3 | N | 5 |

1) New Marking Layout for SC75, implemented at October 2005.

Package Outline



Foot Print



Marking Layout (Example)

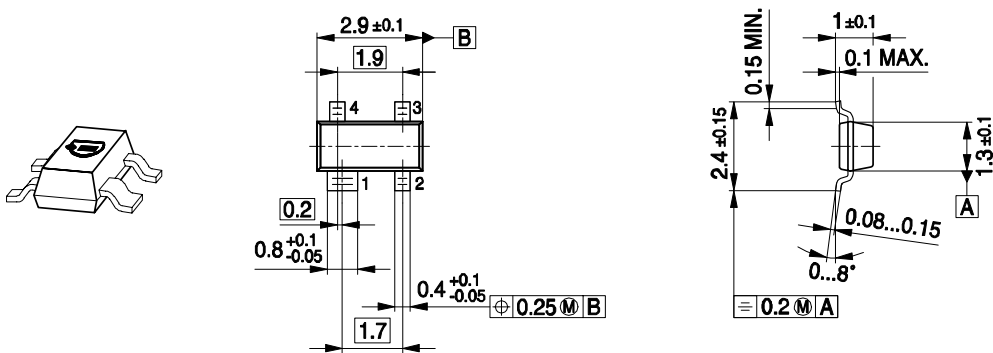


Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
 Reel ø330 mm = 10.000 Pieces/Reel



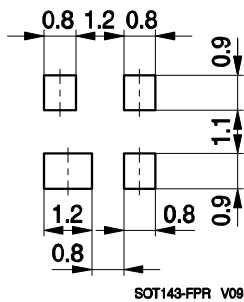
Package Outline



Note: Mold flash, protrusions or gate burrs of 0,2 mm max. per side are not included

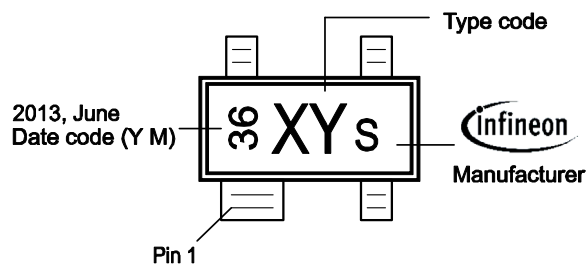
SOT143-PO V09

Foot Print



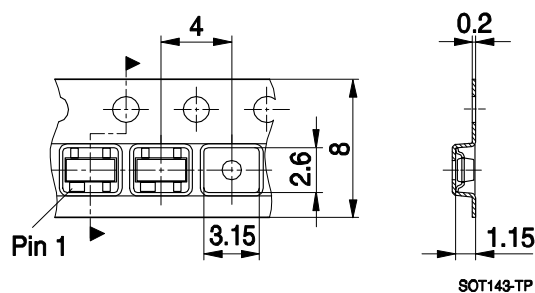
SOT143-FPR V09

Marking Layout (Example)



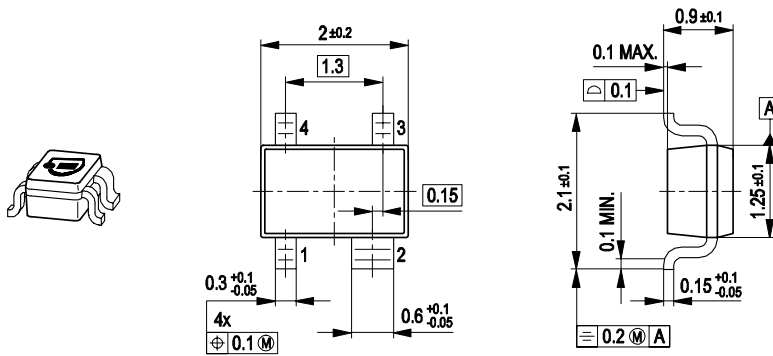
Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
 Reel ø330 mm = 10.000 Pieces/Reel

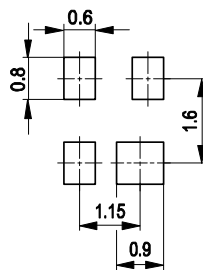


SOT143-TP

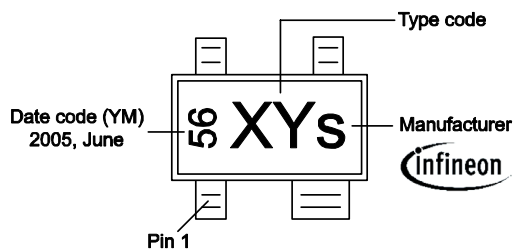
Package Outline



Foot Print

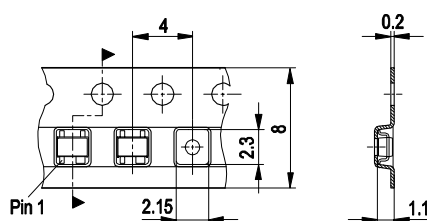


Marking Layout (Example)

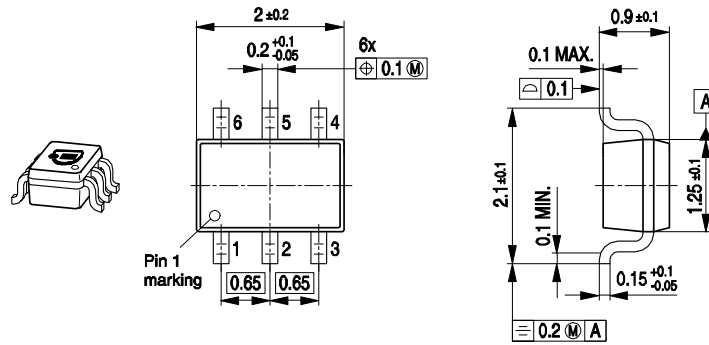


Standard Packing

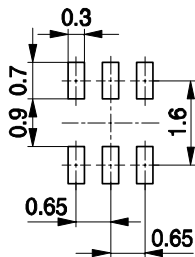
Reel ø180 mm = 3.000 Pieces/Reel
 Reel ø330 mm = 10.000 Pieces/Reel



Package Outline

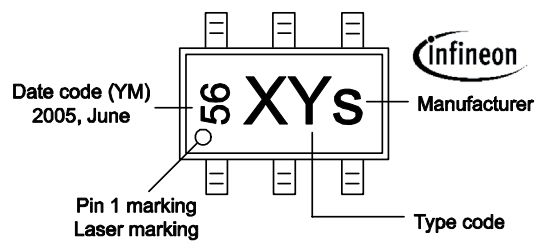


Foot Print



Marking Layout (Example)

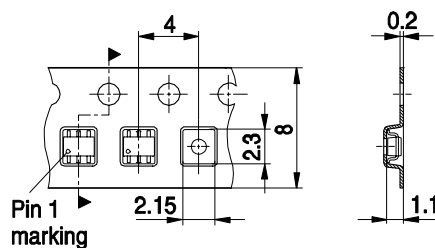
Small variations in positioning of Date code, Type code and Manufacture are possible.



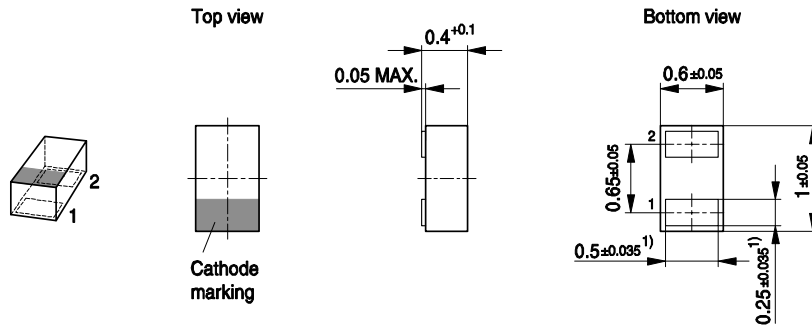
Standard Packing

Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 330 mm = 10.000 Pieces/Reel

For symmetric types no defined Pin 1 orientation in reel.



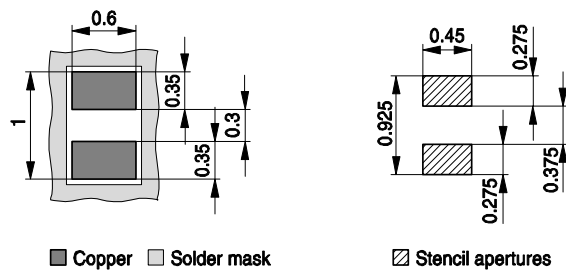
Package Outline



1) Dimension applies to plated terminal

Foot Print

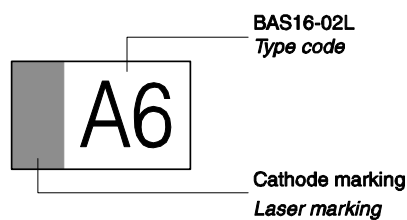
For board assembly information please refer to Infineon website "Packages"



■ Copper □ Solder mask

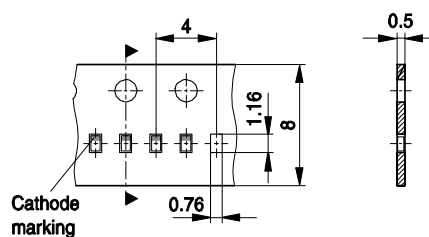
▨ Stencil apertures

Marking Layout (Example)

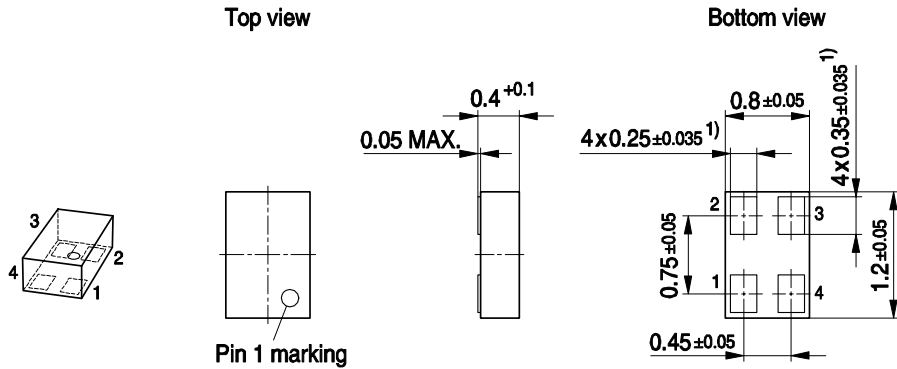


Standard Packing

Reel \varnothing 180 mm = 15.000 Pieces/Reel
 Reel \varnothing 330 mm = 50.000 Pieces/Reel (optional)



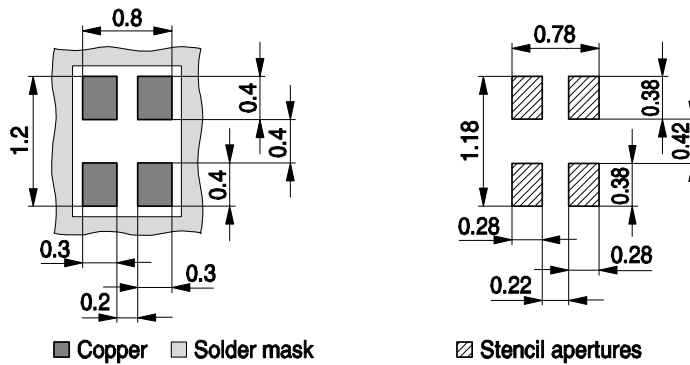
Package Outline



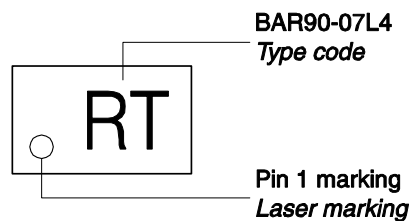
1) Dimension applies to plated terminal

Foot Print

For board assembly information please refer to Infineon website "Packages"

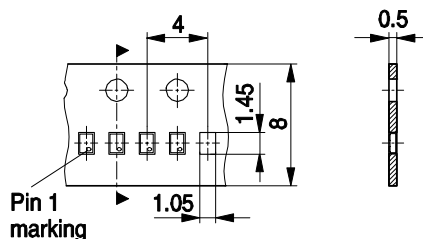


Marking Layout (Example)

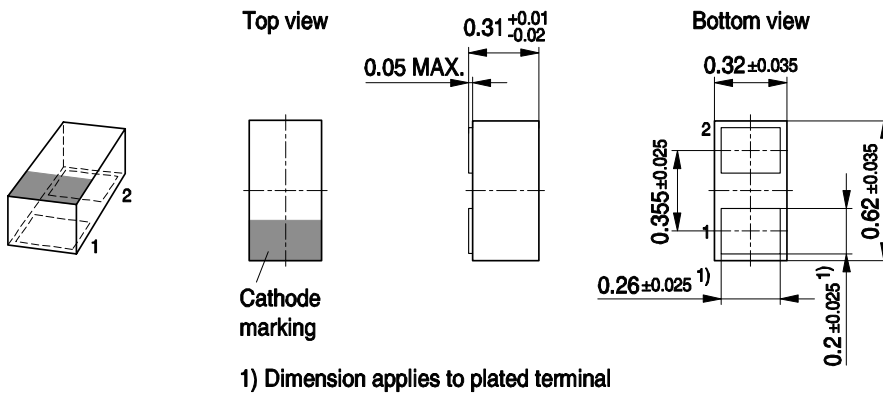


Standard Packing

Reel \varnothing 180 mm = 15.000 Pieces/Reel

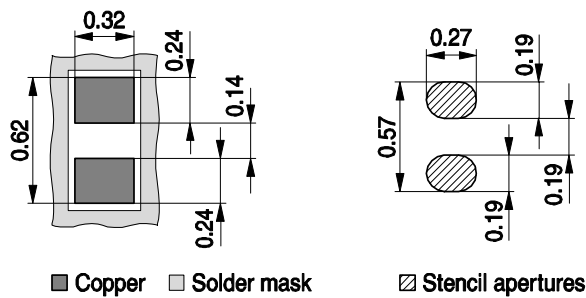


Package Outline

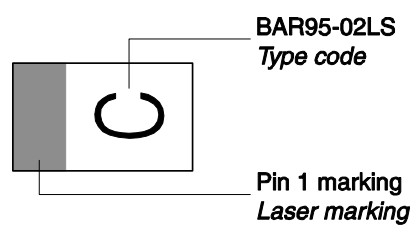


Foot Print

For board assembly information please refer to Infineon website "Packages"

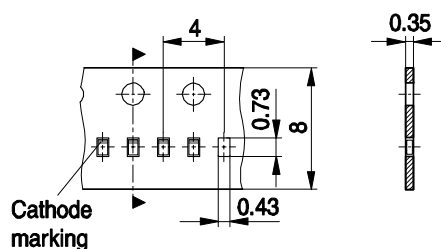


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel



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