# 3 kV RMS Dual Channel Digital Isolators

Data Sheet **ADuM1280/ADuM1281/ADuM1285/ADuM1286**

## FEATURES

- Up to 100 Mbps data rate (NRZ)
- Low propagation delay: 23 ns typical
- Low dynamic power consumption
- Bidirectional communication
- 3.3 V to 5 V level translation
- High temperature operation: 125°C
- High common-mode transient immunity: >25 kV/µs
- Default high output: ADuM1280/ADuM1281
- Default low output: ADuM1285/ADuM1286
- Narrow body, RoHS-compliant, 8-lead SOIC
- Safety and regulatory approvals
  - UL recognition: 3000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - VDE Certificate of Conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
- $V_{IORM}$ = 560 V peak
- Qualified for automotive applications

## APPLICATIONS

- General-purpose multichannel isolation
- Data converter isolation
- Industrial field bus isolation
- Hybrid electric vehicles, battery monitor, and motor drive

## FUNCTIONAL BLOCK DIAGRAMS

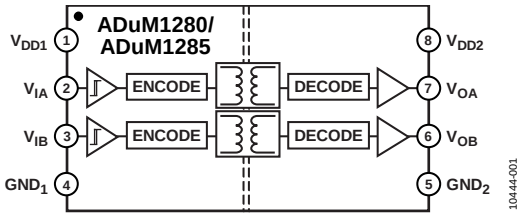


Figure 1. ADuM1280/ADuM1285

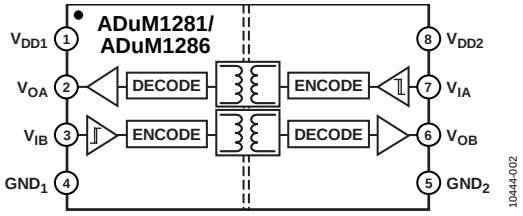


Figure 2. ADuM1281/ADuM1286

## GENERAL DESCRIPTION

The ADuM1280/ADuM1281/ADuM1285/ADuM1286[1] are dual-channel digital isolators based on the Analog Devices, Inc., iCoupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices and other integrated couplers.

With propagation delay at 23 ns, pulse width distortion is less than 2 ns for C grade. Channel-to-channel matching is tight at 5 ns for C grade. The two channels of the ADuM1280/ADuM1281/ADuM1285/ADuM1286 are independent isolation channels and are available in two channel configurations with three different data rates up to 100 Mbps (see the Ordering Guide). Industrial grade models operate with the supply voltage on either side ranging from 3.135 V to 5.5 V and the automotive grades operate from 3.135 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. Unlike other optocoupler alternatives, the ADuM1280/ADuM1281/ADuM1285/ADuM1286 isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions. When power is first applied or is not yet applied to the input side, the ADuM1280 and ADuM1281 have a default high output, and the ADuM1285 and ADuM1286 have a default low output.

For more information on safety and regulatory approvals, go to www.analog.com/icouplersafety.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

Rev. D
Document Feedback


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# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = $V_{DD2}$ = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 4.5 V ≤ $V_{DD2}$ ≤ 5.5 V, −40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Switching specifications are tested with $C_L$ = 15 pF and CMOS signal levels, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | A, WA Grades | | | B, WB Grades | | | C, WC Grades | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| SWITCHING SPECIFICATIONS | | | | | | | | | | | | |
| Pulse Width | PW | 1000 | | | 40 | | | 10 | | | ns | Within PWD limit |
| Data Rate | | | | 1 | | | 25 | | | 100 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | | | 50 | | | 35 | 20 | 23 | 29 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | 10 | | | 3 | | | 2 | ns | $\lvert t_{PLH} - t_{PHL} \rvert$ |
| Change vs. Temperature | | | 7 | | | 3 | | | 1.5 | | ps/°C | |
| Propagation Delay Skew | $t_{PSK}$ | | | 38 | | | 12 | | | 9 | ns | Between any two units at same operating conditions |
| Channel Matching[1] | | | | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 5 | | | 3 | | | 2 | ns | |
| Opposing-Direction | $t_{PSKOD}$ | | | 10 | | | 6 | | | 5 | ns | |
| Jitter | | | 2 | | | 2 | | | 1 | | ns | |

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-direction channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

**Table 2.**

| Parameter | Symbol | 1 Mbps—A, B, C, WA, WB, WC Grades | | | 25 Mbps—B, C, WB, WC Grades | | | 100 Mbps—C, WC Grades | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| SUPPLY CURRENT | | | | | | | | | | | | No load |
| ADuM1280/ADuM1285 | $I_{DD1}$ | | 1.1 | 1.6 | | 6.2 | 7.0 | | 20 | 25 | mA | |
| | $I_{DD2}$ | | 2.7 | 4.5 | | 4.8 | 7.0 | | 9.5 | 15 | mA | |
| ADuM1281/ADuM1286 | $I_{DD1}$ | | 2.1 | 2.6 | | 4.9 | 6.0 | | 15 | 19 | mA | |
| | $I_{DD2}$ | | 2.3 | 2.9 | | 4.7 | 6.4 | | 15.6 | 19 | mA | |

**Table 3. For All Models**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 0.7 $V_{DDx}$ | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.3 $V_{DDx}$ | V | |
| Logic High Output Voltages | $V_{OH}$ | $V_{DDx}$ − 0.1 | 5.0 | | V | $I_{Ox}$ = −20 μA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.4 | 4.8 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | μA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI(Q)}$ | | 0.54 | 0.8 | mA | |
| Quiescent Output Supply Current | $I_{DDO(Q)}$ | | 1.6 | 2.0 | mA | |
| Dynamic Input Supply Current | $I_{DDI(D)}$ | | 0.09 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO(D)}$ | | 0.04 | | mA/Mbps | |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Undervoltage Lockout | | | | | | |
| Positive $V_{DDx}$ Threshold | $V_{DDXUV+}$ | | 2.75 | | V | |
| Negative $V_{DDx}$ Threshold | $V_{DDXUV-}$ | | 2.65 | | V | |
| $V_{DDx}$ Hysteresis | $V_{DDXUVH}$ | | 0.1 | | V | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R/t_F$ | | 2.5 | | ns | 10% to 90% |
| Common-Mode Transient Immunity[1] | \|CM\| | 25 | 35 | | kV/µs | $V_{Ix} = V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Period | $t_r$ | | 1.6 | | µs | |

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DDx}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at $T_A$ = 25°C, $V_{DD1} = V_{DD2}$ = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.135 V ≤ $V_{DD1}$ ≤ 3.6 V, 3.135 V ≤ $V_{DD2}$ ≤ 3.6 V, −40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Switching specifications are tested with $C_L$ = 15 pF and CMOS signal levels, unless otherwise noted.

**Table 4.**

| | | A, WA Grades | | | B, WB Grades | | | C, WC Grades | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit | Test Conditions |
| SWITCHING SPECIFICATIONS | | | | | | | | | | | | |
| Pulse Width | PW | 1000 | | | 40 | | | 10 | | | ns | Within PWD limit |
| Data Rate | | | | 1 | | | 25 | | | 100 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | | | 50 | | | 35 | 22 | 27 | 35 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | 10 | | | 3 | | | 2.5 | ns | $\|t_{PLH} - t_{PHL}\|$ |
| Change vs. Temperature | | | 7 | | | 3 | | | 1.5 | | ps/°C | |
| Propagation Delay Skew | $t_{PSK}$ | | | 38 | | | 16 | | | 12 | ns | Between any two units at same operating conditions |
| Channel Matching[1] | | | | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 5 | | | 3 | | | 2.5 | ns | |
| Opposing-Direction | $t_{PSKOD}$ | | | 10 | | | 6 | | | 5 | ns | |
| Jitter | | | 2 | | | 2 | | | 1 | | ns | |

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-direction channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

**Table 5.**

| | | 1 Mbps—A, B, C, WA, WB, WC Grades | | | 25 Mbps—B, C, WB, WC Grades | | | 100 Mbps—C, WC Grades | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit | Test Conditions |
| SUPPLY CURRENT | | | | | | | | | | | | No load |
| ADuM1280/ADuM1285 | $I_{DD1}$ | | 0.75 | 1.4 | | 5.1 | 9.0 | | 17 | 23 | mA | |
| | $I_{DD2}$ | | 2.0 | 3.5 | | 2.7 | 4.6 | | 4.8 | 9 | mA | |
| ADuM1281/ADuM1286 | $I_{DD1}$ | | 1.6 | 2.1 | | 3.8 | 5.0 | | 11 | 15 | mA | |
| | $I_{DD2}$ | | 1.7 | 2.3 | | 3.9 | 6.2 | | 11 | 15 | mA | |

**Table 6. For All Models**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 0.7 $V_{DDx}$ | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.3 $V_{DDx}$ | V | |
| Logic High Output Voltages | $V_{OH}$ | $V_{DDx}$ − 0.1 | 3.0 | | V | $I_{Ox}$ = −20 μA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.4 | 2.8 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | μA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI(Q)}$ | | 0.4 | 0.6 | mA | |
| Quiescent Output Supply Current | $I_{DDO(Q)}$ | | 1.2 | 1.7 | mA | |
| Dynamic Input Supply Current | $I_{DDI(D)}$ | | 0.08 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO(D)}$ | | 0.015 | | mA/Mbps | |
| Undervoltage Lockout | | | | | | |
| Positive $V_{DDx}$ Threshold | $V_{DDxUV+}$ | | 2.75 | | V | |
| Negative $V_{DDx}$ Threshold | $V_{DDxUV-}$ | | 2.65 | | V | |
| $V_{DDx}$ Hysteresis | $V_{DDxUVH}$ | | 0.1 | | V | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R/t_F$ | | 3 | | ns | 10% to 90% |
| Common-Mode Transient Immunity[1] | \|CM\| | 25 | 35 | | kV/μs | $V_{Ix}$ = $V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Period | $t_r$ | | 1.6 | | μs | |

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o$ > 0.8 $V_{DDx}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = 5 V, $V_{DD2}$ = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 3.135 V ≤ $V_{DD2}$ ≤ 3.6 V; and −40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Switching specifications are tested with $C_L$ = 15 pF and CMOS signal levels unless otherwise noted.

**Table 7.**

| | | A, WA Grades | | | B, WB Grades | | | C, WC Grades | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit | Test Conditions |
| SWITCHING SPECIFICATIONS | | | | | | | | | | | | |
| Pulse Width | PW | 1000 | | | 40 | | | 10 | | | ns | Within PWD limit |
| Data Rate | | | | 1 | | | 25 | | | 100 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | | | 50 | | | 35 | 20 | 25 | 31 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | 10 | | | 3 | | | 2 | ns | $\|t_{PLH} - t_{PHL}\|$ |
| Change vs. Temperature | | | 7 | | | 3 | | | 1.5 | | ps/°C | |
| Propagation Delay Skew | $t_{PSK}$ | | | 38 | | | 16 | | | 12 | ns | Between any two units at same operating conditions |
| Channel Matching[1] | | | | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 5 | | | 3 | | | 2 | ns | |
| Opposing-Direction | $t_{PSKOD}$ | | | 10 | | | 6 | | | 5 | ns | |
| Jitter | | | 2 | | | 2 | | | 1 | | ns | |

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-direction channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

**Table 8.**

| Parameter | Symbol | 1 Mbps—A, B, C, WA, WB, WC Grades | | | 25 Mbps—B, C, WB, WC Grades | | | 100 Mbps—C, WC Grades | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| SUPPLY CURRENT | | | | | | | | | | | | No load |
| ADuM1280/ADuM1285 | $I_{DD1}$ | | 1.1 | 1.6 | | 6.2 | 7.0 | | 20 | 25 | mA | |
| | $I_{DD2}$ | | 2.0 | 3.5 | | 2.7 | 4.6 | | 4.8 | 9.0 | mA | |
| ADuM1281/ADuM1286 | $I_{DD1}$ | | 2.1 | 2.6 | | 4.9 | 6.0 | | 15 | 19 | mA | |
| | $I_{DD2}$ | | 1.7 | 2.3 | | 3.9 | 6.2 | | 11 | 15 | mA | |

**Table 9. For All Models**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 0.7 $V_{DDx}$ | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.3 $V_{DDx}$ | V | |
| Logic High Output Voltages | $V_{OH}$ | $V_{DDx}$ − 0.1 | $V_{DDx}$ | | V | $I_{Ox}$ = −20 µA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.4 | $V_{DDx}$ − 0.2 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 µA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | µA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI(Q)}$ | | 0.54 | 0.75 | mA | |
| Quiescent Output Supply Current | $I_{DDO(Q)}$ | | 1.2 | 2.0 | mA | |
| Dynamic Input Supply Current | $I_{DDI(D)}$ | | 0.09 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO(D)}$ | | 0.02 | | mA/Mbps | |
| Undervoltage Lockout | | | | | | |
| Positive $V_{DDX}$ Threshold | $V_{DDxUV+}$ | | 2.75 | | V | |
| Negative $V_{DDX}$ Threshold | $V_{DDxUV-}$ | | 2.65 | | V | |
| $V_{DDX}$ Hysteresis | $V_{DDxUVH}$ | | 0.1 | | V | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R/t_F$ | | 2.5 | | ns | 10% to 90% |
| Common-Mode Transient Immunity[1] | \|CM\| | 25 | 35 | | kV/µs | $V_{Ix}$ = $V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Period | $t_r$ | | 1.6 | | µs | |

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o$ > 0.8 $V_{DDx}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = 3.3 V, $V_{DD2}$ = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.135 V ≤ $V_{DD1}$ ≤ 3.6 V, 4.5 V ≤ $V_{DD2}$ ≤ 5.5 V; and −40°C ≤ $T_A$ ≤ 125°C; unless otherwise noted. Switching specifications are tested with $C_L$ = 15 pF and CMOS signal levels, unless otherwise noted.

**Table 10.**

| Parameter | Symbol | A, WA Grades | | | B, WB Grades | | | C, WC Grades | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| SWITCHING SPECIFICATIONS | | | | | | | | | | | | |
| Pulse Width | PW | 1000 | | | 40 | | | 10 | | | ns | Within PWD limit |
| Data Rate | | | | 1 | | | 25 | | | 100 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | | | 50 | | | 35 | 20 | 27 | 33 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | 10 | | | 3 | | | 2.5 | ns | $\lvert t_{PLH} - t_{PHL} \rvert$ |
| Change vs. Temperature | | | 7 | | | 3 | | | 1.5 | | ps/°C | |
| Propagation Delay Skew | $t_{PSK}$ | | | 38 | | | 16 | | | 12 | ns | Between any two units at same operating conditions |
| Channel Matching[1] | | | | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 5 | | | 3 | | | 2.5 | ns | |
| Opposing-Direction | $t_{PSKOD}$ | | | 10 | | | 6 | | | 5 | ns | |
| Jitter | | | 2 | | | 2 | | | 1 | | ns | |

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-direction channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

**Table 11.**

| Parameter | Symbol | 1 Mbps—A, B, C, WA, WB, WC Grades | | | 25 Mbps—B, C, WB, WC Grades | | | 100 Mbps—C, WC Grades | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| SUPPLY CURRENT | | | | | | | | | | | | No load |
| ADuM1280/ADuM1285 | $I_{DD1}$ | | 0.75 | 1.4 | | 5.1 | 9.0 | | 17 | 23 | mA | |
| | $I_{DD2}$ | | 2.7 | 4.5 | | 4.8 | 7.0 | | 9.5 | 15 | mA | |
| ADuM1281/ADuM1286 | $I_{DD1}$ | | 1.6 | 2.1 | | 3.8 | 5.0 | | 11 | 15 | mA | |
| | $I_{DD2}$ | | 1.7 | 2.3 | | 3.9 | 6.2 | | 11 | 15 | mA | |

**Table 12. For All Models**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 0.7 $V_{DDx}$ | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.3 $V_{DDx}$ | V | |
| Logic High Output Voltages | $V_{OH}$ | $V_{DDx}$ − 0.1 | $V_{DDx}$ | | V | $I_{Ox}$ = −20 μA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.4 | $V_{DDx}$ − 0.2 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | μA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI(Q)}$ | | 0.4 | 0.75 | mA | |
| Quiescent Output Supply Current | $I_{DDO(Q)}$ | | 1.6 | 2.0 | mA | |
| Dynamic Input Supply Current | $I_{DDI(D)}$ | | 0.08 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO(D)}$ | | 0.03 | | mA/Mbps | |
| Undervoltage Lockout | | | | | | |
| Positive $V_{DDx}$ Threshold | $V_{DDxUV+}$ | | 2.75 | | V | |
| Negative $V_{DDx}$ Threshold | $V_{DDxUV-}$ | | 2.65 | | V | |
| $V_{DDx}$ Hysteresis | $V_{DDxUVH}$ | | 0.1 | | V | |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R/t_F$ | | 2.5 | | ns | 10% to 90% |
| Common-Mode Transient Immunity[1] | \|CM\| | 25 | 35 | | kV/µs | $V_{Ix} = V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Period | $t_r$ | | 1.6 | | µs | |

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o > 0.8\ V_{DDx}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## PACKAGE CHARACTERISTICS

**Table 13.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Resistance (Input-to-Output)[1] | $R_{I-O}$ | | $10^{13}$ | | Ω | |
| Capacitance (Input-to-Output)[1] | $C_{I-O}$ | | 2 | | pF | f = 1 MHz |
| Input Capacitance[2] | $C_I$ | | 4.0 | | pF | |
| IC Junction-to-Ambient Thermal Resistance | $\theta_{JA}$ | | 85 | | °C/W | Thermocouple located at center of package underside |

[1] The device is considered a 2-terminal device; Pin 1 through Pin 4 are shorted together and Pin 5 through Pin 8 are shorted together.
[2] Input capacitance is from any input data pin to ground.

## REGULATORY INFORMATION

The ADuM1280/ADuM1281/ADuM1285/ADuM1286 are approved by the organizations listed in Table 14. See Table 18 and Table 19 for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

**Table 14.**

| UL | CSA | VDE |
|---|---|---|
| Recognized Under UL 1577 Component Recognition Program[1] | Approved under CSA Component Acceptance Notice 5A | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2] |
| Single Protection, 3000 V rms Isolation Voltage | Basic insulation per CSA 60950-1-03 and IEC 60950-1, 390 V rms (550 V peak) maximum working voltage | Reinforced insulation, 560 V peak |
| File E214100 | File 205078 | File 2471900-4880-0001 |

[1] In accordance with UL 1577, each ADuM1280/ADuM1281/ADuM1285/ADuM1286 is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 second (current leakage detection limit = 6 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM1280/ADuM1281/ADuM1285/ADuM1286 is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marked on the component designates DIN V VDE V 0884-10 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

**Table 15.**

| Parameter | Symbol | Value | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| Rated Dielectric Insulation Voltage | | 3000 | V rms | 1-minute duration |
| Clearance in the Plane of the PCB | $CL_{PCB}$ | 4.5 | mm min | Measured from input terminals to output terminals, shortest line of sight distance through air in the plane of the PCB |
| Minimum External Air Gap (Clearance) | L(I01) | 4.0 | mm min | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 4.0 | mm min | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.017 | mm min | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

## DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation within the safety limit data only. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marked on packages denotes DIN V VDE V 0884-10 approval.

**Table 16.**

| Description | Test Conditions/Comments | Symbol | Characteristic | Unit |
|---|---|---|---|---|
| Installation Classification per DIN VDE 0110 | | | | |
| For Rated Mains Voltage ≤ 150 V rms | | | I to IV | |
| For Rated Mains Voltage ≤ 300 V rms | | | I to III | |
| For Rated Mains Voltage ≤ 400 V rms | | | I to II | |
| Climatic Classification | | | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum Working Insulation Voltage | | $V_{IORM}$ | 560 | $V_{PEAK}$ |
| Input-to-Output Test Voltage, Method B1 | $V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 1050 | $V_{PEAK}$ |
| Input-to-Output Test Voltage, Method A | | | | |
| After Environmental Tests Subgroup 1 | $V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini}$=60 sec, $t_m$ = 10 sec, partial discharge < 5 pC | $V_{pd(m)}$ | 840 | $V_{PEAK}$ |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini}$ = 60 sec, $t_m$ = 10 sec, partial discharge < 5 pC | $V_{pd(m)}$ | 672 | $V_{PEAK}$ |
| Highest Allowable Overvoltage | | $V_{IOTM}$ | 4000 | $V_{PEAK}$ |
| Withstand Isolation Voltage | 1 minute withstand rating | $V_{ISO}$ | 3000 | $V_{RMS}$ |
| Surge Isolation Voltage | $V_{PEAK}$ = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time | $V_{IOSM}$ | 6000 | $V_{PEAK}$ |
| Safety Limiting Values | Maximum value allowed in the event of a failure (see Figure 3) | | | |
| Case Temperature | | $T_S$ | 150 | °C |
| Total $I_{DD1}$ and $I_{DD2}$ Safety Limiting Current | | $I_S$ | 290 | mA |
| Insulation Resistance at $T_S$ | $V_{IO}$ = 500 V | $R_S$ | $>10^9$ | Ω |

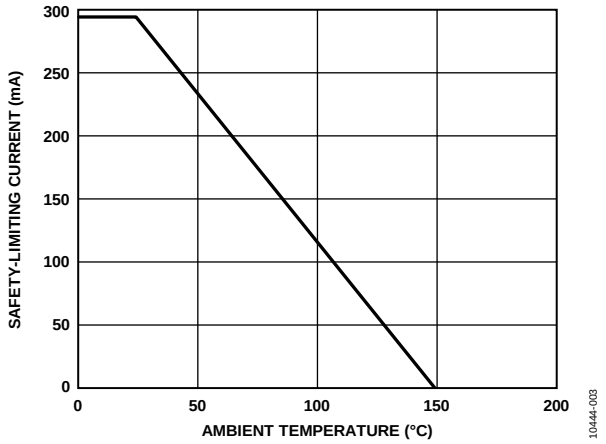



*Figure 3. Thermal Derating Curve at $V_{DDx}$ = 5 V, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10*

## RECOMMENDED OPERATING CONDITIONS

**Table 17.**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | −40 | +125 | °C |
| Supply Voltages[1] | $V_{DD1}$, $V_{DD2}$ | | | |
| A, B, and C Grades | | 3.135 | 5.5 | V |
| WA, WB, and WC Grades | | 3.135 | 5.5 | V |
| Input Signal Rise and Fall Times | | | 1.0 | ms |

[1] See the DC Correctness and Magnetic Field Immunity section.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 18.**

| Parameter | Rating |
|---|---|
| Storage Temperature ($T_{ST}$) Range | −65°C to +150°C |
| Ambient Operating Temperature ($T_A$) Range | −40°C to +125°C |
| Supply Voltages ($V_{DD1}$, $V_{DD2}$) | −0.5 V to +7.0 V |
| Input Voltages ($V_{IA}$, $V_{IB}$) | −0.5 V to $V_{DDI}$ + 0.5 V |
| Output Voltages ($V_{OA}$, $V_{OB}$) | −0.5 V to $V_{DD2}$ + 0.5 V |
| Average Output Current per Pin[1] | |
| Side 1 ($I_{O1}$) | −10 mA to +10 mA |
| Side 2 ($I_{O2}$) | −10 mA to +10 mA |
| Common-Mode Transients[2] | −100 kV/µs to +100 kV/µs |

[1] See Figure 3 for maximum rated current values for various temperatures.
[2] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Table 19. Maximum Continuous Working Voltage[1]**

| Parameter | Max | Unit | Constraint |
|---|---|---|---|
| AC Voltage, Bipolar Waveform | 565 | V peak | 50-year minimum lifetime |
| AC Voltage, Unipolar Waveform | | | |
| Basic Insulation | 1131 | V peak | Maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 560 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |
| DC Voltage | | | |
| Basic Insulation | 1131 | V peak | Maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 560 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

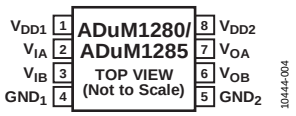



*Figure 4. ADuM1280/ADuM1285 Pin Configuration*

**Table 20. ADuM1280/ADuM1285 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1 (3.135 V to 5.5 V). |
| 2 | $V_{IA}$ | Logic Input A. |
| 3 | $V_{IB}$ | Logic Input B. |
| 4 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. |
| 5 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. |
| 6 | $V_{OB}$ | Logic Output B. |
| 7 | $V_{OA}$ | Logic Output A. |
| 8 | $V_{DD2}$ | Supply Voltage for Isolator Side 2 (3.135 V to 5.5 V). |

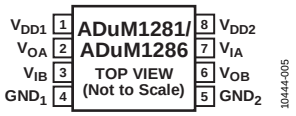



*Figure 5. ADuM1281/ADuM1286 Pin Configuration*

**Table 21. ADuM1281/ADuM1286 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1 (3.135 V to 5.5 V). |
| 2 | $V_{OA}$ | Logic Output A. |
| 3 | $V_{IB}$ | Logic Input B. |
| 4 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. |
| 5 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. |
| 6 | $V_{OB}$ | Logic Output B. |
| 7 | $V_{IA}$ | Logic Input A. |
| 8 | $V_{DD2}$ | Supply Voltage for Isolator Side 2 (3.135 V to 5.5 V). |

For specific layout guidelines, refer to the AN-1109 Application Note, *Recommendations for Control of Radiated Emissions with i*Coupler *Devices*.

**Table 22. ADuM1280 Truth Table (Positive Logic)**

| $V_{IA}$ Input | $V_{IB}$ Input | $V_{DD1}$ State | $V_{DD2}$ State | $V_{OA}$ Output | $V_{OB}$ Output | Notes |
|---|---|---|---|---|---|---|
| H | H | Powered | Powered | H | H | |
| L | L | Powered | Powered | L | L | |
| H | L | Powered | Powered | H | L | |
| L | H | Powered | Powered | L | H | |
| L | L | Unpowered | Powered | H | H | Outputs return to the input state within 1.6 µs of $V_{DDI}$ power restoration. |
| X | X | Powered | Unpowered | Indeterminate | Indeterminate | Outputs return to the input state within 1.6 µs of $V_{DDO}$ power restoration. |

**Table 23. ADuM1281 Truth Table (Positive Logic)**

| $V_{IA}$ Input | $V_{IB}$ Input | $V_{DD1}$ State | $V_{DD2}$ State | $V_{OA}$ Output | $V_{OB}$ Output | Notes |
|---|---|---|---|---|---|---|
| H | H | Powered | Powered | H | H | |
| L | L | Powered | Powered | L | L | |
| H | L | Powered | Powered | H | L | |
| L | H | Powered | Powered | L | H | |
| X | L | Unpowered | Powered | Indeterminate | H | Outputs return to the input state within 1.6 µs of $V_{DD1}$ power restoration. |
| L | X | Powered | Unpowered | H | Indeterminate | Outputs return to the input state within 1.6 µs of $V_{DDO}$ power restoration. |

**Table 24. ADuM1285 Truth Table (Positive Logic)**

| $V_{IA}$ Input | $V_{IB}$ Input | $V_{DD1}$ State | $V_{DD2}$ State | $V_{OA}$ Output | $V_{OB}$ Output | Notes |
|---|---|---|---|---|---|---|
| H | H | Powered | Powered | H | H | |
| L | L | Powered | Powered | L | L | |
| H | L | Powered | Powered | H | L | |
| L | H | Powered | Powered | L | H | |
| L | L | Unpowered | Powered | L | L | Outputs return to the input state within 1.6 µs of $V_{DDI}$ power restoration. |
| X | X | Powered | Unpowered | Indeterminate | Indeterminate | Outputs return to the input state within 1.6 µs of $V_{DDO}$ power restoration. |

**Table 25. ADuM1286 Truth Table (Positive Logic)**

| $V_{IA}$ Input | $V_{IB}$ Input | $V_{DD1}$ State | $V_{DD2}$ State | $V_{OA}$ Output | $V_{OB}$ Output | Notes |
|---|---|---|---|---|---|---|
| H | H | Powered | Powered | H | H | |
| L | L | Powered | Powered | L | L | |
| H | L | Powered | Powered | H | L | |
| L | H | Powered | Powered | L | H | |
| X | L | Unpowered | Powered | Indeterminate | L | Outputs return to the input state within 1.6 µs of $V_{DD1}$ power restoration. |
| L | X | Powered | Unpowered | L | Indeterminate | Outputs return to the input state within 1.6 µs of $V_{DDO}$ power restoration. |

# TYPICAL PERFORMANCE CHARACTERISTICS

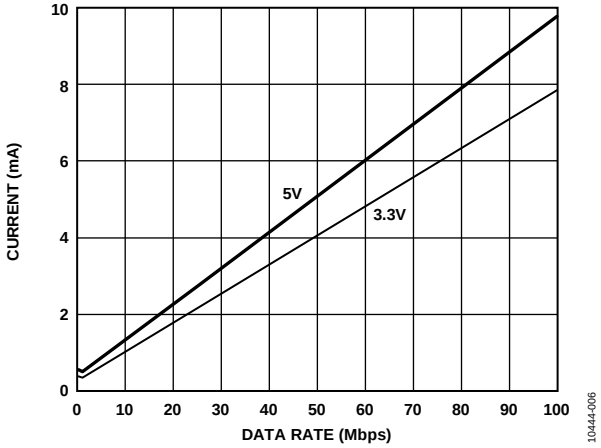



*Figure 6. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3.3 V Operation*

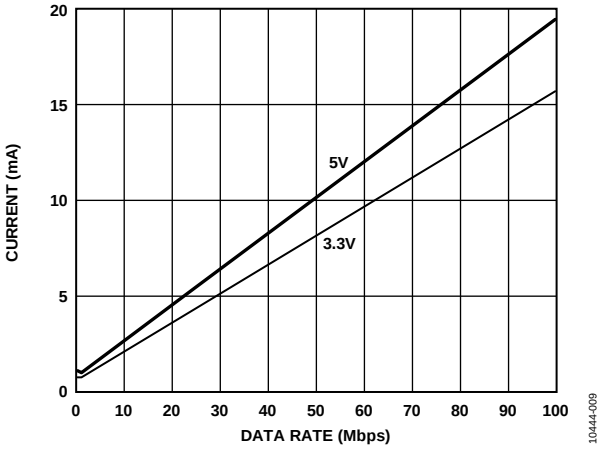



*Figure 9. Typical ADuM1280 or ADuM1285 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation*

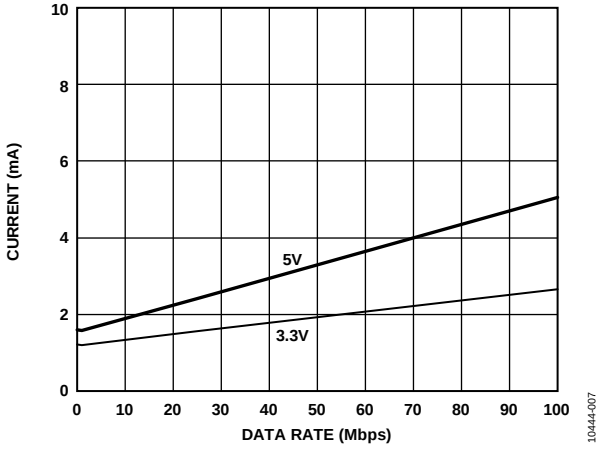



*Figure 7. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)*

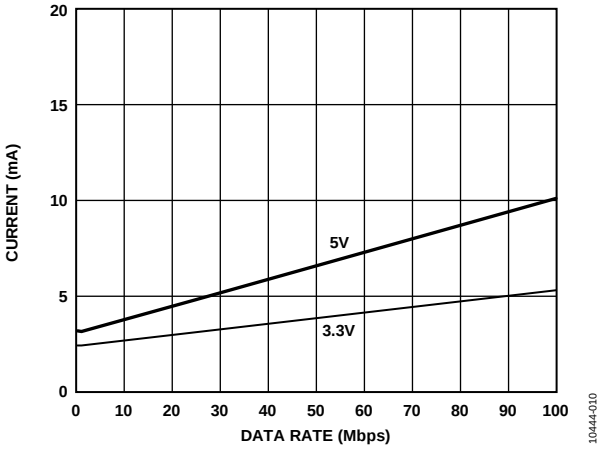



*Figure 10. Typical ADuM1280 or ADuM1285 $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation*

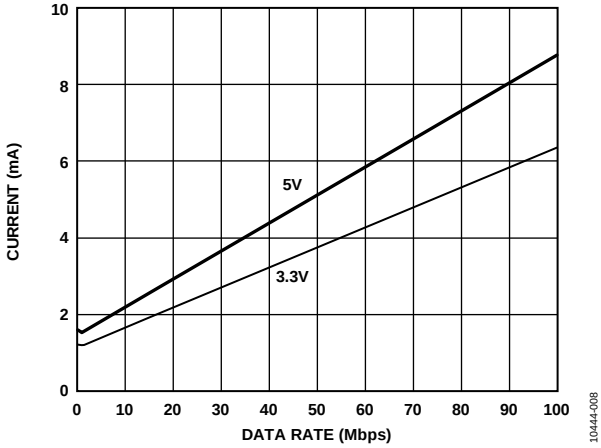



*Figure 8. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3.3 V Operation (15 pF Output Load)*

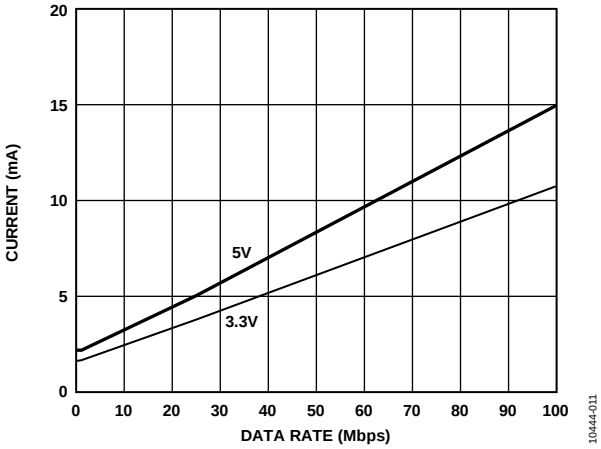



*Figure 11. Typical ADuM1281 or ADuM1286 $V_{DD1}$ or $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation*

# APPLICATIONS INFORMATION

## PRINTED CIRCUIT BOARD LAYOUT

The ADuM1280/ADuM1281/ADuM1285/ADuM1286 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at both input and output supply pins $V_{DD1}$ and $V_{DD2}$ (see Figure 12). The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

The ADuM1280/ADuM1281/ADuM1285/ADuM1286 can readily meet CISPR 22 Class A (and FCC Class A) emissions standards, as well as the more stringent CISPR 22 Class B (and FCC Class B) standards in an unshielded environment, with proper PCB design choices. Refer to the AN-1109 Applicaton Note, *Recommendations for Control of Radiated Emissions with iCoupler Devices* for PCB-related EMI mitigation techniques, including board layout and stack-up issues.

## PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time of a low-to-high transition.

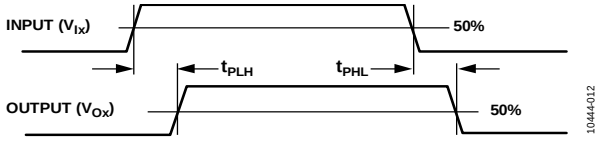



*Figure 12. Propagation Delay Parameters*

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM1280/ADuM1281/ADuM1285/ADuM1286 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM1280/ADuM1281/ADuM1285/ADuM1286 components operating under the same conditions.

## DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is, therefore, either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than ~1.6 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output.

If the decoder receives no pulses for more than about 6.4 µs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default low state by the watchdog timer circuit.

The limitation on the device's magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines such conditions. The ADuM1280 is examined in a 3.3 V operating condition because it represents the most susceptible mode of operation of this product.

The pulses at the transformer output have an amplitude greater than 1.5 V. The decoder has a sensing threshold of about 1.0 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2; n = 1, 2, \ldots, N$$

where:

$\beta$ is the magnetic flux density.
$r_n$ is the radius of the $n^{th}$ turn in the receiving coil.
$N$ is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM1280 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 13.

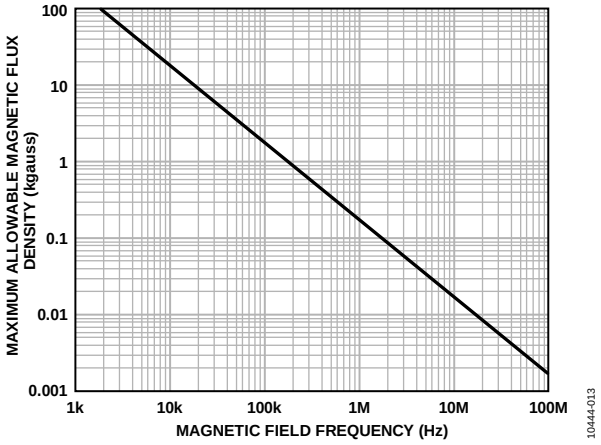



*Figure 13. Maximum Allowable External Magnetic Flux Density*

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.08 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs, with the worst-case polarity, during a transmitted pulse, it would reduce the received pulse from >1.0 V to 0.75 V. This is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM1280 transformers. Figure 14 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADuM1280 is very insensitive to external fields. Only extremely large, high frequency currents, very close to the component could potentially be a concern. For the 1 MHz example noted, place a 0.2 kA current 5 mm away from the ADuM1280 to affect component operation.

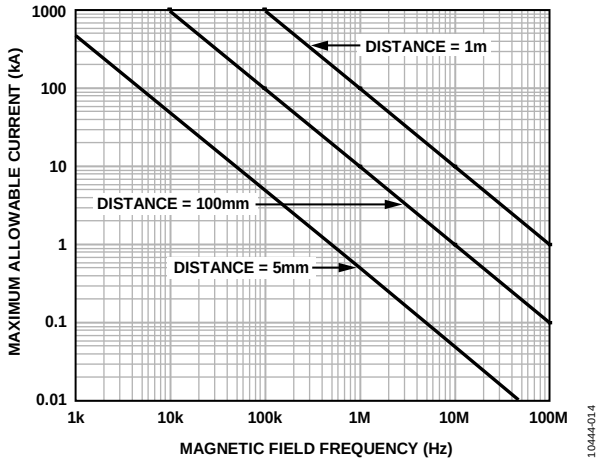



*Figure 14. Maximum Allowable Current for Various Current to ADuM1280 Spacings*

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Take care to avoid PCB structures that form loops.

## POWER CONSUMPTION

The supply current at a given channel of the ADuM1280/ADuM1281/ADuM1285/ADuM1286 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \qquad f \leq 0.5\,f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \qquad f > 0.5\,f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \qquad f \leq 0.5\,f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \qquad f > 0.5\,f_r$$

where:
$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
$C_L$ is the output load capacitance (pF).
$V_{DDO}$ is the output supply voltage (V).
$f$ is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.
$f_r$ is the input stage refresh rate (Mbps) = $1/t_r$ (µs).
$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total $V_{DD1}$ and $V_{DD2}$ supply current, the supply currents for each input and output channel corresponding to $V_{DD1}$ and $V_{DD2}$ are calculated and totaled. Figure 6 and Figure 7 show per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 shows the per-channel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 11 show the total $V_{DD1}$ and $V_{DD2}$ supply current as a function of data rate for ADuM1280/ADuM1281 channel configurations.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM1280/ADuM1281/ADuM1285/ADuM1286.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 19 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM1280/ADuM1281/ADuM1285/ADuM1286 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 19 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage case. Any cross-insulation voltage waveform that does not conform to Figure 16 or Figure 17 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 19.

Note that the voltage presented in Figure 17 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

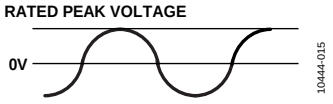



*Figure 15. Bipolar AC Waveform*

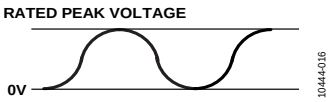



*Figure 16. Unipolar AC Waveform*

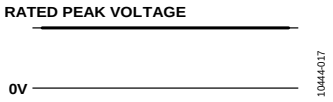
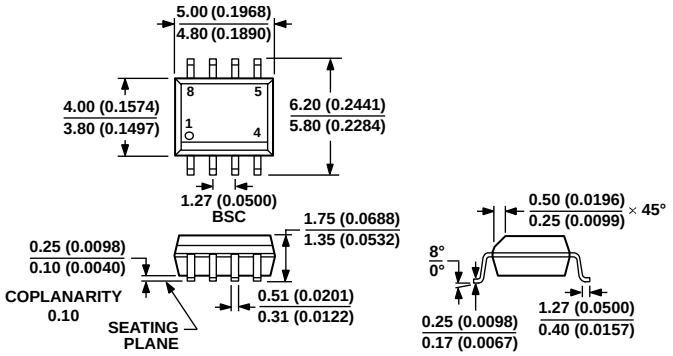



*Figure 17. DC Waveform*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

*Figure 18. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body (R-8)*
*Dimensions shown in millimeters (inches)*

## ORDERING GUIDE

| Model[1, 2, 3] | No. of Inputs, $V_{DD1}$ Side | No. of Inputs, $V_{DD2}$ Side | Max Data Rate | Max Prop Delay, 5 V | Output Default State | Temperature Range | Package Description | Package Option |
|---|---|---|---|---|---|---|---|---|
| ADuM1280ARZ | 2 | 0 | 1 Mbps | 50 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1280WARZ | 2 | 0 | 1 Mbps | 50 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1280BRZ | 2 | 0 | 25 Mbps | 35 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1280WBRZ | 2 | 0 | 25 Mbps | 35 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1280CRZ | 2 | 0 | 100 Mbps | 24 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1280WCRZ | 2 | 0 | 100 Mbps | 24 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1281ARZ | 1 | 1 | 1 Mbps | 50 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1281WARZ | 1 | 1 | 1 Mbps | 50 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1281BRZ | 1 | 1 | 25 Mbps | 35 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1281WBRZ | 1 | 1 | 25 Mbps | 35 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1281CRZ | 1 | 1 | 100 Mbps | 24 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1281WCRZ | 1 | 1 | 100 Mbps | 24 | High | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1285ARZ | 2 | 0 | 1 Mbps | 50 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1285WARZ | 2 | 0 | 1 Mbps | 50 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1285BRZ | 2 | 0 | 25 Mbps | 35 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1285WBRZ | 2 | 0 | 25 Mbps | 35 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1285CRZ | 2 | 0 | 100 Mbps | 24 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1285WCRZ | 2 | 0 | 100 Mbps | 24 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1286ARZ | 1 | 1 | 1 Mbps | 50 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1286WARZ | 1 | 1 | 1 Mbps | 50 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1286BRZ | 1 | 1 | 25 Mbps | 35 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1286WBRZ | 1 | 1 | 25 Mbps | 35 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1286CRZ | 1 | 1 | 100 Mbps | 24 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |
| ADuM1286WCRZ | 1 | 1 | 100 Mbps | 24 | Low | −40°C to +125°C | 8-Lead SOIC_N | R-8 |

[1] Z = RoHS Compliant Part.
[2] Tape and reel are available. The addition of an "-RL7" suffix designates a 7" (1,000 units) tape and reel option.
[3] W = Qualified for Automotive Applications.

## AUTOMOTIVE PRODUCTS

The ADuM1280W, ADuM1281W, ADuM1285W, and ADuM1286W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.


D10444-0-2/17(D)

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADUM1286ARZ ADUM1286BRZ-RL7 ADUM1286CRZ ADUM1286BRZ ADUM1286ARZ-RL7 ADUM1286CRZ-RL7 ADUM1286WARZ ADUM1286WCRZ ADUM1286WARZ-RL7 ADUM1286WCRZ-RL7 ADUM1286WBRZ-RL7 ADUM1286WBRZ