Low Cost, 270 MHz Differential Receiver Amplifier

Data Sheet

AD8130ACHIPS

FEATURES

High speed
- **270 MHz, 1090 V/µs at G = +1**

High CMRR
- **90 dB (minimum), dc to 100 kHz**
- **80 dB (minimum) at 2 MHz**
- **70 dB (typical) at 10 MHz**

High input impedance: 6 MΩ differential
Input common-mode range: ±10.5 V
Low noise: 12.5 nV/√Hz
Low distortion, 1 V p-p at 5 MHz
- **−79 dBc worst harmonic at 5 MHz**

User adjustable gain
- **No external components for G = +1**

Power supply range: ±2.25 to ±12.6 V
Power-down

APPLICATIONS

High speed differential line receivers
Differential-to-single-ended converters
High speed instrumentation amps
Level shifting

FUNCTION BLOCK DIAGRAM

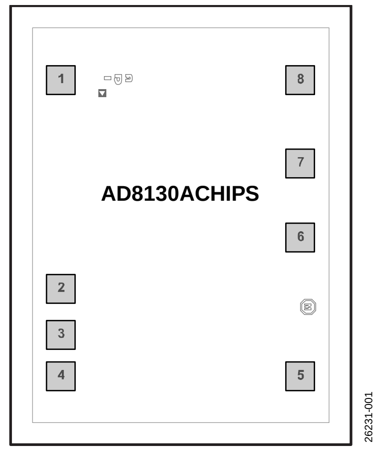

Figure 1.

GENERAL DESCRIPTION

The AD8130ACHIPS is designed as a receiver for the transmission of high speed signals over twisted pair cables to work with the AD8131 or AD8132 driver. The AD8130ACHIPS can be used for analog or digital video signals and for high speed data transmission.

The AD8130ACHIPS is a differential to single-ended amplifier with an extremely high common-mode rejection ratio (CMRR) at high frequency. Therefore, this device can also be effectively used as a high speed instrumentation amp or for converting differential signals to single-ended signals.

The AD8130ACHIPS is stable at a gain of 1 and can be used for applications where lower gains are required. The AD8130ACHIPS has a very high input impedance on both inputs, regardless of the gain setting.

The AD8130ACHIPS has excellent common-mode rejection (70 dB at 10 MHz), allowing the use of low cost, unshielded twisted pair cables without fear of corruption by external noise sources or crosstalk. The AD8130ACHIPS has a wide power supply range from a single +5 V to ±12 V, allowing wide common-mode and differential mode voltage ranges while maintaining signal integrity. The wide common-mode voltage range enables the driver and receiver pair to operate without isolation transformers in many systems where the ground potential difference between drive and receive locations is many volts. The AD8130ACHIPS has considerable cost and performance improvements over op amps and other multiamplifier receiving solutions.

Additional application and technical information can be found in the AD8130 data sheet.

Rev. 0
Document Feedback

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Technical Support
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REVISION HISTORY

6/2021—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

G = +1, T_A = 25°C, $+V_S$ = 5 V, $−V_S$ = 0 V, REF = 2.5 V, $\overline{PD} \geq V_{IH}$, load resistance ($R_{LOAD}$) = 1 kΩ, load capacitance (C_L) = 2 pF, unless otherwise specified. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	Output voltage (V_{OUT}) ≤ 0.3 V p-p	220	250		MHz
	V_{OUT} = 1 V p-p	180	205		MHz
Slew Rate	V_{OUT} = 2 V p-p, 25% to 75%	810	930		V/µs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		20		ns
Rise and Fall Times	V_{OUT} ≤ 1 V p-p, 10% to 90%		1.5		ns
Output Overdrive Recovery			30		ns
NOISE/DISTORTION					
Second Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−72		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−65		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−60		dBc
	V_{OUT} = 2 V p-p, 10 MHz		−68		dBc
Third Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−79		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−71		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−62		dBc
	V_{OUT} = 2 V p-p, 10 MHz		−68		dBc
Intermodulation Distortion (IMD)	V_{OUT} = 2 V p-p, 10 MHz		−70		dBc
Output Third-Order Intercept (IP3)	V_{OUT} = 2 V p-p, 10 MHz		26		dBm
Input Voltage Noise (Referred to Input (RTI))	f ≥ 10 kHz		12.3		nV/√Hz
Input Current Noise (+IN, −IN)	f ≥ 100 kHz		1		pA/√Hz
Input Current Noise (REF, FB)	f ≥ 100 kHz		1.4		pA/√Hz
Differential Gain Error	G = +2, NTSC 100 IRE, R_{LOAD} ≥ 150 Ω		0.13		%
Differential Phase Error	G = +2, NTSC 100 IRE, R_{LOAD} ≥ 150 Ω		0.15		Degrees
INPUT CHARACTERISTICS					
Common-Mode Rejection Ratio (CMRR)	DC to 100 kHz, common-mode voltage (V_{CM}) = 1.5 V to 3.5 V	86	96		dB
	V_{CM} = 1 V p-p at 1 MHz	80			dB
	V_{CM} = 1 V p-p at 10 MHz		70		dB
CMRR with V_{OUT} = 1 V p-p	V_{CM} = 1 V p-p at 1 kHz, V_{OUT} = ±0.5 V dc		72		dB
Common-Mode Voltage Range	+IN voltage (V_{+IN}) − −IN voltage ($V_{−IN}$) = 0 V		1.25 to 3.8		V
Differential Operating Range			±2.5		V
Differential Clipping Level		±2.3	±2.8	±3.3	V
Resistance	Differential		6		MΩ
	Common mode		4		MΩ
Capacitance	Differential		3		pF
	Common mode		4		pF
DC PEFORMANCE					
Closed-Loop Gain Error	V_{OUT} = ±1 V, R_{LOAD} ≥ 150 Ω		±0.1	±0.6	%
	T_{MIN} to T_{MAX}		20		ppm/°C
Open-Loop Gain	V_{OUT} = ±1 V		71		dB
Gain Nonlinearity	V_{OUT} = ±1 V		200		ppm
Input Offset Voltage			0.4	1.8	mV
	T_{MIN} to T_{MAX}		20		µV/°C
	T_{MIN} to T_{MAX}			3.5	mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Offset Voltage vs. Supply	$+V_S$ = 5 V, $-V_S$ = −0.5 V to +0.5 V		−74	−70	dB
	$-V_S$ = 0 V, $+V_S$ = 4.5 V to 5.5 V		−90	−76	dB
Input Bias Current (+IN, −IN)			±0.5	±2	µA
Input Bias Current (REF, FB)			±1	±3.5	µA
	T_{MIN} to T_{MAX} (+IN, −IN, REF, FB)		5		nA/°C
Input Offset Current	(+IN, −IN, REF, FB)		±0.08	±0.4	µA
	T_{MIN} to T_{MAX}		0.2		nA/°C
OUTPUT PERFORMANCE					
Voltage Swing	R_{LOAD} ≥ 150 Ω	1.1		3.9	V
Output Current			35		mA
Short-Circuit Current	To common				
Sinking			−60		mA
Sourcing			55		mA
	T_{MIN} to T_{MAX}		−240		µA/°C
Output Impedance	$\overline{PD}$ ≤ V_{IL}, in power-down mode		10		pF
POWER SUPPLY					
Operating Voltage Range	Total supply voltage	±2.25		±12.6	V
Quiescent Supply Current			9.9	10.6	mA
	T_{MIN} to T_{MAX}		33		µA/°C
	$\overline{PD}$ ≤ V_{IL}		0.65	0.85	mA
	$\overline{PD}$ ≤ V_{IL}, T_{MIN} to T_{MAX}			1	mA
$\overline{PD}$ PIN					
Input Voltage					
High (V_{IH})		+Vs − 1.5			V
Low (V_{IL})				+Vs − 2.5	V
Input Current					
High (I_{IH})	$\overline{PD}$ = minimum V_{IH}			−30	µA
Low (I_{IL})	$\overline{PD}$ = maximum V_{IH}			−50	µA
Input Resistance	$\overline{PD}$ ≤ $+V_S$ − 3 V		12.5		kΩ
	$\overline{PD}$ ≥ $+V_S$ − 2 V		100		kΩ
Enable Time			0.5		µs
OPERATING TEMPERATURE RANGE		−40		+85	°C

ELECTRICAL CHARACTERISTICS—±5 V OPERATION

G = +1, T_A = 25°C, $+V_S$ = ±5 V, REF = 0 V, $\overline{PD}$ ≥ V_{IH}, R_{LOAD} = 1 kΩ, C_L = 2 pF, unless otherwise specified. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} ≤ 0.3 V p-p	240	270		MHz
	V_{OUT} = 2 V p-p	140	155		MHz
Slew Rate	V_{OUT} = 2 V p-p, 25% to 75%	950	1090		V/µs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		20		ns
Rise and Fall Times	V_{OUT} ≤ 1 V p-p, 10% to 90%		1.4		ns
Output Overdrive Recovery			40		ns
NOISE/DISTORTION					
Second Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−79		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−74		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−74		dBc
	V_{OUT} = 2 V p-p, 10 MHz		−74		dBc
Third Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−86		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−81		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−80		dBc
	V_{OUT} = 2 V p-p, 10 MHz		−76		dBc
IMD	V_{OUT} = 2 V p-p, 10 MHz		−70		dBc
Output IP3	V_{OUT} = 2 V p-p, 10 MHz		26		dBm
Input Voltage Noise (RTI)	f ≥ 10 kHz		12.5		nV/√Hz
Input Current Noise (+IN, −IN)	f ≥ 100 kHz		1		pA/√Hz
Input Current Noise (REF, FB)	f ≥ 100 kHz		1.4		pA/√Hz
Differential Gain Error	G = +2, NTSC 100 IRE, R_{LOAD} ≥ 150 Ω		0.13		%
Differential Phase Error	G = +2, NTSC 100 IRE, R_{LOAD} ≥ 150 Ω		0.15		Degrees
INPUT CHARACTERISTICS					
CMRR	DC to 100 kHz, V_{CM} = −3 V to +3.5 V	90	110		dB
	V_{CM} = 1 V p-p at 2 MHz	80			dB
	V_{CM} = 1 V p-p at 10 MHz		70		dB
CMRR with V_{OUT} = 1 V p-p	V_{CM} = 2 V p-p at 1 kHz, V_{OUT} = ±0.5 V dc		83		dB
Common-Mode Voltage Range	V_{+IN} − V_{-IN} = 0 V		±3.8		V
Differential Operating Range			±2.5		V
Differential Clipping Level		±2.3	±2.8	±3.3	V
Resistance	Differential		6		MΩ
	Common mode		4		MΩ
Capacitance	Differential		3		pF
	Common mode		4		pF
DC PEFORMANCE					
Closed-Loop Gain Error	V_{OUT} = ±1 V, R_{LOAD} ≥ 150 Ω		±0.15	±0.6	%
	T_{MIN} to T_{MAX}		10		ppm/°C
Open-Loop Gain	V_{OUT} = ±1 V		74		dB
Gain Nonlinearity	V_{OUT} = ±1 V		200		ppm
Input Offset Voltage			0.4	1.8	mV
	T_{MIN} to T_{MAX}		20		µV/°C
	T_{MIN} to T_{MAX}			3.5	mV
Input Offset Voltage vs. Supply	$+V_S$ = +5 V, $-V_S$ = −4.5 V to −5.5 V		−78	−74	dB
	$-V_S$ = -5 V, $+V_S$ = +4.5 V to +5.5 V		−80	−74	dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Bias Current					
+IN, −IN			±0.5	±2	µA
REF, FB			±1	±3.5	µA
+IN, −IN, REF, FB	T_{MIN} to T_{MAX}		5		nA/°C
Input Offset Current	+IN, −IN, REF, FB		±0.08	±0.4	µA
	T_{MIN} to T_{MAX}		0.2		nA/°C
OUTPUT PERFORMANCE					
Voltage Swing	R_{LOAD} = 150 Ω	±3.6			V
	R_{LOAD} = 1 k Ω	±4.0			V
Output Current			40		mA
Short-Circuit Current	To common				mA
Sinking			−60		mA
Sourcing			55		mA
	T_{MIN} to T_{MAX}		−240		µA/°C
Output Impedance	$\overline{PD}$ ≤ V_{IL}, in power-down mode		10		pF
POWER SUPPLY					
Operating Voltage Range	Total supply voltage	±2.25		±12.6	V
Quiescent Supply Current			10.8	11.6	mA
	T_{MIN} to T_{MAX}		36		µA/°C
	$\overline{PD}$ ≤ V_{IL}		0.68	0.85	mA
	$\overline{PD}$ ≤ V_{IL}, T_{MIN} to T_{MAX}			1	mA
$\overline{PD}$ PIN					
V_{IH}		$+V_S$ − 1.5			V
V_{IL}				$+V_S$ − 2.5	V
I_{IH}	$\overline{PD}$ = minimum V_{IH}			−30	µA
I_{IL}	$\overline{PD}$ = maximum V_{IH}			−50	µA
Input Resistance	$\overline{PD}$ ≤ $+V_S$ − 3 V		12.5		kΩ
	$\overline{PD}$ ≥ $+V_S$ − 2 V		100		kΩ
Enable Time			0.5		µs
OPERATING TEMPERATURE RANGE		−40		+85	°C

ELECTRICAL CHARACTERISTICS—±12 V OPERATION

G = +1, T_A = 25°C, $+V_S$ = ±12 V, REF = 0 V, $\overline{PD}$ ≥ V_{IH}, R_{LOAD} = 1 kΩ, C_L = 2 pF, unless otherwise specified. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} ≤ 0.3 V p-p	250	290		MHz
	V_{OUT} = 2 V p-p	150	175		MHz
Slew Rate	V_{OUT} = 2 V p-p, 25% to 75%	960	1100		V/µs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		20		ns
Rise and Fall Times	V_{OUT} ≤ 1 V p-p, 10% to 90%		1.4		ns
Output Overdrive Recovery			40		ns
NOISE/DISTORTION					
Second Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−79		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−74		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−74		dBc
	V_{OUT} = 2 V p-p, 10 MHz		−74		dBc
Third Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−86		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−81		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−80		dBc
	V_{OUT} = 2 V p-p, 10 MHz		−74		dBc
IMD	V_{OUT} = 2 V p-p, 10 MHz		−70		dBc
Output IP3	V_{OUT} = 2 V p-p, 10 MHz		26		dBm
Input Voltage Noise (RTI)	f ≥ 10 kHz		13		nV/√Hz
Input Current Noise (+IN, −IN)	f ≥ 100 kHz		1		pA/√Hz
Input Current Noise (REF, FB)	f ≥ 100 kHz		1.4		pA/√Hz
Differential Gain Error	G = +2, NTSC 100 IRE, R_{LOAD} ≥ 150 Ω		0.13		%
Differential Phase Error	G = +2, NTSC 100 IRE, R_{LOAD} ≥ 150 Ω		0.2		Degrees
INPUT CHARACTERISTICS					
CMRR	DC to 100 kHz, V_{CM} = ±10 V	88	105		dB
	V_{CM} = 1 V p-p at 2 MHz	80			dB
	V_{CM} = 1 V p-p at 10 MHz		70		dB
CMRR with V_{OUT} = 1 V p-p	V_{CM} = 4 V p-p at 1 kHz, V_{OUT} = ±0.5 V dc		80		dB
Common-Mode Voltage Range	V_{+IN} − $V_{−IN}$ = 0 V		±10.5		V
Differential Operating Range			±2.5		V
Differential Clipping Level		±2.3	±2.8	±3.3	V
Resistance	Differential		6		MΩ
	Common mode		4		MΩ
Capacitance	Differential		3		pF
	Common mode		4		pF
DC PEFORMANCE					
Closed-Loop Gain Error	V_{OUT} = ±1 V, R_{LOAD} ≥ 150 Ω		±0.15	±0.6	%
	T_{MIN} to T_{MAX}		10		ppm/°C
Open-Loop Gain	V_{OUT} = ±1 V		73		dB
Gain Nonlinearity	V_{OUT} = ±1 V		200		ppm
Input Offset Voltage			0.4	1.8	mV
	T_{MIN} to T_{MAX}		20		µV/°C
	T_{MIN} to T_{MAX}			3.5	mV
Input Offset Voltage vs. Supply	$+V_S$ = +12 V, $−V_S$ = −11.0 V to −13.0 V		−77	−70	dB
	$−V_S$ = −12 V, $+V_S$ = 11.0 V to 13.0 V		−88	−70	dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Bias Current					
+IN, −IN			±0.25	±2	µA
REF, FB			±0.5	±3.5	µA
+IN, −IN, REF, FB	T_{MIN} to T_{MAX}		2.5		nA/°C
Input Offset Current	+IN, −IN, REF, FB		±0.08	±0.4	µA
	T_{MIN} to T_{MAX}		0.2		nA/°C
OUTPUT PERFORMANCE					
Voltage Swing	R_{LOAD} = 700 Ω	±10.8			V
Output Current			40		mA
Short-Circuit Current	To common				mA
Sinking			−60		mA
Sourcing			55		mA
	T_{MIN} to T_{MAX}		−240		µA/°C
Output Impedance	$\overline{PD} \leq V_{IL}$, in power-down mode		10		pF
POWER SUPPLY					
Operating Voltage Range	Total supply voltage	±2.25		±12.6	V
Quiescent Supply Current			13	13.9	mA
	T_{MIN} to T_{MAX}		43		µA/°C
	$\overline{PD} \leq V_{IL}$		0.73	0.9	mA
	$\overline{PD} \leq V_{IL}$, T_{MIN} to T_{MAX}			1.1	mA
$\overline{PD}$PIN					
V_{IH}		$+V_S - 1.5$			V
V_{IL}				$+V_S - 2.5$	V
I_{IH}	$\overline{PD}$ = minimum V_{IH}			−30	µA
I_{IL}	$\overline{PD}$ = maximum V_{IH}			−50	µA
Input Resistance	$\overline{PD} \leq +V_S - 3$ V		3		kΩ
	$\overline{PD} \geq +V_S - 2$ V		100		kΩ
Enable Time			0.5		µs
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	26.4 V
Input Voltage (Any Input)	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Differential Input Voltage	±8.4 V
Storage Temperature Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

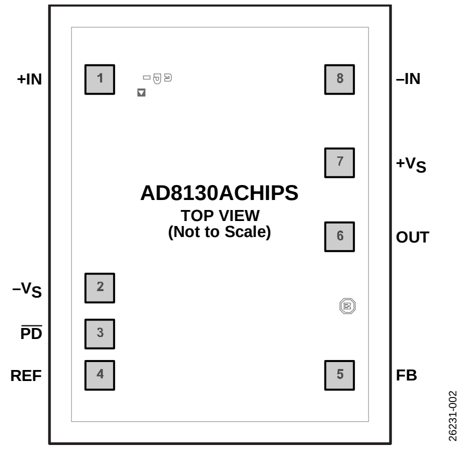

Figure 2. Pad Configuration

Table 5. Pad Configuration Descriptions[1]

Pad No.	Mnemonic	X-Axis (µm)	Y-Axis (µm)	Description
1	+IN	−385	+465	Noninverting Input
2	$-V_S$	−385	−204	Negative Supply Voltage
3	$\overline{PD}$	−385	−352	Power-Down
4	REF	−385	−484	Reference
5	FB	+385	−506	Feedback
6	OUT	+385	−41	Output
7	$+V_S$	+385	+198	Positive Supply Voltage
8	−IN	+385	+465	Inverting Input

[1] All dimensions are referenced from the center of the die to the center of each bond pad.

OUTLINE DIMENSIONS

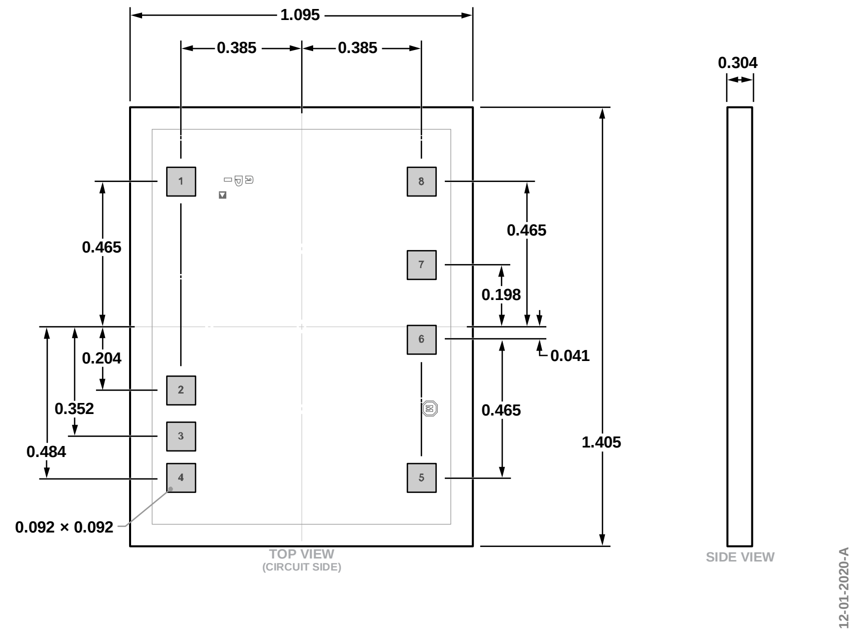

Figure 3. 8-Pad Bare Die [CHIP]
(C-8-26)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Die Specifications

Parameter	Value	Unit
Chip Size	1020 × 1330	µm
Scribe Line Width	75	µm
Die Size	1095 × 1405	µm
Thickness	305	µm
Backside	$-V_S$ or left floating	V
Passivation	Doped oxide/silicon nitride (SiN)	Not applicable
Polyimide Thickness	7	µm
Bond Pads (Minimum)	92 × 92	µm
Bond Pad Composition	99.5 aluminum (Al), 0.5 copper (Cu)	%

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Hitachi EN 4900GC conductive
Bonding Method	1 mil gold
Bonding Sequence	Unspecified

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8130ACHIPS	−40°C to +85°C	8-Pad Bare Die [CHIP], Waffle Pack	C-8-26	1980

[1] AD8130ACHIPS is a RoHS compliant part.

D26231-6/21(0)