User Manual

DA1469x PRO Development Kit

UM-B-093

Abstract

DA1469x Development Kit Pro hardware provides a tested reference platform, access to all signals for connecting peripherals, and advanced debugging features.

Contents

Figures

Tables

1 Terms and Definitions

BLE	Bluetooth Low Energy
CIB	Communication Interface Board
DB	Daughterboard
LRA	Linear Resonant Actuator
ERM	Eccentric Rotating Mass
GPIO	General Purpose Input Output
HDK	HW Development Kit
I^2C	Inter-Integrated Circuit
JTAG	Join Test Action Group
LDO	Low Dropout
LRA	Linear Resonant Actuator
MB	Motherboard
MISO	Master In Slave Out
MOSI	Master Out Slave In
NTC	Negative temperature coefficient (resistor)
OVP	Over Voltage Protection
PCB	Printed Circuit Board
PRS	Product Requirement Specification
QSPI	Quad Serial Peripheral Interface
RF	Radio Frequency
RFIO	Radio Frequency Input Output
SDK	SW Development Kit
SIMO	Single-Inductor Multiple-Output
SOC	System on Chip
SPI	Serial Peripheral Interface
SW	Software
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

2 References

[1] DA1469x, Datasheet, Dialog Semiconductor.
[2] AN-B-052, DA1458x/68x Development Kit J-Link Interface, Application Note, Dialog Semiconductor.
[3] AN-B-037, DA1468x Power Measurements, Application Note, Dialog Semiconductor.
[4] DA1469x Pro Development Kit Mainboard Schematics, Reference Design, Dialog Semiconductor.
[5] DA1469x Pro Development Kit VFBGA-100 Schematics, Reference Design, Dialog Semiconductor.
[6] DA1469x Pro Development Kit VFBGA-86 Daughterboard Schematics, Reference Design, Dialog Semiconductor.

3 DA1469x DK PRO Hardware Architecture and Implementation

3.1 Introduction

The DA1469x development kit PRO is available as a mainboard providing a socket for one of two variants of daughterboard (VFBGA-100/LFBGA-86).

Our engineers have paid special attention in designing this DK to provide trouble-free user experiences and to keep compatibility with existing tools from DA1458x/DA1468x/ product lines.

When combined with the DA1469x SDK and SmartSnippets tools, the DA1469x DK PRO provides an easy-to-use and complete platform for software/hardware development.

3.2 Features

- Flexible battery options
- QSPI-Flash memory for booting
- Headers for I/O monitoring and expandability
- Option to support Arduino shields
- Option to support MikroBUS click boards
- Provisions for automated test
- On-board basic peripherals for demo and development
- JTAG debugger and connectivity to PC
- Look and feel similar to DA14680 PRO DK
- DA1469x silicon easily replaceable on a daughterboard core module

3.3 DA1469x PRO DK Hardware Block Diagram

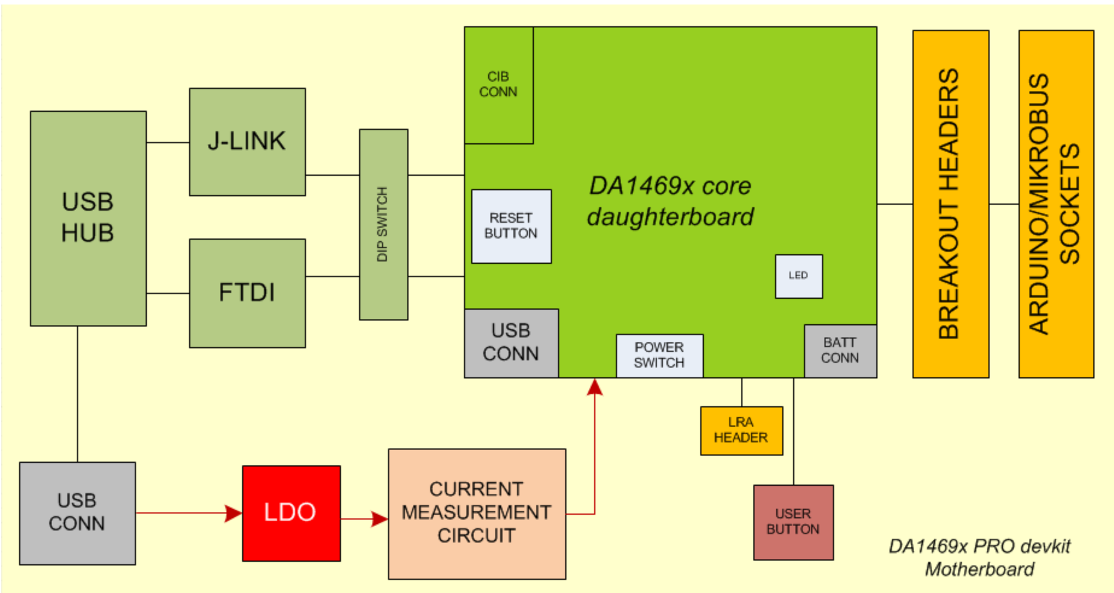

Figure 1: System Block Diagram

3.4 Main Features of Mainboard in DA1469x PRO DK

- Main USB connector

NOTE
USB host must support USB 2.0 high-speed for reliable power measurements.

- USB hub with two downstream ports:
  - Port1: SEGGER JLink-OB SWD-JTAG debugger for ARM Cortex M33
  - Port2: FT2232H multiprotocol serial interface providing a booting/debugging/HCI UART (2-pin or 4-pin) and SPI connected to the current measurement circuit Analog/Digital converter
- Low profile Connectors mating to the 69x daughterboard
- Breakout Headers (Figure 2, two pieces, 2 × 20 pins in each piece) for monitoring GPIO and power signals, with markings of signal names on the PCB top silkscreen

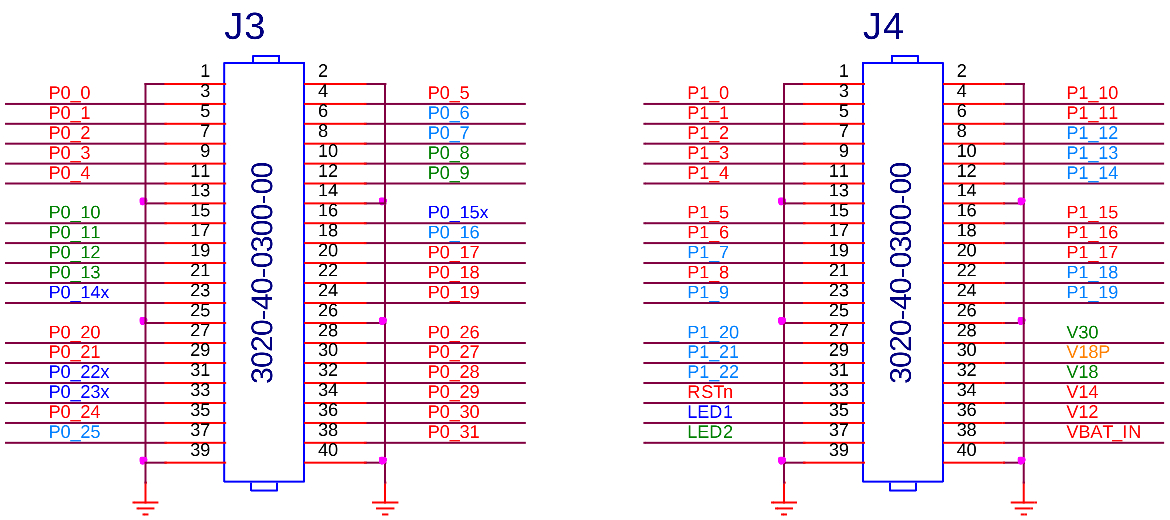

Figure 2: DA1469x DK PRO Mainboard Breakout Headers

- Headers for the dedicated LRA/ERM haptic motor driver pins
- One user button K1, connected to a GPIO through a jumper
- LDO adjustable from 1.8 V up to 4.2 V to supply the VBAT pin (default 3.0 V)

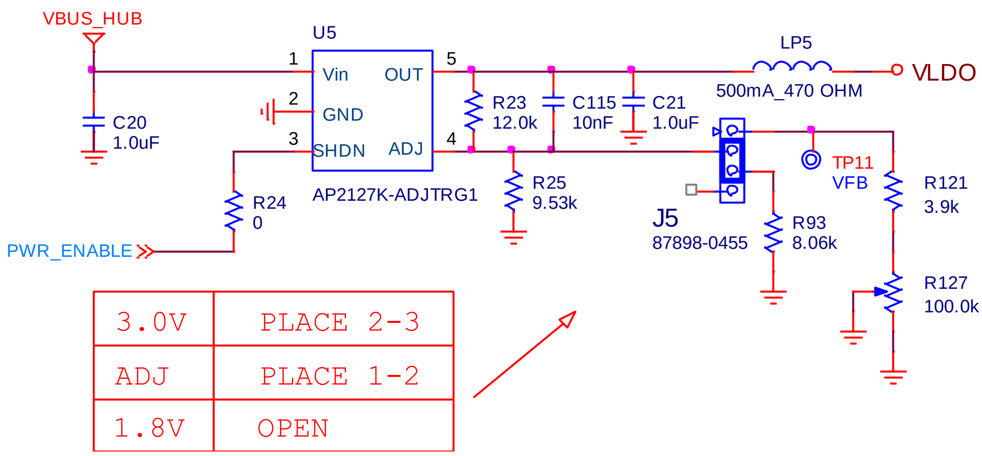

Figure 3: VBAT Adjustable LDO

- Circuit to measure/monitor the current from LDO to VBAT
  - Software trigger support for SmartSnippets Toolbox (driven from a DA1469x GPIO, P0_16, through a jumper)
- DIP switch to isolate UART and JTAG signals (in case we need to secure the most accurate sleep current measurements, Figure 4)
  - The board is shipped with all switches at the "ON" position (all signals connected to the related DA1469x pins)
  - Signal names are marked on PCB top silkscreen

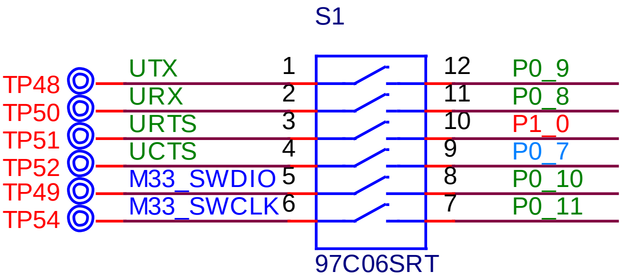

Figure 4: DIP Switch

- Test points (TP) for automated production test (placed on the bottom of the board)
- Ground points (TP28 and TP29) for connecting crocodile clips
- QSPI-RAM option (not populated)
- Optional Arduino sockets (supporting 3.3 V compatible Arduino shields)

Figure 5: Arduino Sockets

- Optional 2× MikroBUS sockets (supporting 3.3 V compatible click boards from MikroElektronika or other sources)

Figure 6: MikroBUS sockets

3.5 User Accessible Elements in DA1469x PRO DK

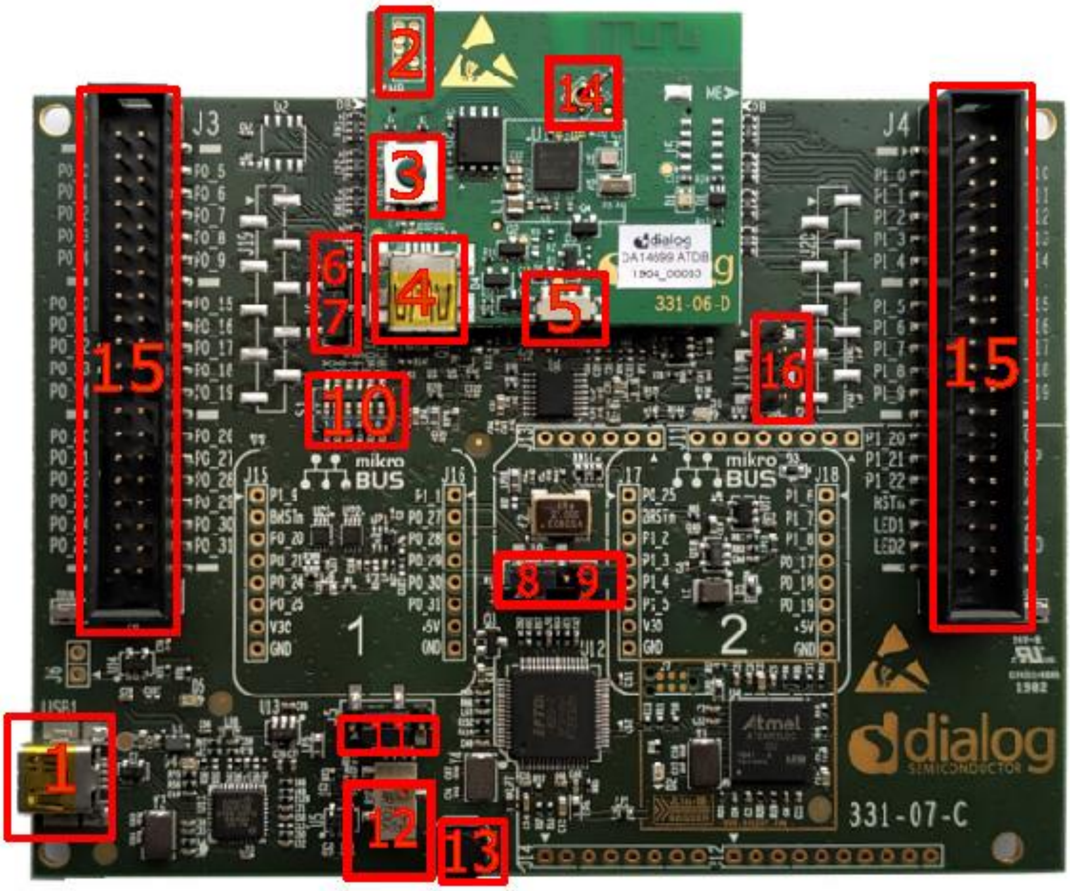

Figure 7: Main Accessible Features in Main Board/Daughter Board in DA1469x PRO DK

1. USB connector on mainboard for power and communication interface
2. Connector for CIB cable (option for JTAG/UART in standalone daughterboard)
3. Reset button
4. USB connector on daughterboard, which is an alternative power option and connects to DA1469x USB data pins
5. Power selector switch [LDO or battery]
6. Header for current measurement circuit input (J9.1-2)
7. Header for current measurement circuit output (J9.3-4)
8. Header (J8.1-2) for enabling user button (K1 on mainboard)
9. Software trigger header (J8.3-4)
10. DIP switch (S1) connecting the debugging interface signals (JTAG/UART)
11. LDO voltage selection header, J5, (3.0 V as default, can be adjustable from 1.8 V to 4.2 V)
12. Trimmer to define the adjustable LDO voltage (R127)
13. User button (K1)
14. RF coaxial switch (J7 on daughterboard)
15. Signal/Power breakout headers (J3 and J4)
16. LRA/ERM interface header (J10)

3.6 DA1469x PRO DK Daughterboard (db-VFBGA-100 and db-LFBGA-86)

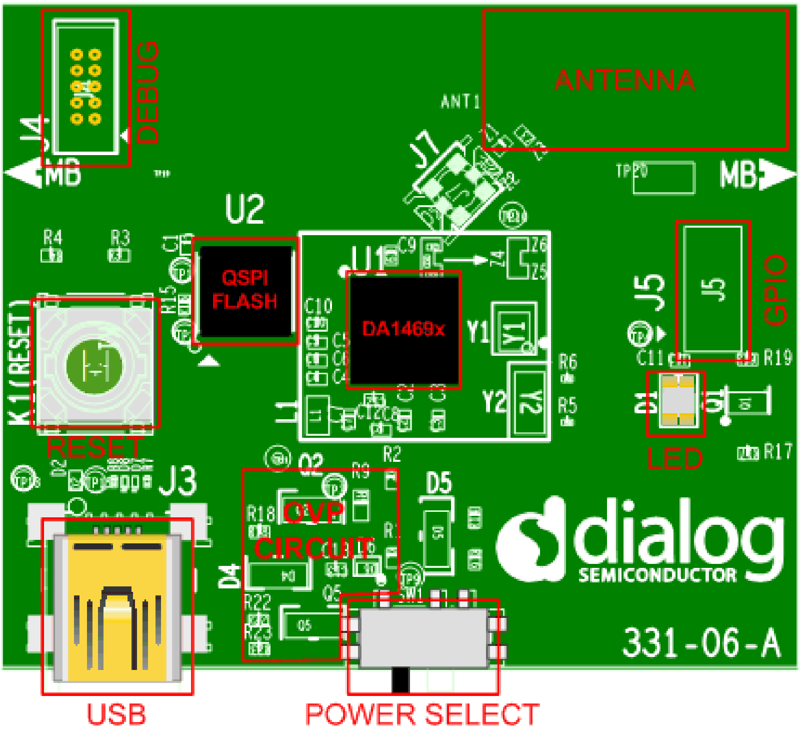

Figure 8: DA1469x PRO DK Daughterboard

- DA1469x in micro-BGA package (U1)
- Crystals with frequencies of 32 MHz and 32.768 kHz, (Y1 and Y2, respectively)
- QSPI Flash (SOIC-8 or USON-8 package), the default of which is W25Q80EWSNIG (8 Mbit), (U2)
- Printed RF antenna (ANT1)
- Coaxial switch for conducted RF measurements (J7)
- Reset button, K1(RESET)
- USB connector for charging and data communications (supporting USB 2.0 full speed), (J3)
- OVP circuit on the VBUS power input (Figure 9)

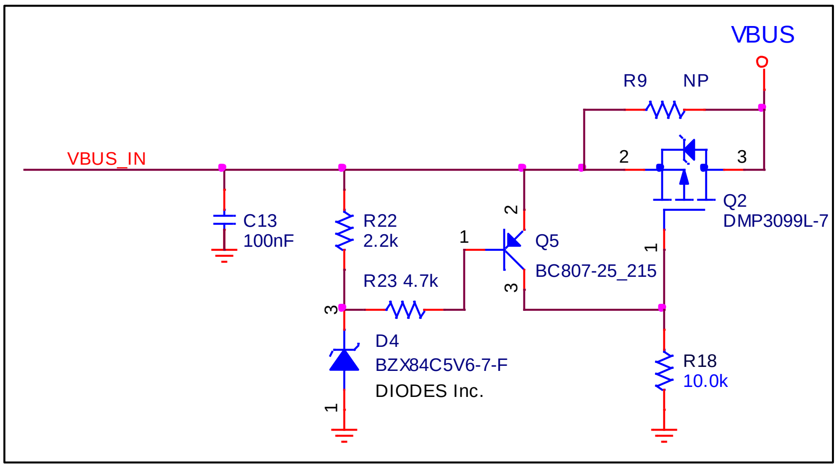

Figure 9: USB Overvoltage Protection

- Battery/Power connectors (Figure 10):
  - 2-pin connector for Li-Ion/LiPo (J6, default)
  - Optional coin cell holder (unpopulated, CR2032 type)
  - Power selector switch (can be used as on-off switch), (SW1)

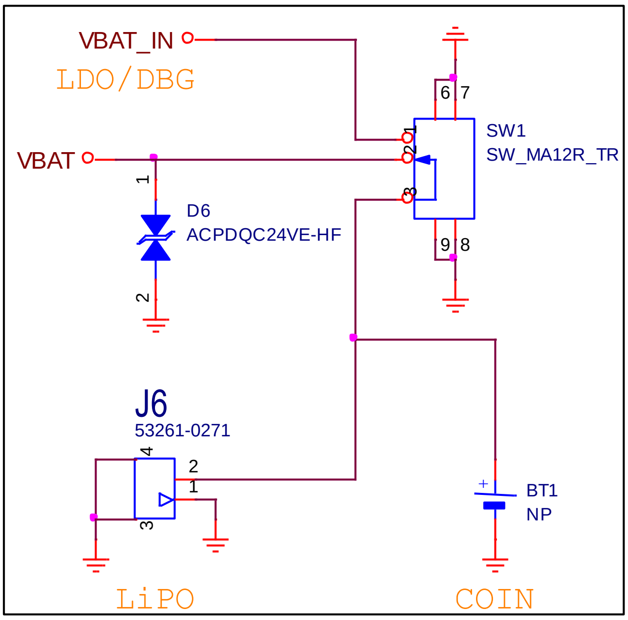

Figure 10: Power Options

- Low profile connectors (2×, placed on the bottom of the PCB, Figure 11) matching a set of mating connectors on the main board (J1, J2)

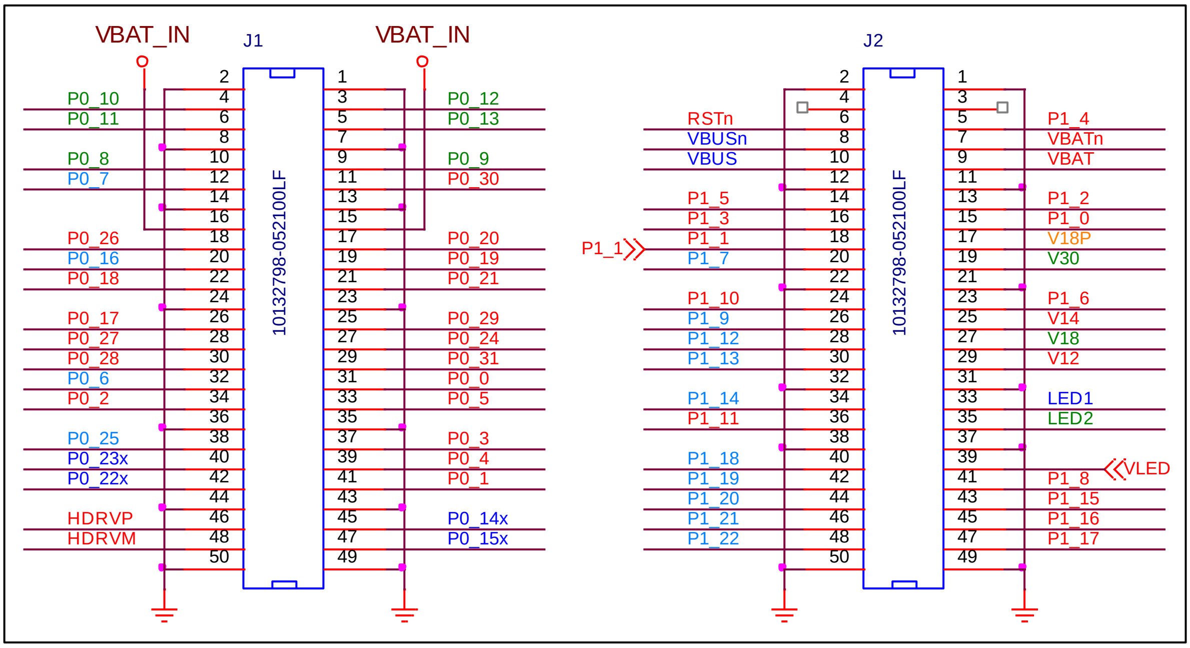

Figure 11: Connection to Mainboard

- CIB debugging connector (Figure 12):
  - SWD pins connected to Cortex M33 core
  - Reset from JLink-OB or button on the CIB board

- ○ 2-pin UART signals connected to bootable UART pins
- ○ Can provide power to the daughterboard in stand-alone operation

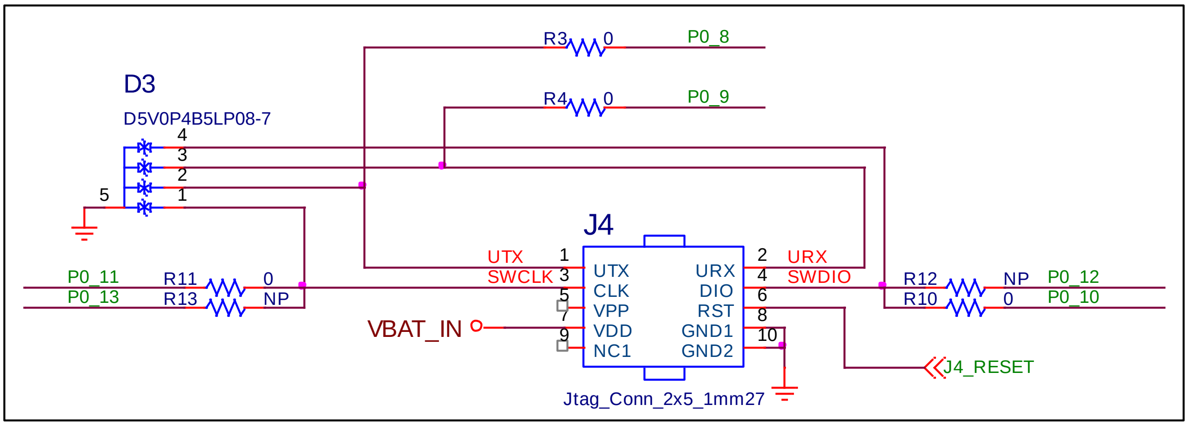

Figure 12: CIB Debugging Header

- RGB LED, (D3)

NOTE
The RGB LED is only available on the DA14699 daughterboard.

- ○ Green and Blue segments connected to dedicated LED driver pins
- ○ Red segment connected to a MOSFET driven by a GPIO
- ○ Circuit for powering the LED from either VBUS or VBAT
- ○ Option to power the LEDs from the 6.0 V available on the mainboard. If this option is chosen, the SmartSnippets Toolbox measurement will exclude the LED current

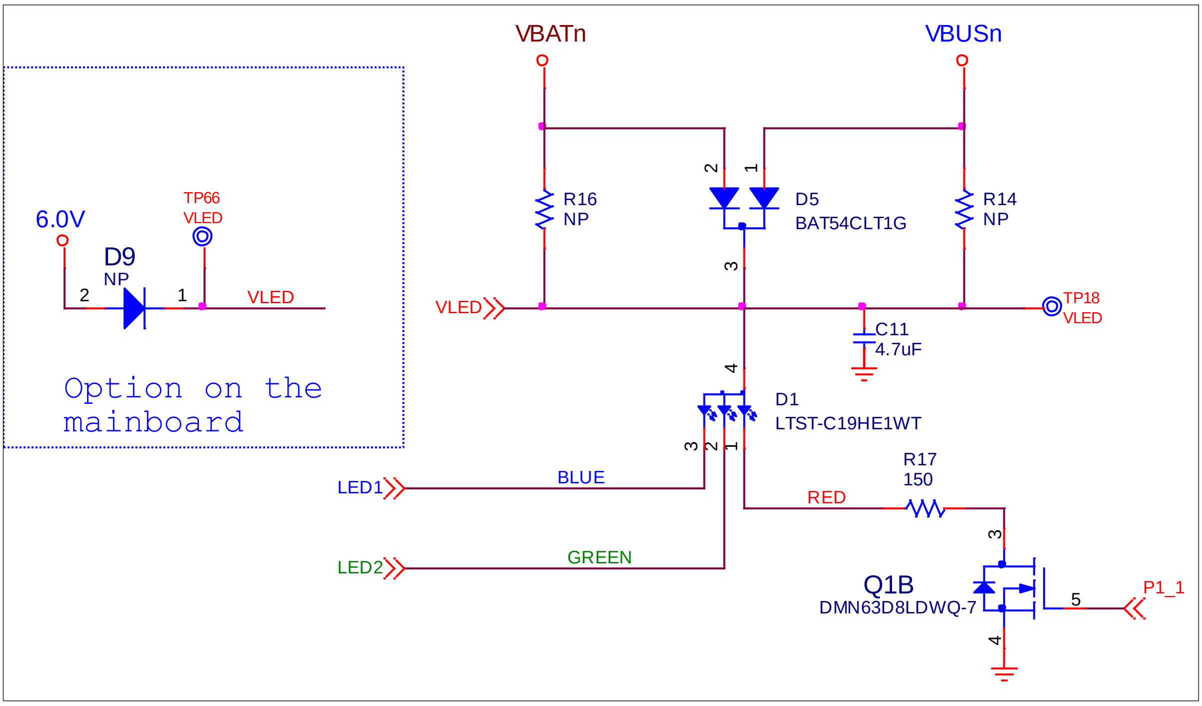

Figure 13: LED Powering Circuit

- ESD protection diodes at the most susceptible points (USB connector J3, CIB interface J4, and power selector switch SW1)

- Possibility to operate stand-alone (without the mainboard), powered from one of these options:
  - Li-Ion/LiPo/coin Battery
  - USB connector
  - CIB interface (providing also JTAG/UART debugging functions)

3.7 Current Measurement Section in DA1469x DK PRO

- Following the DA1469x DK current measurement topology and circuitry
- Full scale range 250 mA
- Measurement accuracy down to 1 µA
- Current sense resistors of 2.37 Ω in series to VBAT
- FTDI chip for transferring data to the PC
- Analog processing blocks
- Software trigger circuit
- Fast 24-bit ADC with SPI interface
- Known limitation: measurement accuracy between 500 µA and 1 mA is worse than the typical 1% we have in all other cases (from 1 µA to 250 mA)

3.8 DA1469x PRO DK Power Block Diagram

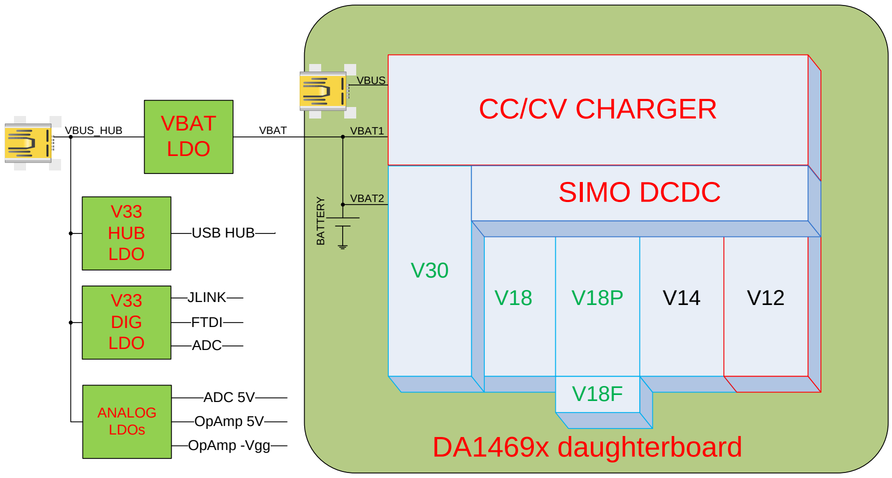

Figure 14: DA1469x PRO DK Power Distribution Diagram

DA1469x system consists of the SoC, QSPI, and the peripherals that are directly connected to the chip.

Four possible power sources can be used for DA1469x system:

- USB on the daughterboard (feeding VBUS pin)
- Li-ion/Li-Po/coin battery on the daughterboard (VBAT)
- Debugging (CIB) port on the daughterboard (VBAT)
- Adjustable LDO (default) supplied by the USB connector on the main board (VBAT). **This is the only option where current can be measured by SmartSnippets Toolbox**. By default, the LDO provides 3.0 V.

All DCDC outputs are supplemented by automatic bypass LDOs (default at startup) and retainer LDOs and/or voltage clamps (for lower consumption in sleep mode). For more details check the [1] DA1469x datasheet.

The debugging section consists of JTAG, UART, and current sense circuitry. This section is supplied from the mainboard USB connector.

The USB Hub has its own dedicated 3.3 V LDO (U13, always on, Figure 15).

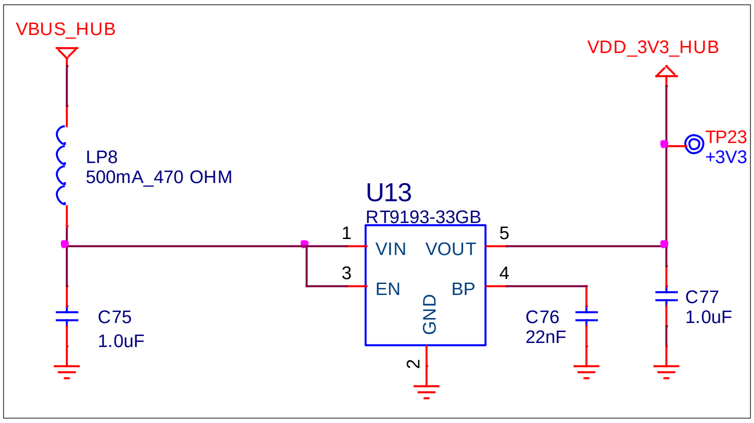

Figure 15: 3.3V LDO for USB Hub

The remaining support circuits on the mainboard are powered by a second 3.3 V supply (U14). This powers SEGGER (U4), FTDI (U12), and ADC (U8).

U14 is enabled by a signal coming from the USB hub. This signal (PWR_ENABLE) goes high after the hub has successfully enumerated with a USB host. If we need to operate the system without a host, for example, with an AC wall adapter, we need to solder a header on J6 and place a jumper.

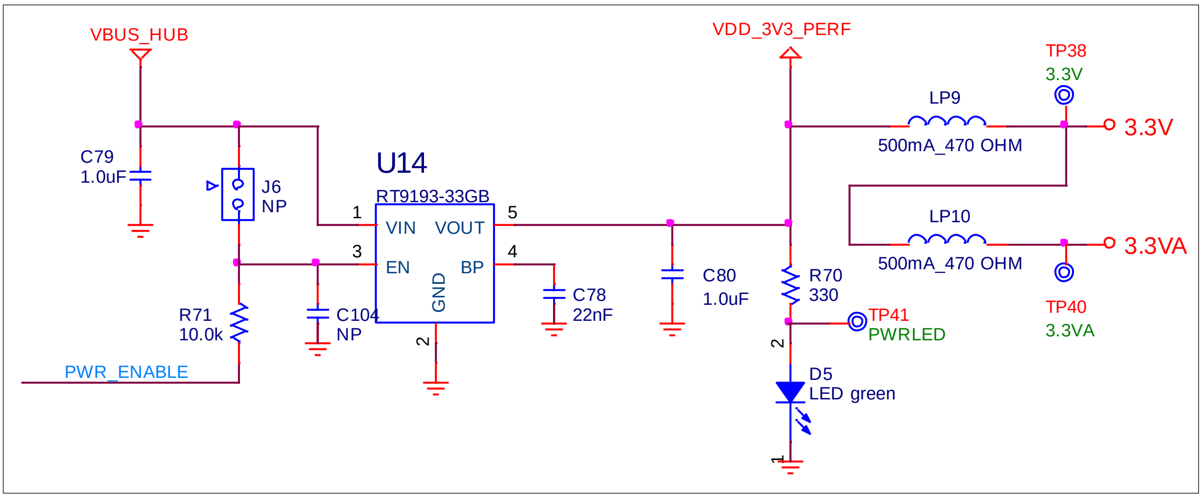

Figure 16: 3.3 V LDO for Mainboard Peripherals

The analog/digital converter and several op-amps on the current measurement section need a clean 5.0 V power supply (Figure 17). This is generated by a step-up regulator (U18) which generates 6.0 V, and U18 is followed by a 5 V LDO (U17). U18 is also controlled by PWR_ENABLED.

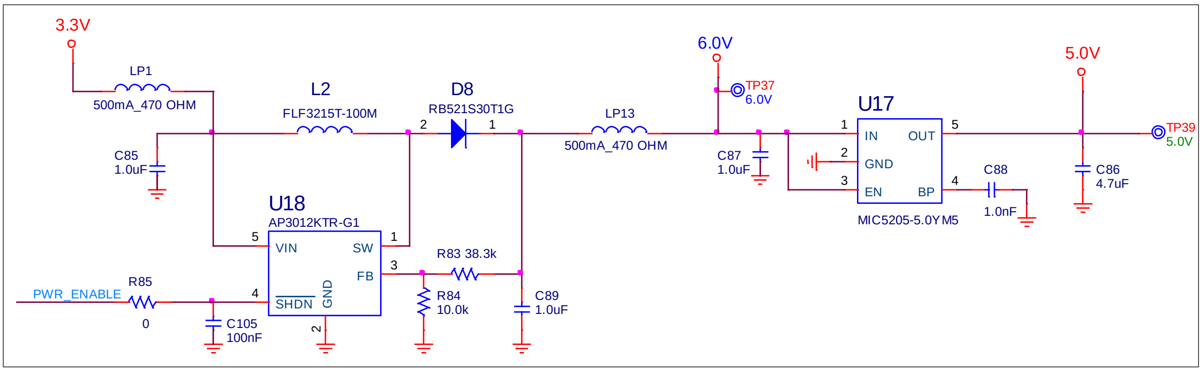

Figure 17: Op-Amps/ADC 5.0 V Power Supply

The Op-Amps also require a small negative supply (-0.232 V) generated by U20 (Figure 18).

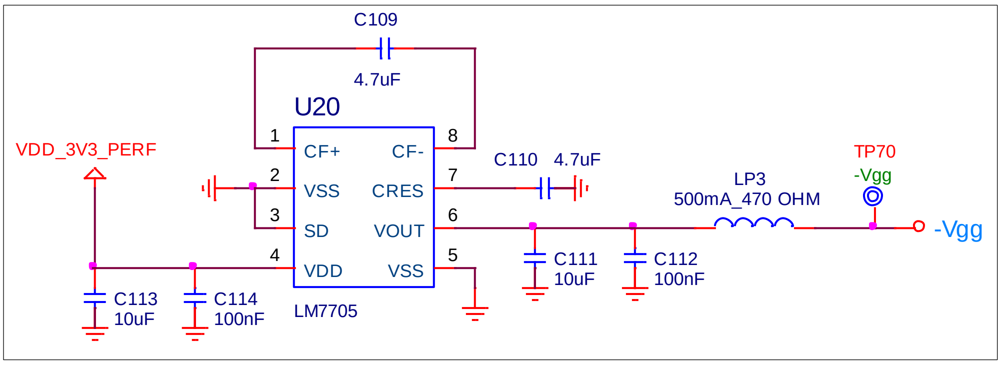

Figure 18: Negative Supply for Op-Amps

3.9 Voltage Level Translation (Debugging) for Avoiding Leakage

Voltage translation is required because the DA1469x I/O voltage varies depending on the battery level and setting for the I/OLDO (V30).For example, if the other side (on board interfaces, JTAG/UART) is fixed at 3.3 V, there is a leakage through the pins if the DA1469x voltage I/Os are at 3.0 V or less.

Table 1: Signals with Level Translation

Pin Name	Signal Name
P0_10	SWDIO
P0_11	SWCLK
P0_9	UTX
P0_8	URX
P1_0	URTS
P0_7	UCTS

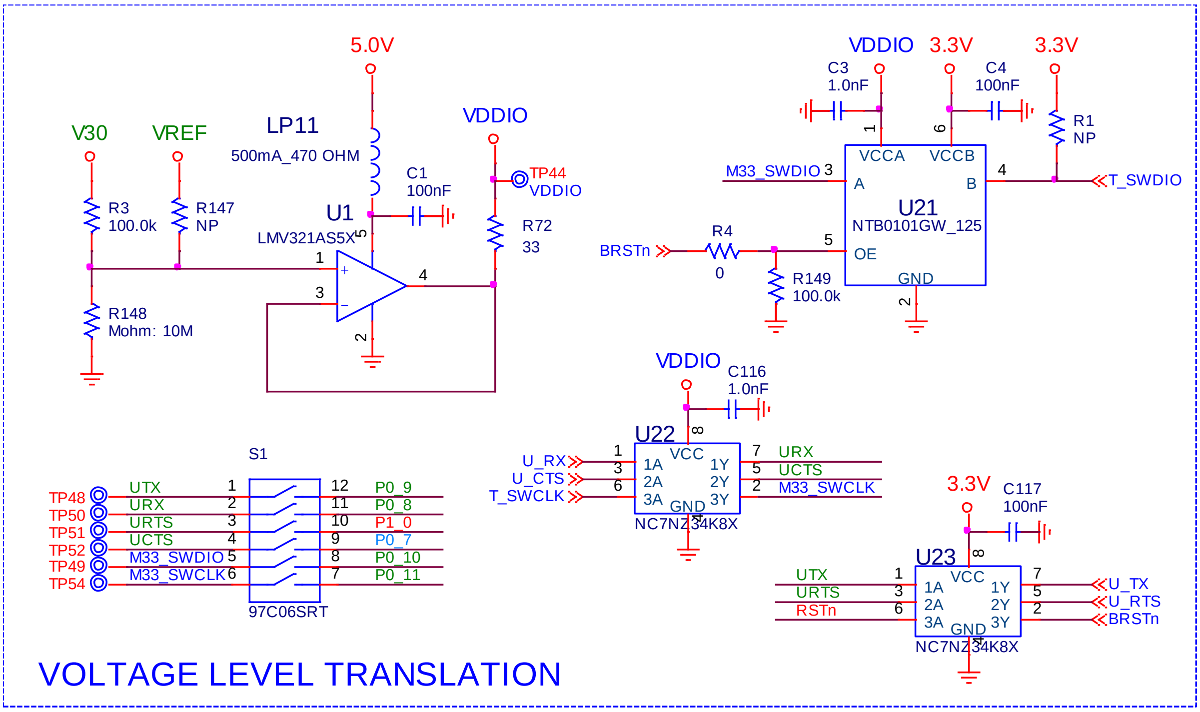

Figure 19: Voltage Level Translation Circuit

VDDIO is a buffered version of the voltage used in the I/O from DA1469x side. This powers a triple buffer gate (U22) with the direction from mainboard to DA1469x pins and also the single bidirectional transceiver used for SWDIO (U21) on the DA1469x side.

The direction of signals from DA1469x to the mainboard is handled by U23 powered from the mainboard 3.3 V.

The DA1469x debugging pins can be disconnected by the associated main board peripherals through the multiple DIP-switch S1.

3.10 Mainboard/Daughterboard Mechanical Mating

The daughterboard can be placed on top of the mainboard via two low-profile SMD connectors, which are specified for a limited number of mating cycles (50).

Table 2: Mainboard/Daughterboard Mating Connectors

Main Board	Daughter Board
 Amphenol FCI 10132797-055100LF	 Amphenol FCI 10132798-052100LF

NOTE: The connectors have no polarity feature, so please be careful not to connect the daughterboard rotated by 180°. Small arrows on the top silk screens of both boards are added to indicate a properly aligned placement (Figure 20). The arrows on the mainboard must point to the arrows on the daughterboard.

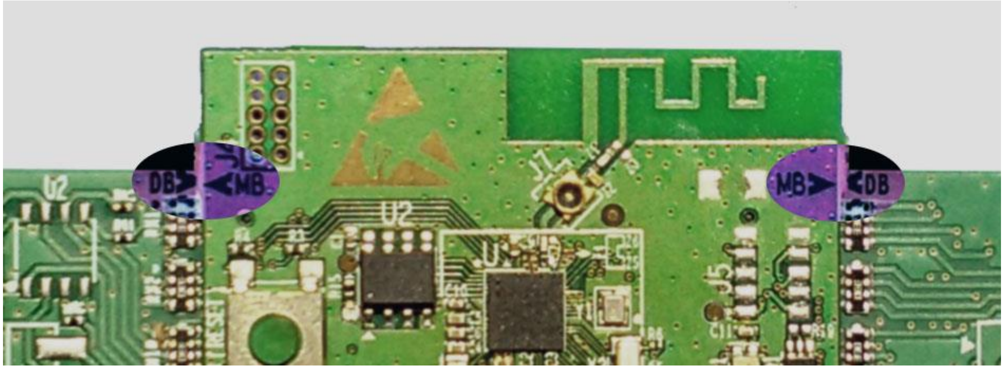

Figure 20: Mainboard/Daughterboard Alignment

3.11 GPIO Assignments

Table 3: Mainboard/Daughterboard Pin Assignment

Pin Name	DK Function	Comments
P0_0	QSPIR_D0	QSPI RAM for parallel LCD framebuffer. 1.8 V only.
P0_1	QSPIR_D1	
P0_2	QSPIR_D2	
P0_3	QSPIR_D3	
P0_4	QSPIR_CSn	
P0_5	QSPIR_CLK	
P0_6	GP_BUTT	
P0_7	UCTS	
P0_8	URXD	
P0_9	UTXD	
P0_10	M33 SWDIO	
P0_11	M33 SWCLK	
P0_12		
P0_13		
P0_14	USB_DP	Daughterboard USB
P0_15	USB_DM	
P0_16	C_TRIG	software trigger
P0_17		
P0_18		
P0_19		
P0_20		
P0_21		
P0_22	XTAL32km	Daughterboard xtal 32.768kHz
P0_23	XTAL32kp	
P0_24		
P0_25		
P0_26		

Pin Name	DK Function	Comments
P0_27		
P0_28		
P0_29		
P0_30		
P0_31		
P1_0	URTS	
P1_1	RGB LED (RED)	Daughterboard LED
P1_2		
P1_3		
P1_4		
P1_5		
P1_6		
P1_7		
P1_8		
P1_9		
P1_10		
P1_11		
P1_12		
P1_13		
P1_14		
P1_15		
P1_16		
P1_17		
P1_18		
P1_19		
P1_20		
P1_21		
P1_22		
LED1	RGB LED (BLUE)	Daughterboard LED
LED2	RGB LED (GREEN)	
HDRVP	J10 HEADER	LRA/ERM motor driving pins
HDRVM		
RSTn	RESET (active low)	Daughterboard button

Note 1 USB and XTAL32k signals are typically not connected to the mainboard breakout headers. Series resistors must be placed on the daughterboard to connect these signals.

Note 2 LCD (various types), micro-motor drive, ADC inputs, NTC (charger), and sleep mode PWM outputs are available on specific pins only. Check the DA1469x datasheet [1] for more details.

3.12 Jumper/DIP Switch Settings

Table 4: Default Jumper Settings

Jumper Block	Default Position	Comment
J5	2-3	Selects 3.0 V as default VBAT
J6	not placed	
J8	1-2 & 3-4	button (K1) and C_TRIG
J9	1-2 & 3-4	Current measurement input and output
J10	1-2 no jumpers	Haptic driver outputs
	3-4	Enable reset from SEGGER

The DIP switch (S1) has all individual segments set to the “ON” position by default.

3.13 QSPI-RAM Operation

QSPI-RAM may be used in applications where we need bulk data transfers with DMA. The most common case is as an LCD framebuffer. The selected QSPI-RAM chip (APS6404L-SQ-SN) is **not populated** on the PCBs and it has to be added by users.

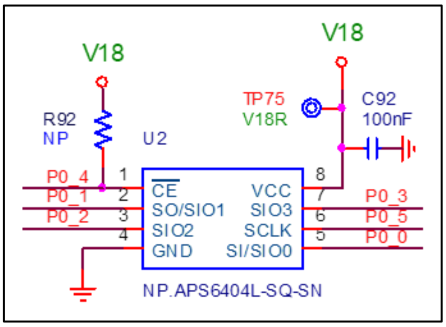

Figure 21: QSPI-RAM

3.14 Test Section

Table 5: Mainboard Test Points (Placed on the Bottom Of DA1469x PRO DK)

TP Name on Reference Design	Signal Name	Comments
TP1	VDD_CR	3.3V (SEGGER)
TP2	T_RESET	JTAG Reset
TP3	sERASE	SEGGER chip programming
TP4	sVCC	
TP5	sRST	
TP6	sDIO	
TP7	sCLK	
TP8	sTDI	
TP9	DBLED	SEGGER LED

TP Name on Reference Design	Signal Name	Comments
TP10	sTDO	SEGGER chip programming
TP11	VFB	VBAT LDO feedback
TP12	VBAT	3.0 V
TP13	VINN	2.5 V
TP14	VINP	2.5 V
TP15	5.0VA	5 V (ADC analog)
TP16	VREF	2.5 V
TP17	27MHz	ADC reference clock
TP18	VREG	1.8 V (FTDI)
TP19	VBUS2	5 V (USB)
TP20	PWR_EN	Enable for most LDOs
TP23	+3V3	3.3 V (USB hub)
TP24	GND	
TP25	GND	
TP26	GND	
TP27	GND	
TP30	RSTn	RESETn (from db)
TP31	V12	1.2 V (from db)
TP32	V14	1.4 V (from db)
TP36	USBLED	USB hub LED
TP37	6.0V	6 V
TP38	3.3V	3.3 V
TP39	5.0V	5 V
TP40	3.3VA	3.3 V
TP41	PWRLED	3.3 V Peripheral Power LED
TP42	VOUT	Current measurement output (high scale)
TP44	VDDIO	VDDIO (buffered V30)
TP48	UTX	UART Tx (FTDI side)
TP49	SWDIO	SEGGER data I/O
TP50	URX	UART Rx (FTDI side)
TP51	URTS	UART RTS (FTDI side)
TP52	UCTS	UART CTS (FTDI side)

TP Name on Reference Design	Signal Name	Comments
TP54	SWCLK	SEGGER Clock
TP56	C_TRIG	Software trigger for SmartSnippets Toolbox
TP57	V30	3.0 V
TP58	OSC_EN	Enable for ADC clock
TP59	BCBUS7	Aux I/O from FTDI
TP60	VOUT2	Current measurement output (low scale)
TP61	SEL	ADC control from FTDI
TP62	VS+	Current measurement sense+
TP63	VS-	Current measurement sense-
TP64	BCBUS5	Aux I/O from FTDI

Table 6: Daughterboard Test Points

TP Name on Reference Design	Signal Name	Comments	Position on Daughter Board
TP1	V18	1.8 V ± 5%	top
TP2	FCS	Flash chip select	top
TP3	VBUS	5.0 V ± 5% (output of OVP circuit)	top
TP4	V30	3.0 V ± 2%	top
TP5	V18	1.8 V ± 5%	bottom
TP6	V18P	1.8 V ± 5%	bottom
TP7	V14	1.4 V ± 5%	bottom
TP8	V12	1.2 V ± 5%	bottom
TP9	VBAT	Battery (default LDO 3.0 V ± 2%)	top
TP12	GND		bottom
TP13	GND		top
TP14	GND		bottom
TP15	VBUS_IN	5.0 V ± 5% (from USB, before OVP)	top
TP16	VBATn	VBAT pin (default LDO 3.0 V ± 2 %)	bottom
TP17	VBUSn	5.0 V ± 5% (to DA1469x pin)	bottom
TP18	VLED	LED power (VBUS or VBAT - 0.2 V)	bottom
TP20	GND		top
TP21	V18	VFLASH 1.8 V ± 5%	bottom

Revision History

<table>
<tr><th>Revision</th><th>Date</th><th>Description</th></tr>
<tr><td>1.2</td><td>17-Jan-2022</td><td>Updated logo, disclaimer, copyright.</td></tr>
<tr><td>1.1</td><td>19-Feb-2019</td><td>To be released with DA1469x Pro DKs.</td></tr>
<tr><td colspan="3">Change details:
● Update document title to “DA1469x PRO Development Kit”
● Removed reference to Basic Kit
● Minor text editing
● Improved template compliance</td></tr>
<tr><td>1.0</td><td>15-Feb-2018</td><td>Initial version (specification)</td></tr>
</table>

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

