LMH0366 3 Gbps HD/SD SDI Low Power Reclocker with Integrated Eye Monitor

Check for Samples: LMH0366

FEATURES

- **SMPTE ST 424, SMPTE ST 292, and SMPTE ST 259-C Compliant**
- **Supports 125 Mbps, 270 Mbps, 1.4835 Gbps, 1.485 Gbps, 2.967 Gbps, and 2.97 Gbps Serial Data Rate Operation**
- **Supports DVB-ASI at 270 Mbps and MADI at 125 Mbps**
- **100 mW Typical Power Consumption (145 mW with Both Output Drivers Enabled)**
- **Input Equalization (0-60” FR4) and Input Signal Detection**
- **Two Differential, Reclocked Outputs with Option of Recovered Clock**
- **Output De-Emphasis to Compensate for up to 40” of FR4 Trace Losses**
- **64 x 64 Point Eye Opening Monitor**
- **27 MHz External Reference or Referenceless Operation**
- **Internally Terminated 100Ω Input with Rail-to-Rail Input Common Mode Voltage**
- **Internally Terminated 100Ω LVDS Outputs with Programmable Output Common Mode Voltage and Swing**
- **Single 2.5V Supply Operation**
- **Power Save Mode with Device Power Down Control**
- **Industrial Temperature Range: -40°C to +85°C**

APPLICATIONS

- **SMPTE ST 424, SMPTE ST 292, and ST SMPTE 259 Serial Digital Interfaces**
- **Broadcast Video Routers, Switchers, and Distribution Amplifiers**

DESCRIPTION

The LMH0366 3 Gbps HD/SD SDI Low Power Reclocker with Integrated Eye Monitor retimes serial digital video data conforming to the SMPTE ST 424, SMPTE ST 292, and SMPTE ST 259-C standards. The reclocker operates at serial data rates of 125 Mbps, 270 Mbps, 1.4835 Gbps, 1.485 Gbps, 2.967 Gbps, and 2.97 Gbps.

The LMH0366 automatically detects the incoming data rate and retimes the data to suppress accumulated jitter. The reclocker recovers the serial data-rate clock and optionally provides it as an output.

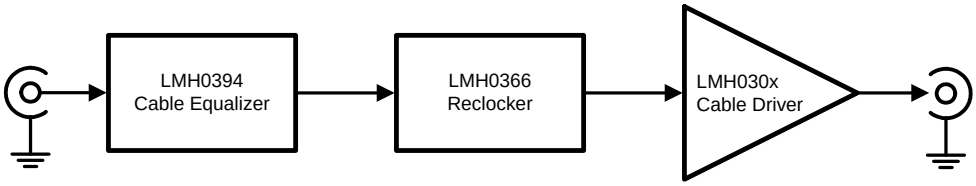
The LMH0366 input has an FR4 equalizer capable of equalizing 0-60” of FR4 trace length, and also includes signal detection with a programmable threshold.

The LMH0366 has two differential serial data outputs and offers flexibility in selecting the output signals between the reclocked data, recovered clock, or bypassed data. The output drivers offer programmable de-emphasis for up to 40” of FR4 trace losses, in addition to programmable common mode voltage and swing for flexible interfacing.

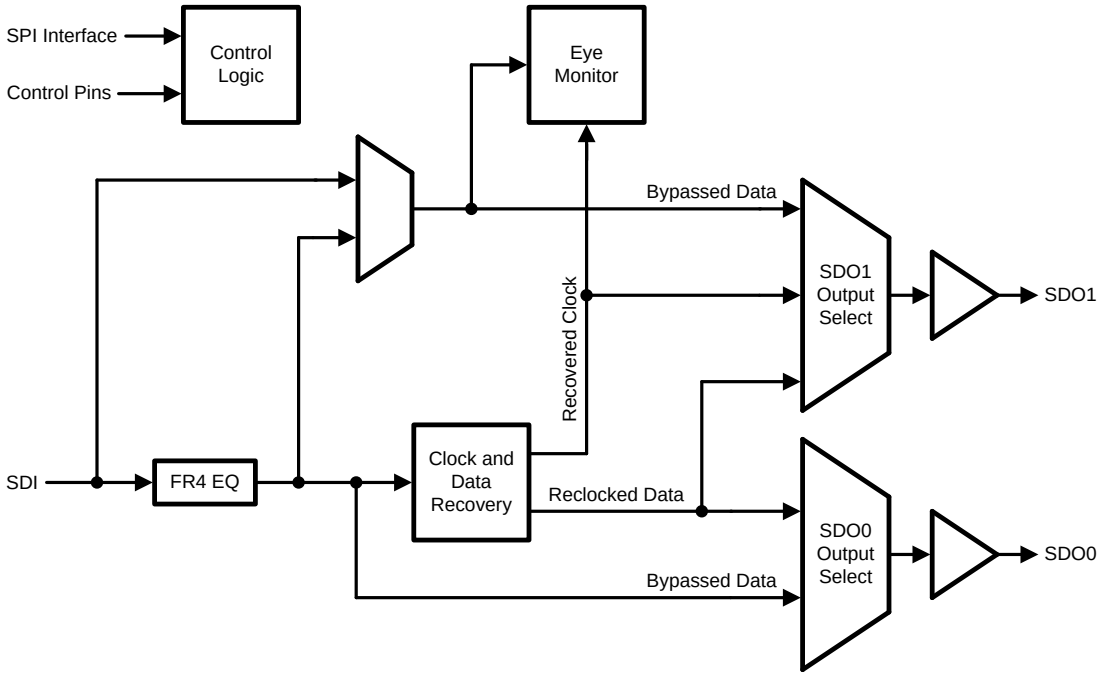
The LMH0366 provides a 64 x 64 point eye monitor for analyzing the eye quality of the incoming signal.

The LMH0366 supports two modes of operation. In pin mode, the LMH0366 operates with control pins to set its operating state. In SPI mode, an optional SPI serial interface can be used to configure and monitor multiple LMH0366 devices in a daisy-chain configuration.

TYPICAL APPLICATION



Block Diagram



Connection Diagram

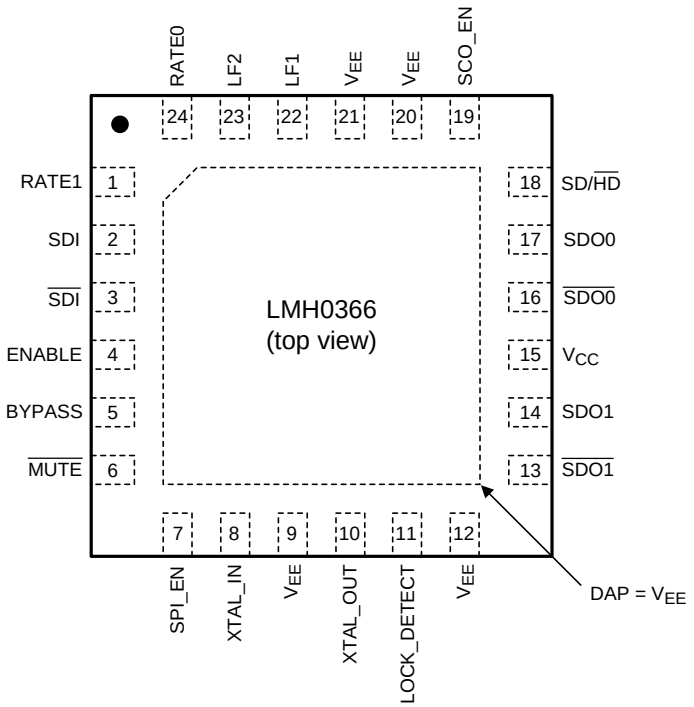
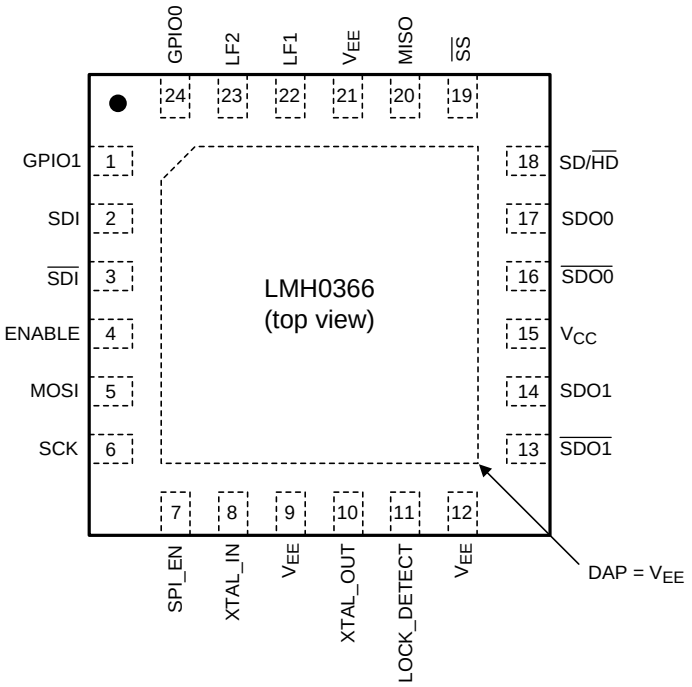


Figure 1. Pin Mode (non-SPI) / SPI_EN = GND



The exposed die attach pad is the primary negative electrical terminal for this device. It must be connected to the negative power supply voltage.

Figure 2. SPI Mode / SPI_EN = V_{CC}
24-Pin
See Package Number RTW0024A

PIN DESCRIPTIONS – PIN MODE (NON-SPI) / SPI_EN = GND

Pin	Name	I/O, Type	Description
1, 24	RATE1, RATE0	I, LVCMOS	Data rate select inputs. RATE0 and RATE1 each has an internal pulldown.
2, 3	SDI, $\overline{SDI}$	I, SDI	Serial data differential input.
4	ENABLE	I, LVCMOS	Device enable. This pin has an internal pullup. H = Device enabled (normal operation). L = Device powered down.
5	BYPASS	I, LVCMOS	Reclocker bypass. This pin has an internal pulldown. H = Reclocking bypassed. L = Normal operation.
6	$\overline{MUTE}$	I, LVCMOS	Output mute. This pin has an internal pullup. H = Normal operation. L = SDO0 and SDO1 outputs are muted.
7	SPI_EN	I, LVCMOS	SPI register access enable. This pin has an internal pulldown. H = SPI register access mode. L = Pin mode.
8	XTAL_IN	I, ANALOG	External crystal or clock input for optional 27 MHz external reference. When not used (i.e. referenceless mode), connect to ground.
10	XTAL_OUT	O, ANALOG	External crystal or clock output.
11	LOCK_DETECT	O, LVCMOS	PLL lock detect status. H = PLL locked. L = PLL not locked.
13, 14	$\overline{SDO1}$, SDO1	O, LVDS	Serial data differential output 1.
16, 17	$\overline{SDO0}$, SDO0	O, LVDS	Serial data differential output 0.
18	SD/$\overline{HD}$	O, LVCMOS	Data rate range indication. H = Locked data rate is SD. L = Locked data rate is 3G or HD (or PLL unlocked).

PIN DESCRIPTIONS – PIN MODE (NON-SPI) / SPI_EN = GND (continued)

Pin	Name	I/O, Type	Description
19	SCO_EN	I, LVCMOS	Serial clock output enable for SDO1. This pin has an internal pulldown. H = SDO1 output is serial clock. L = SDO1 output is serial data.
22, 23	LF1, LF2	I, Analog	Loop filter. Connect a 56 nF capacitor between LF1 and LF2.
15	V_{CC}	Power	Positive power supply (2.5V).
DAP, 9, 12, 20, 21	V_{EE}	Ground	Negative power supply (ground).

PIN DESCRIPTIONS – SPI MODE / SPI_EN = V_{CC}

Pin	Name	I/O, Type	Description
1, 24	GPIO1, GPIO0	I/O, LVCMOS	General purpose input/output pins, selectable via the SPI. Pins 24 and 1 will operate as RATE0 and RATE1 inputs (the same as while in pin mode), with internal pulldowns, unless configured differently via the SPI.
2, 3	SDI, $\overline{\text{SDI}}$	I, SDI	Serial data differential input.
4	ENABLE	I, LVCMOS	Device enable. This pin has an internal pullup. H = Device enabled (normal operation). L = Device powered down.
5	MOSI (SPI)	I, LVCMOS	SPI master output / slave input. LMH0366 data receive. This pin has an internal pullup.
6	SCK (SPI)	I, LVCMOS	SPI serial clock input.
7	SPI_EN	I, LVCMOS	SPI register access enable. This pin has an internal pulldown. H = SPI register access mode. L = Pin mode.
8	XTAL_IN	I, ANALOG	External crystal or clock input for optional 27 MHz external reference. When not used (i.e. referenceless mode), connect to ground.
10	XTAL_OUT	O, ANALOG	External crystal or clock output.
11	LOCK_DETECT	O, LVCMOS	PLL lock detect status. H = PLL locked. L = PLL not locked.
13, 14	$\overline{\text{SDO1}}$, SDO1	O, LVDS	Serial data differential output 1.
16, 17	$\overline{\text{SDO0}}$, SDO0	O, LVDS	Serial data differential output 0.
18	SD/$\overline{\text{HD}}$	O, LVCMOS	Data rate range indication. H = Locked data rate is SD. L = Locked data rate is 3G or HD (or PLL unlocked).
19	$\overline{\text{SS}}$ (SPI)	I, LVCMOS	SPI slave select. This pin has an internal pullup.
20	MISO (SPI)	O, LVCMOS	SPI master input / slave output. LMH0366 data transmit.
22, 23	LF1, LF2	I, Analog	Loop filter. Connect a 56 nF capacitor between LF1 and LF2.
15	V_{CC}	Power	Positive power supply (2.5V).
DAP, 9, 12, 21	V_{EE}	Ground	Negative power supply (ground).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage (V_{CC})	3.1V
Input Voltage (any input)	−0.3V to V_{CC}+0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+125°C
Package Thermal Resistance	
θ_{JA} 24-pin WQFN	42.7°C/W
θ_{JC} 24-pin WQFN	8.7°C/W
ESD Ratings	
HBM (std: JESD22-A114-F)	≥±6 kV
MM (std: JESD22-A115-C)	≥±250V
CDM (std: JESD22-C101-E)	≥±1250V

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device my occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.5V ±5%
Input Voltage	0V to V_{CC}
Operating Free Air Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (1)(2)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{IH}	Input Voltage High Level		Logic inputs	1.7		V_{CC}	V
V_{IL}	Input Voltage Low Level			V_{EE}		0.7	V
I_{IN}	Input Current			−55		55	µA
V_{OH}	Output Voltage High Level	I_{OH} = −2 mA	Logic outputs	2.0			V
V_{OL}	Output Voltage Low Level	I_{OL} = +2 mA				0.2	V
V_{SDID}	Serial Input Voltage, Differential	(3)	SDI	200		1600	mV_{P-P}
V_{CMI}	Input Common Mode Voltage	(3)		0		V_{CC}	V
V_{SSP-P}	Differential Output Voltage, P-P	100Ω load, default register settings (4), Figure 3	SDO0, SDO1	700	800	1000	mV_{P-P}
V_{OD}	Differential Output Voltage			350	400	500	mV_{P-P}
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States					50	mV
V_{OS}	Offset Voltage			1.1	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States					50	mV
I_{OS}	Output Short Circuit Current					30	mA

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{CC} = +2.5V, T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not ensured.
(3) Specification is ensured by characterization and is not tested in production.
(4) The differential output voltage and offset voltage are adjustable via the SPI.

DC Electrical Characteristics (continued)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (1)(2)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
I_{CC}	Supply Current	Normal operation, two output drivers			58	75	mA
		Normal operation, one output driver and low power settings (5)			40	55	mA
		Device disabled (ENABLE = 0)			7	14	mA

(5) Low power mode with one output driver is achieved by powering down the second output driver, setting the amplitude of the active output driver to the lowest setting, disabling input signal detection, and disabling signal detection and equalization for input channels not present on the LMH0366. This can be configured with the following SPI register settings: write "1" to register 0x20 bit 7 (SIG_DET_PRESET) to force the reclocker to assume an input signal is present (so input signal detection can be turned off), write "1" to register 0x11 bit 3 (SDO1_PD) to power down the SDO1 output driver, write "00" to register 0x12 bits 7:6 (SDO0_VOD) to set the SDO0 V_{OD} to 400 mV_{P-P}, and write "11111110" (0xFE) to register 0x15 to power down the input signal detection as well as power down the signal detection and the equalization for input channels not present on the LMH0366.

AC Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DR_{SDI}	Serial Input Data Rate (for reclocking)	MADI	SDI		125		Mbps
		SMPTE ST 259-C, DVB-ASI			270		Mbps
		SMPTE ST 292			1483.5, 1485		Mbps
		SMPTE ST 424			2967, 2970		Mbps
TOL_{JIT}	Serial Input Jitter Tolerance			(3)(4)(5)> 6			UI_{P-P}
		(3) (4) (6)		>0.6			UI_{P-P}
t_{JIT}	Serial Data Output Intrinsic Jitter	270 Mbps (3)	SDO0, SDO1		0.01	0.02	UI_{P-P}
		1483.5 or 1485 Mbps (3)			0.02	0.05	UI_{P-P}
		2967 or 2970 Mbps (3)			0.04	0.1	UI_{P-P}
BW_{LOOP}	Loop Bandwidth	270 Mbps, <0.1dB Peaking			220		kHz
		1485 Mbps, <0.1dB Peaking			0.9		MHz
		2970 Mbps, <0.1dB Peaking			1.7		MHz
F_{CO}	Serial Clock Output Frequency	125 Mbps data rate	SDO1		125		MHz
		270 Mbps data rate			270		MHz
		1483.5 Mbps data rate			1483.5		MHz
		1485 Mbps data rate			1485		MHz
		2967 Mbps data rate			2967		MHz
		2970 Mbps data rate			2970		MHz

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{CC} = +2.5V, T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not ensured.
(3) Specification is ensured by characterization and is not tested in production.
(4) Peak-to-peak amplitude with sinusoidal modulation per SMPTE RP 184-1996 paragraph 4.1. The test data signal shall be color bars.
(5) Refer to "A1" in Figure 1 of SMPTE RP 184-1996.
(6) Refer to "A2" in Figure 1 of SMPTE RP 184-1996.

AC Electrical Characteristics (continued)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
t_{LOCK}	Asynchronous Lock Time	(7)				25	ms
$t_{SYNLOCK}$	Synchronous Lock Time	(8)				1	ms
t_R, t_F	Output Rise/Fall Time	20% – 80%, 100Ω load (3)	SDO0, SDO1		80	130	ps

(7) Time to acquire lock when an input signal is first applied or when the data rate of the input signal is changed. The maximum asynchronous lock time can be improved (decreased) to be less than 15 ms with the following SPI register setting: write 0xA3 to register 0x0E.
(8) Time to reacquire lock after the switch to another input signal at the same data rate as the PLL is currently locked.

AC Electrical Characteristics – SPI

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
Recommended Input Timing Requirements							
f_{SCK}	SCK Frequency		SCK			20	MHz
t_{PH}	SCK Pulse Width High	Figure 4, Figure 5		40			% SCK period
t_{PL}	SCK Pulse Width Low			40			% SCK period
t_{SU}	MOSI Setup Time	Figure 4, Figure 5	MOSI	4			ns
t_H	MOSI Hold Time			4			ns
t_{SSSU}	$\overline{SS}$ Setup Time	Figure 4, Figure 5	$\overline{SS}$	14			ns
t_{SSH}	$\overline{SS}$ Hold Time			4			ns
t_{SSOF}	$\overline{SS}$ Off Time			1			SCK period
Switching Characteristics							
t_{ODZ}	MISO Driven-to-Tristate Time	Figure 5	MISO			20	ns
t_{OZD}	MISO Tristate-to-Driven Time					10	ns
t_{OD}	MISO Output Delay Time					15	ns

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{CC} = +2.5V, T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not ensured.

Timing Diagrams

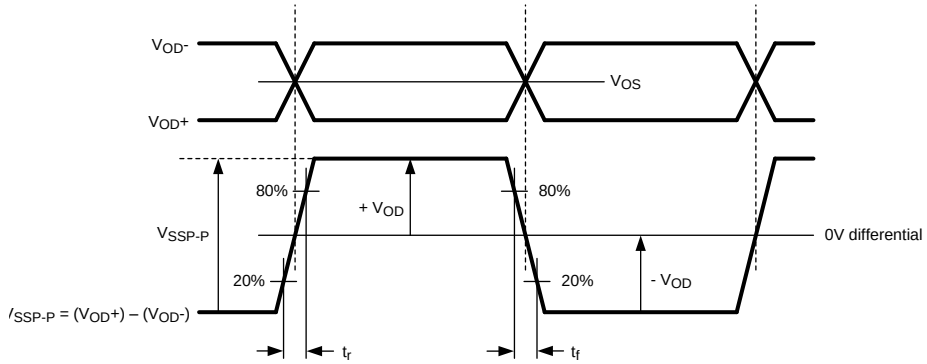


Figure 3. LVDS Output Voltage, Offset, and Timing Parameters

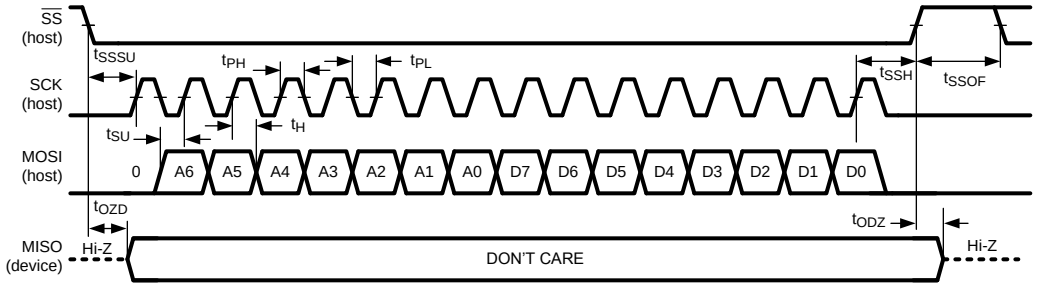


Figure 4. SPI Write

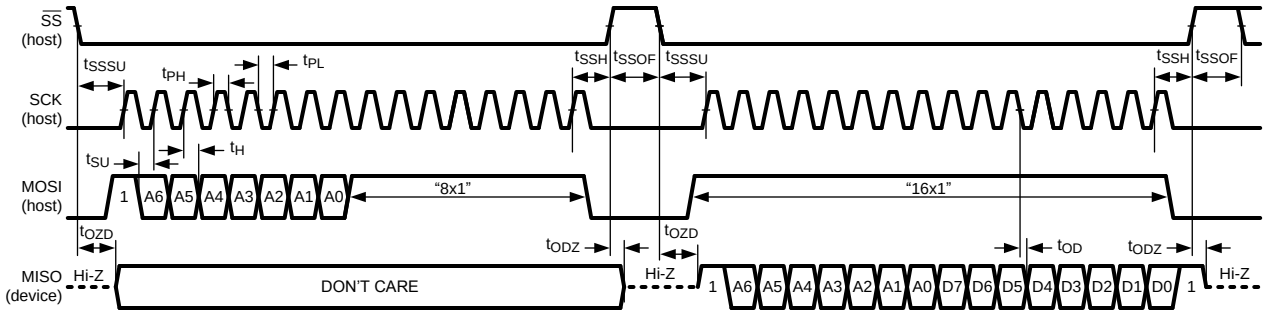


Figure 5. SPI Read

Functional Description

The LMH0366 is a multi-rate reclocker for serial digital video data and operates at 125 Mbps, 270 Mbps, 1.4835 Gbps, 1.485 Gbps, 2.967 Gbps, and 2.97 Gbps. The LMH0366 recovers the serial clock and retimes the serial data stream to suppress accumulated jitter.

Modes of Operation

The LMH0366 has two modes of operation: pin mode (SPI_EN = 0) and SPI mode (SPI_EN = 1).

In pin mode, the LMH0366 functions are controlled by control pins only.

SPI mode allows access to SPI registers for controlling all LMH0366 features, including additional features such as:

- Eye opening monitor
- Output driver amplitude, common mode voltage, and de-emphasis controls
- Input signal detection
- More control over which signals are sent to the output drivers
- Full details of the locked data rate
- Ability to distinguish between 1.4835 and 1.485 Gbps, and between 2.967 and 2.97 Gbps (in external reference mode)
- Ability to configure device pins as GPIOs
- Ability to power down unused features for power savings

The LMH0366 SPI protocol is described in the SPI Register Access section.

Four device pins are dual mode and change functionality depending on whether the device is in pin mode or SPI mode, as indicated in Table 1.

Table 1. Pin Mode vs. SPI Mode Pin Changes

Pin	Pin Mode (SPI_EN = 0)	SPI Mode (SPI_EN = 1)
5	BYPASS	MOSI
6	$\overline{\text{MUTE}}$	SCK
19	SCO_EN	$\overline{\text{SS}}$
20	V_{EE}	MISO

SPI mode provides the ability to configure two device pins as general purpose input/output (GPIO) pins. With default register settings, pins 24 and 1 operate as RATE0 and RATE1. In SPI mode, these pins can be configured as GPIOs (GPIO0 and GPIO1 respectively), but they do not explicitly change function to GPIOs upon entering SPI mode by setting SPI_EN high. These pins will continue to operate as RATE0 and RATE1 until they are optionally configured differently via SPI register writes. Once changed, these pins will continue to operate as GPIOs even after reentering pin mode by setting SPI_EN low.

Serial Data Input

The LMH0366 input has a 100Ω differential internal termination and supports a rail-to-rail input common mode voltage for versatility in DC input coupling. It is intended to be DC coupled to devices such as the LMH0394 adaptive cable equalizer.

The input is equalized and includes signal detection with a programmable threshold, accessible via the SPI.

Input FR4 Equalization

The input includes an FR4 equalizer capable of equalizing up to 60” of FR4 trace.

The FR4 equalizer can be optimized for long trace lengths via the SPI. For input FR4 trace lengths longer than 40”, it is recommended to set register 0x11 bit 1 (EQ_BOOST_60) to enable additional equalizer boost in order to compensate for the longer trace length.

The signal that goes to the eye opening monitor and also to the bypassed data for the SDO1 output can either be equalized or it can bypass the FR4 equalizer (see Block Diagram). By default, this signal is equalized, but register 0x14 bit 1 (MUX2_EQ_SEL) selects between non-equalized or equalized data (before or after the FR4 equalizer) for this signal.

Input Signal Detection

The input includes a signal detect circuit accessible via the SPI. The status of the input signal detection is indicated either by register 0x01 bit 0 (SIG_DET) or register 0x03 bit 4 (SIG_DET).

The signal detection threshold is adjustable via register 0x20 bits 5:3 (SIG_DET_LVL).

The signal detection status can optionally be indicated via the GPIO pins (see the General Purpose Input/Output Pins (GPIO[3:0]) section).

Serial Data Output

The LMH0366 provides two internally terminated 100Ω LVDS outputs: SDO0 and SDO1.

The SDO0 output provides either serial reclocked data or bypassed data. The SDO1 output provides either serial reclocked data, the recovered serial clock, or bypassed data.

The LMH0366 output should be DC coupled to the input of the receiving device where possible. 100Ω transmission lines should be used to connect between the LMH0366 outputs and the input of the receiving device. The LMH0366 output should not be DC coupled to CML inputs. If there are strong pullup resistors (e.g. 50Ω) at the receiving device, AC coupling should be used.

The output driver swing (amplitude), offset voltage (common mode voltage), and de-emphasis level are adjustable via the SPI. In addition, SPI register access allows the signal polarity of the output drivers to be inverted and the output drivers to be independently powered down.

Output Swing (V_{OD})

The default peak-to-peak differential output voltage is 800 mV_{P-P}. The output swing is individually adjustable for the two output drivers via register 0x12 bits 7:6 (SDO0_VOD) and bits 5:4 (SDO1_VOD). The output swing may be selected between 400 mV_{P-P}, 530 mV_{P-P}, 670 mV_{P-P}, and 800 mV_{P-P}.

Offset Voltage (V_{OS})

The default offset voltage is 1.2V. The offset voltage is adjustable via register 0x11 bits 7:6 (SDO_VOS). The offset voltage may be selected between 0.8V, 1.0V, and 1.2V. This setting applies to both the SDO0 and SDO1 output drivers.

Output De-Emphasis

Output de-emphasis compensates for board trace losses. The output driver de-emphasis is turned off (0 dB) by default. The output de-emphasis is individually adjustable for the two output drivers via register 0x13 bits 7:6 (SDO0_DEM) and bits 5:4 (SDO1_DEM). The output de-emphasis may be selected between 0 dB (no-de-emphasis, for driving up to 10” FR4), 3 dB (for driving 10-20” FR4), 5 dB (for driving 20-30” FR4), and 7 dB (for driving 30-40” FR4).

Output Polarity Inversion

The output polarity of both output drivers can be inverted via register 0x11 bit 0 (SDO_INV). This may be useful to preserve the proper signal polarity for polarity sensitive applications (e.g. DVB-ASI) in which the polarity of the reclocker’s input or output signal needs to be swapped for layout reasons.

Output Power Down

The output drivers may be individually powered down via register 0x11 bit 4 (SDO0_PD) and bit 3 (SDO1_PD).

Lock Detect

The lock detect indicates when the reclocker is locked to the incoming data stream. The lock detection status can be monitored by the active-high LOCK_DETECT pin, or by reading register 0x01 bit 4 (LOCK_DET). Note that when the bypass mode is active, lock detect will not assert. See Table 2.

Output Mute

The output mute places the SDO0 and SDO1 outputs into the muted state. When muted, the outputs will be forced to a logic 0. The output mute has precedence over the bypass mode. See Table 2.

In pin mode, the output mute is controlled by the active-low $\overline{\text{MUTE}}$ pin. The $\overline{\text{MUTE}}$ pin has an internal pullup to enable the outputs by default.

In SPI mode, the output mute is controlled by register 0x12 bit 1 ($\overline{\text{MUTE}}$), as long as manual output selection is not enabled (i.e. as long as register 0x09 bit 5, PIN_MODE_OV, remains cleared). The muted state of the output drivers can be changed via register 0x14 bit 7 (MUTE_STATE) so that, when muted, the outputs are forced to a logic 1 instead of a logic 0.

Bypass Mode

The bypass mode forces the reclocker to output the serial data without reclocking it. In bypass mode, bypassed (non-reclocked) data will be present on both the SDO0 and SDO1 outputs (unless SDO1 is configured for the serial clock, in which case the SDO1 output will be muted). When not in bypass mode, the reclocker will still automatically bypass the reclocking function when the detected data rate is a rate which the device does not support. Note that when the bypass mode is active, lock detect will not assert. See Table 2.

In pin mode, the bypass mode is controlled by the active-high BYPASS pin. The BYPASS pin has an internal pulldown to disable reclocker bypassing by default.

In SPI mode, the bypass mode is controlled by register 0x12 bit 2 (BYPASS). Note that the eye opening monitor is not operational while the bypass mode is enabled.

Serial Clock Output Enable (SCO_EN)

The serial clock output enable (SCO_EN) controls whether the SDO1 output is the serial clock or data. When SCO_EN is asserted, the SDO1 output will be the recovered serial clock. If the SDO1 output is configured for the serial clock and either bypass mode is activated or the PLL lock is lost, then the SDO1 output will be muted. See Table 2.

In pin mode, this function is controlled by the active-high SCO_EN pin. The SCO_EN pin has an internal pulldown to configure the SDO1 output as serial data by default.

In SPI mode, this function is controlled by register 0x12 bit 0 (SCO_EN), as long as manual output selection is not enabled (i.e. as long as register 0x09 bit 5, PIN_MODE_OV, remains cleared).

Table 2. SDO0 and SDO1 Output Configuration Based on $\overline{\text{MUTE}}$, BYPASS, SCO_EN and LOCK DETECT

$\overline{\text{MUTE}}$	BYPASS	SCO_EN	LOCK DETECT	SDO0 Output	SDO1 Output
0	X	X	X	Muted	Muted
1	1	0	0	Bypassed data	Bypassed data
1	1	1	0	Bypassed data	Muted
1	0	0	0	Bypassed data	Bypassed data
1	0	1	0	Bypassed data	Muted
1	0	0	1	Reclocked data	Reclocked data
1	0	1	1	Reclocked data	Recovered clock

Manual Output Selection

In pin mode and in SPI mode with default register settings, the SDO0 and SDO1 outputs are configured by the BYPASS, $\overline{\text{MUTE}}$, and SCO_EN functions according to Table 2. (In pin mode, these functions are controlled by the BYPASS, $\overline{\text{MUTE}}$, and SCO_EN pins, and in SPI mode, these functions are controlled by register 0x12 bits 2:0.)

SPI register access allows the SDO0 and SDO1 outputs to be manually selected instead of using the BYPASS, MUTE, and SCO_EN functions. Upon entering SPI mode, the SDO0 and SDO1 outputs will be configured by register 0x12 bits 2:0 (BYPASS, MUTE, and SCO_EN). Register 0x09 bit 5 (PIN_MODE_OV) can be used to override this control and choose manual SDO0 and SDO1 output selection. Once this override bit is set, then register 0x1E bits 6:5 (SDO0_SEL) select the output for SDO0 according to Table 3, and register 0x1E bits 4:3 (SDO1_SEL) select the output for SDO1 according to Table 4. Note that register 0x09 bit 5 (PIN_MODE_OV) overrides the use of register 0x12 bits 1:0 (MUTE and SCO_EN), but register 0x12 bit 2 (BYPASS), will still operate and can be used to bypass reclocking for both outputs.

Table 3. SDO0 Manual Output Selection (via Register 0x1E bits 6:5)

SDO0_SEL[1:0]	SDO0 Output	
	Lock Detect = 1	Lock Detect = 0
00	Reclocked data	Bypassed data
01	Bypassed data	Bypassed data
10	Muted	Muted
11	Reclocked data	Bypassed data

Table 4. SDO1 Manual Output Selection (via Register 0x1E bits 4:3)

SDO1_SEL[1:0]	SDO1 Output	
	Lock Detect = 1	Lock Detect = 0
00	Recovered clock	Muted
01	Reclocked data	Bypassed data
10	Muted	Muted
11	Bypassed data	Bypassed data

Data Rate Selection

The LMH0366 can be configured for automatic or manual rate selection, which is controlled either by the RATE0 and RATE1 pins or through SPI register access. With default register settings, the RATE0 and RATE1 pins select the allowable rates at which the reclocker will lock, as shown in Table 5. The RATE0 and RATE1 pins have internal pulldowns to select auto-rate detect by default.

Table 5. Data Rate Selection

RATE1	RATE0	Selected Rate or Mode
0	0	Auto-rate detect – video rates (270, 1483.5, 1485, 2967, 2970 Mbps)
0	1	270 Mbps
1	0	1483.5/1485 Mbps, 2967/2970 Mbps
1	1	125 Mbps

Upon entering SPI mode, the RATE pins will continue to select the allowable rates at which the reclocker will lock. Setting register 0x1D bit 0 (RATE_SEL_OV) overrides this selection and allows the rate selection to be controlled by register 0x1C bits 1:0 (RATE_SEL) instead of the RATE pins. (This frees up the RATE0 and RATE1 pins to be used as GPIOs since they are no longer needed for rate selection.)

External Clock Reference or Referenceless Mode

The LMH0366 can operate with an external 27 MHz crystal or external clock signal as a timing reference input (external reference mode), or it can operate with no reference at all (referenceless mode). Providing an external 27 MHz reference allows the LMH0366 to distinguish between 2.97 Gbps and 2.97/1.001 Gbps, and between 1.485 Gbps and 1.485/1.001 Gbps. This reference could be a 27 MHz parallel resonant crystal and load network connected to the XTAL_IN and XTAL_OUT pins, or a 27 MHz 2.5V LVCMOS compatible clock signal connected to XTAL_IN. The LMH0366 will automatically detect the 27 MHz reference clock and indicate its presence via register 0x41 bit 3 (REF_CLK_DET).

When using the LMH0366 in referenceless mode (i.e. no external 27 MHz crystal or reference clock applied), the XTAL_IN pin must be connected to ground (V_{EE}).

Parameters for a suitable crystal are given in Table 6. A single crystal can be used as the 27 MHz reference for multiple reclockers by connecting the XTAL_OUT output of one reclocker to the XTAL_IN input of the next , propagating the 27 MHz reference signal through a cascade of reclockers.

Table 6. Recommended Crystal Parameters

Parameter	Value
Frequency	27 MHz
Frequency Stability	±50 ppm @ Recommended Drive Level
Operating Mode	Fundamental Mode, Parallel Resonant
Load Capacitance	20 pF
Shunt Capacitance	7 pF
Series Resistance	40Ω max
Recommended Drive Level	100 µW
Maximum Drive Level	250 µW
Operating Temperature Range	−10°C to +60°C

SD/$\overline{HD}$ Indication

The SD/$\overline{HD}$ output indicates whether the LMH0366 is processing SD or HD/3G data rates. It may be used to control the slew rate of another device such as the LMH0303 cable driver. This output is high when the data rate is 270 Mbps, and this output is low for all other data rates. When the PLL is not locked (the LOCK_DETECT output is low), the SD/$\overline{HD}$ output is low.

Data Rate Indication

Details about the currently locked data rate can be obtained via the SPI. Register 0x03 bits 7:5 (RATE_STATUS) indicate the locked data rate according to Table 7.

The LMH0366 will detect the presence of a 27 MHz reference clock on the XTAL_IN pin (register 0x41 bit 3, REF_CLK_DET, indicates the presence of the reference clock). When using an external reference, the LMH0366 can distinguish between 1.4835 and 1.485 Gbps, and between 2.967 and 2.97 Gbps. This is indicated in the RATE_STATUS register bits. Also, when the reference clock is present, register 0x41 bit 2 (RATE_1_OV_M) indicates if the detected data rate is a 1 over M rate (1.485/1.001 or 2.97/1.001 Gbps).

Table 7. Data Rate Indication (via Register 0x03 bits 7:5)

RATE_STATUS[2:0]	Data Rate Indication	
	External Reference Mode	Referenceless Mode
000	125 Mbps	125 Mbps
001	270 Mbps	270 Mpbs
010	1.4835 Gbps	N/A
011	1.485 Gbps	1.485 or 1.4835 Gbps
100	2.967 Gbps	N/A
101	2.97 Gbps	2.97 or 2.967 Gbps
111	Unlocked	Unlocked

Loop Filter

The reclocker uses an external loop filter, which consists of a 56 nF capacitor connected between the LF1 and LF2 pins.

Enable

The ENABLE input is used to enable or disable the LMH0366. Disabling the device powers down the output drivers and most of the internal circuitry in order to minimize the power dissipation. While in the disabled state, the SPI and input signal detection remain active. The external clock reference circuitry (XTAL_IN and XTAL_OUT) also remains active, allowing the 27 MHz reference clock signal to be generated and passed on to additional reclockers. ENABLE is active high and this pin has an internal pullup to enable the LMH0366 by default.

General Purpose Input/Output Pins (GPIO[3:0])

The LMH0366 has two pins that can be configured through the SPI to provide direct access to certain register values via a dedicated pin. For example, if a particular application requires fast access to the condition of losing the input signal to the reclocker, the signal detect status bit could be routed directly to an external pin where it might generate an interrupt for the host processor. The GPIO pins can be configured as inputs or outputs. When used as inputs, the GPIO pins can be configured with a pullup resistor, a pulldown resistor, or no biasing at all.

The two GPIO pins, pins 24 and 1, originally function as the RATE0 and RATE1 inputs, respectively. To use these pins as GPIOs, their default functions must first be overridden. Setting register 0x1D bit 0 (RATE_SEL_OV) overrides the use of these pins as RATE0 and RATE1 and allows the rate selection to be controlled by register 0x1C bits 1:0 (RATE_SEL), freeing pins 24 and 1 to be used as GPIO0 and GPIO1.

The two GPIO pins are controlled by registers 0x04 (GPIO0 Control) and 0x05 (GPIO1 Control).

For each of these GPIO control registers, bits 7:4 control the output mode, and can select between general purpose output and signal detect. When the GPIO is configured as an input, this mode selection has no effect.

Bits 3 and 2 select either a pullup or pulldown resistor for when the GPIO is operating as an input. Do not enable the pullup and pulldown resistor simultaneously. When the GPIO is operating as an output, neither the pullup nor the pulldown resistor should be enabled.

Bits 1 and 0 enable or disable the input and output buffers. If the GPIO is used as an output, the output buffer must be enabled and the input buffer must be disabled. If the GPIO is used as an input, the input buffer must be enabled and the output must be disabled. Do not enable both the input and output buffers simultaneously.

If the GPIO pins are configured as inputs, then the input values on each of the four GPIOs can be monitored via register 0x03 bits 1:0 (GPIO_IN_VAL). If the GPIO pins are configured as general purpose output pins, then the values written to register 0x08 bits 1:0 (GPIO_OUT_VAL) will appear on the respective GPIO pins.

Eye Opening Monitor (EOM)

The LMH0366 includes an eye opening monitor for analyzing the quality of the incoming signal, accessible via the SPI. It analyzes the eye opening with 64 horizontal time points and 64 vertical voltage points, with 6-bit phase DAC control for the horizontal coordinates and 6-bit voltage DAC control for the vertical coordinates.

The eye opening monitor can be used to measure the eye shape using either the normal or fast EOM modes. It can also be used to quickly determine the width and height of the eye opening.

Eye Opening Monitor Configuration

For all modes, the eye opening monitor must first be enabled by clearing register 0x14 bit 4 (EOM_PD).

The LMH0366 must be locked to the incoming data rate for eye opening monitor operation.

The input signal to the eye opening monitor is equalized by default, but register 0x14 bit 1 (MUX2_EQ_SEL) can be used to select between non-equalized or equalized data.

The output eye monitor is configured for HD input signals by default. When analyzing SD input signals, it is recommended to set register 0x11 bit 2 (EOM_SEL_SD) to enable SD eye monitor mode. For 3G input signals, it is recommended to set register 0x22 bit 6 (EOM_SEL_3G) to enable 3G eye monitor mode.

The amount of time during which the eye opening monitor accumulates eye opening data can be set by the value in register 0x29 (EOM_TIMER). In general, the greater this value, the longer the accumulation time.

Normal Eye Opening Monitor Mode

In normal eye opening monitor mode, the external controller has full control over the horizontal and vertical coordinates, and must enable the measurement for each point. This provides the option to do a more coarse measurement.

The procedure for normal EOM mode is as follows:

1. Enable the eye opening monitor by clearing register 0x14 bit 4 (EOM_PD).
2. Enable manual operation of the phase DAC and voltage DAC by setting register 0x22 bit 7 (EOM_OV).
3. Write the 6-bit phase DAC value to register 0x22 bits 5:0 (EOM_PDAC), and write the 6-bit voltage DAC value to register 0x23 bits 5:0 (EOM_VDAC).
4. Enable the EOM counter by setting register 0x24 bit 0 (EOM_START), and poll for completion of the measurement by reading this bit until it has cleared itself.
5. Read register 0x25 (EOM_COUNT[15:8]) to get the most significant byte and register 0x26 (EOM_COUNT[7:0]) to get the least significant byte of the hits counter, and store this value.
6. Repeat steps 3-5 for the remaining desired phase DAC and voltage DAC points. (In a typical application, steps 2-4 will be repeated by sweeping through every voltage DAC setting at each phase DAC setting.)

Fast Eye Opening Monitor Mode

In fast eye opening monitor mode, the eye opening monitor sweeps through all 4096 phase and voltage DAC settings autonomously. A new measurement at the next coordinate is automatically triggered when the current 16-bit count is ready and has been read. The full 64-by-64 point dimensions are used in this mode.

The procedure for fast EOM mode is as follows:

1. Enable the eye opening monitor by clearing register 0x14 bit 4 (EOM_PD).
2. Enable fast EOM mode by setting register 0x24 bit 7 (FAST_EOM).
3. Read register 0x26 (EOM_COUNT[7:0]) to clear the initial invalid data and start the EOM counter, and poll for completion of the measurement by reading register 0x24 bit 0 (EOM_START) until it has cleared itself.
4. Read register 0x26 again to load the hits counter for read back and start the next measurement.
5. Poll for completion of the measurement by reading register 0x24 bit 0 (EOM_START) until it has cleared itself.
6. Read register 0x25 (EOM_COUNT[15:8]) to get the most significant byte and register 0x26 (EOM_COUNT[7:0]) to get the least significant byte of the hits counter, and store this value. (Reading register 0x26 will also automatically step to the next point in the EOM graph and initiate the measurement.)
7. Repeat steps 5-6 a total of 4096 times.

Measuring Horizontal and Vertical Eye Openings

The eye opening monitor can quickly detect and report the horizontal eye opening (HEO) and vertical eye opening (VEO). The eye opening monitor first sweeps its variable-phase clock through one unit interval with the comparison voltage set to the midpoint of the signal. This determines the midpoint of the horizontal eye opening. The eye opening monitor then sets its variable-phase clock to the midpoint of the horizontal eye opening and sweeps its comparison voltage. These two measurements determine the horizontal and vertical eye openings.

The procedure to measure the horizontal and vertical eye openings is as follows:

1. Enable the eye opening monitor by clearing register 0x14 bit 4 (EOM_PD).
2. Enable the measurement by setting register 0x24 bit 1 (GET_HEO_VEO), and wait for completion by reading this bit until it has cleared itself.
3. Ensure no errors have occurred by verifying that register 0x24 bits 4:2 (VEO_MAX_ERR, NO_OPENING_ERR, and NO_HITS_ERR) are all cleared.
4. Read the horizontal eye opening in register 0x2A (HEO) and the vertical eye opening in register 0x2B (VEO).

SPI Register Access

Setting SPI_EN high enables the optional SPI register access mode. The LMH0366 supports SPI daisy-chaining among an unlimited number of LMH0366 devices. With SPI_EN set low, the device operates in pin mode.

Table 8 shows the SPI register table for the LMH0366. The LMH0366 provides over 50 accessible registers, which are divided into over 100 bit fields. When writing to the device registers, it is important to ensure that reserved register values are not changed.

In configuring the LMH0366, it is often required to write to a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register.

When power is first applied to the LMH0366, the host must wait 500 ms to ensure the power-on reset has competed before initiating SPI transactions.

SPI Transaction Overview

Each SPI transaction to a single device is 16-bits long. The transaction is initiated by driving $\overline{SS}$ low, and completed by returning $\overline{SS}$ high. The 16-bit MOSI payload consists of the read/write command (“1” for reads and “0” for writes), the seven address bits of the device register (MSB first), and the eight data bits (MSB first). The LMH0366 MOSI input data is latched on the rising edge of SCK, and the MISO output data is sourced on the falling edge of SCK.

In order to facilitate daisy-chaining, the prior SPI command, address, and data are shifted out on the MISO output as the current command, address, and data are shifted in on the MOSI input. For SPI writes, the MISO output is typically ignored as “Don't Care” data. For SPI reads, the MISO output provides the requested read data (after 16 periods of SCK). The MISO output is active when $\overline{SS}$ low, and tri-stated when $\overline{SS}$ is high.

SPI Write

The SPI write is shown in Figure 4. The SPI write is 16 bits long. The 16-bit MOSI payload consists of a “0” (write command), seven address bits, and eight data bits. The $\overline{SS}$ signal is driven low, and the 16 bits are sent to the LMH0366's MOSI input. After the SPI write, $\overline{SS}$ must return high. The prior SPI command, address, and data shifted out on the MISO output during the SPI write is shown as “Don't Care” on the MISO output in Figure 4.

SPI Read

The SPI read is shown in Figure 5. The SPI read is 32 bits long, consisting of a 16-bit read transaction followed by a 16-bit dummy read transaction to shift out the read data on the MISO output. The first 16-bit MOSI payload consists of a “1” (read command), seven address bits, and eight “1”s which are ignored. The second 16-bit MOSI payload consists of 16 “1”s which are ignored but necessary in order to shift out the requested read data on the MISO output. The $\overline{SS}$ signal is driven low, and the first 16 bits are sent to the LMH0366's MOSI input. The prior SPI command, address, and data are shifted out on the MISO output during the first 16-bit transaction, and are typically ignored (this is shown as “Don't Care” on the MISO output in Figure 5. $\overline{SS}$ must return high and then is driven low again before the second 16 bits (all “1”s) are sent to the LMH0366's MOSI input. Once again, the prior SPI command, address, and data are shifted out on the MISO output, but this data now includes the requested read data. The read data is available on the MISO output during the second 8 bits of the 16-bit dummy read transaction, as shown by D7-D0 in Figure 5.

SPI Daisy-Chain Operation

The LMH0366 SPI controller supports daisy-chaining the serial data between an unlimited number of LMH0366 devices. Each LMH0366 device is directly connected to the SCK and $\overline{SS}$ pins on the host. However, only the first LMH0366 device in the chain is connected to the host’s MOSI pin, and only the last device in the chain is connected to the host’s MISO pin. The MISO pin of each intermediate LMH0366 device in the chain is connected to the MOSI pin of the next LMH0366 device, creating a serial shift register. This daisy-chain architecture is shown in Figure 6.

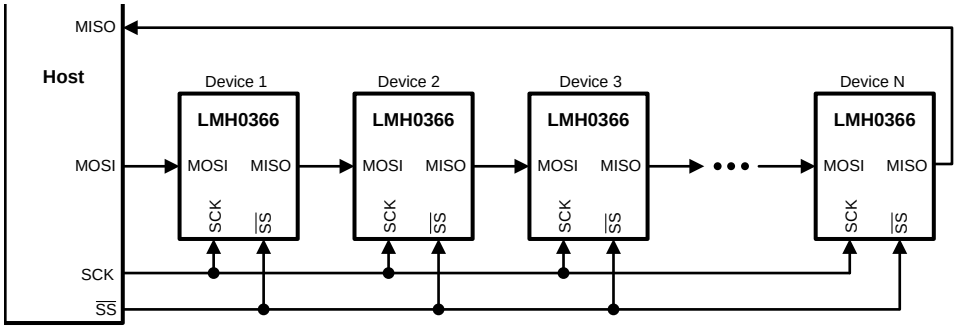


Figure 6. SPI Daisy Chain System Architecture

In a daisy-chain configuration of N LMH0366 devices, the host conceptually sees a shift register of length 16xN. Therefore the length of SPI transactions (as previously described) is 16xN bits, and $\overline{SS}$ must be asserted for 16xN clock cycles for each SPI transaction.

SPI Daisy-Chain Write

Figure 7 shows the SPI daisy-chain write for a daisy-chain of N devices. The $\overline{SS}$ signal is driven low and SCK is toggled for 16xN clocks. The 16xN bit MOSI payload (sent to Device 1 in the daisy-chain) consists of the 16-bit SPI write data for Device N (the last device in the chain), followed by the write data for Device N-1, Device N-2, etc., ending with the write data for Device 1 (the first device in the chain). The 16-bit SPI write data for each device consists of a "0" (write command), seven address bits, and eight data bits. After the SPI daisy-chain write, $\overline{SS}$ must return high and then the write occurs for all devices in the daisy-chain.

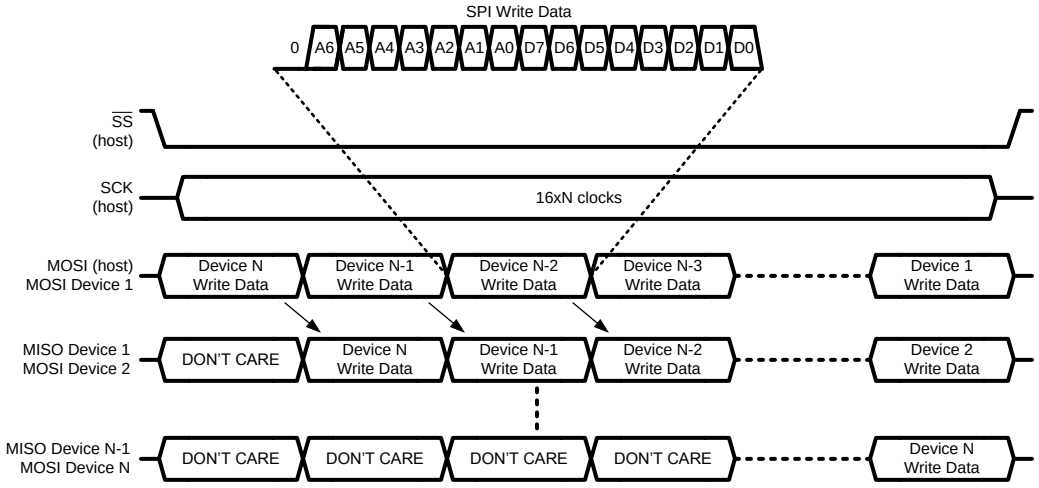


Figure 7. SPI Daisy-Chain Write

SPI Daisy-Chain Read

Figure 8 shows the SPI daisy-chain read for a daisy-chain of N devices. The SPI daisy-chain read is 32xN bits long, consisting of 16xN bits for the read transaction followed by 16xN bits for the dummy read transaction (all "1"s) to shift out the read data on the MISO output. The $\overline{SS}$ signal is driven low and SCK is toggled for 16xN clocks. The first 16xN bit MOSI payload (sent to Device 1 in the daisy-chain) consists of the 16-bit SPI read data for Device N (the last device in the chain), followed by the read data for Device N-1, Device N-2, etc., ending with the read data for Device 1 (the first device in the chain). The 16-bit SPI read data for each device consists of a "1" (read command), seven address bits, and eight "1"s (which are ignored). After the first 16xN bit transaction, $\overline{SS}$ must return high (to latch the data) and then is driven low again before the second 16xN bit transaction of all "1"s is sent to the MOSI input. The requested read data is shifted out on MISO starting with the data for Device N and ending with the data for Device 1. After this transaction, $\overline{SS}$ must return high.

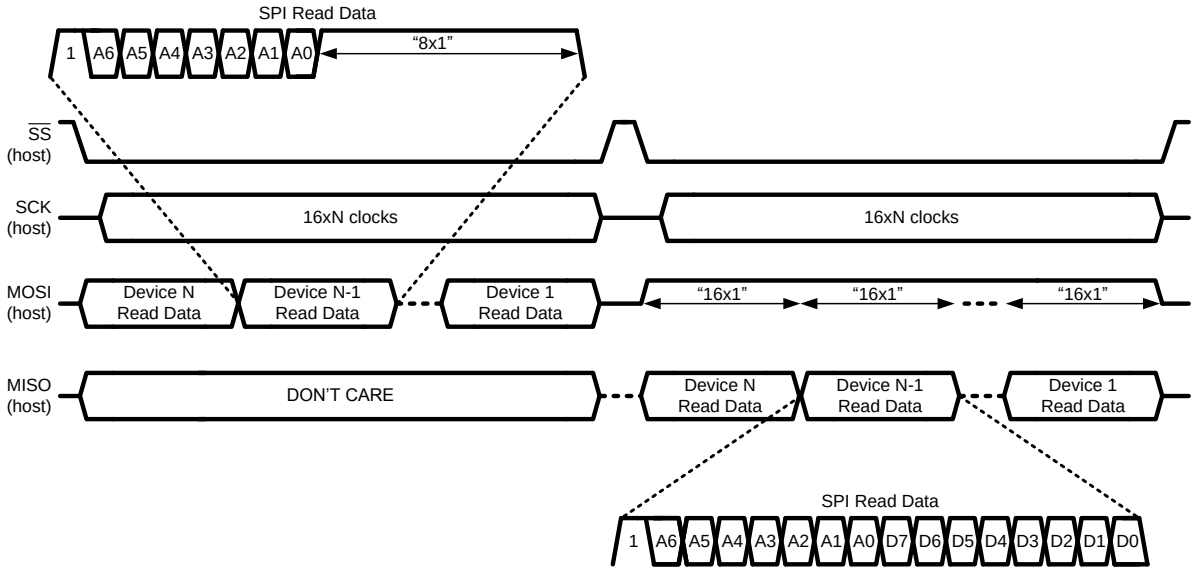


Figure 8. SPI Daisy-Chain Read

SPI Daisy-Chain Read and Write Example

The following example further clarifies LMH0366 SPI daisy-chain operation. Assume a daisy-chain of three LMH0366 devices (Device 1, Device 2, and Device 3), with Device 1 as the first device in the chain and Device 3 as the last device in the chain, as shown by the first three devices in Figure 6. Since there are three devices in the daisy-chain, each SPI transaction is 48-bits long.

This example shows an SPI operation combining SPI reads and writes in order to accomplish the following three tasks:

1. Write 0x02 to register 0x12 of Device 1 in order to set the output swing of both SDO0 and SDO1 to 400 mV_{P-P}.
2. Read the contents of register 0x01 of Device 2.
3. Write 0x50 to register 0x13 of Device 3 in order to set the output de-emphasis of both SDO0 and SDO1 to 3 dB.

Figure 9 shows the two 48-bit SPI transactions required to complete these tasks (the bits are shifted in left to right).

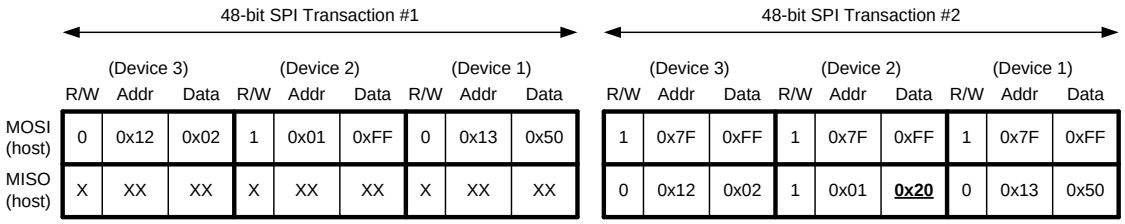


Figure 9. SPI Daisy-Chain Read and Write Example

The following occurs at the end of the first transaction:

1. Write 0x02 to register 0x12 of Device 1.
2. Latch the data from register 0x01 of Device 2.
3. Write 0x50 to register 0x13 of Device 3.

In the second transaction, three dummy reads (each consisting of 16 "1"s) are shifted in, and the read data from Device 2 (with value 0x20) appears on MISO in the 25th through 32nd clock cycles.

SPI Daisy-Chain Length Detection

A useful operation for the host may be to detect the length of the daisy-chain. This is a simple matter of shifting in a series of dummy reads with a known data value (such as 0x5A). For an SPI daisy-chain of N LMH0366 devices, the known data value will appear on the host's MISO pin after N+1 writes. Assuming a daisy-chain of three LMH0366 devices, the result of this operation is shown in Figure 10.

	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data
MOSI (host)	1	0x7F	0x5A	1	0x7F	0x5A	1	0x7F	0x5A	1	0x7F	0x5A
MISO (host)	X	XX	XX	X	XX	XX	X	XX	XX	**1**	**0x7F**	**0x5A**

Figure 10. SPI Daisy-Chain Length Detection

APPLICATION INFORMATION

Application Circuit (Pin Mode)

Figure 11 shows the typical application circuit for the LMH0366 in pin mode.

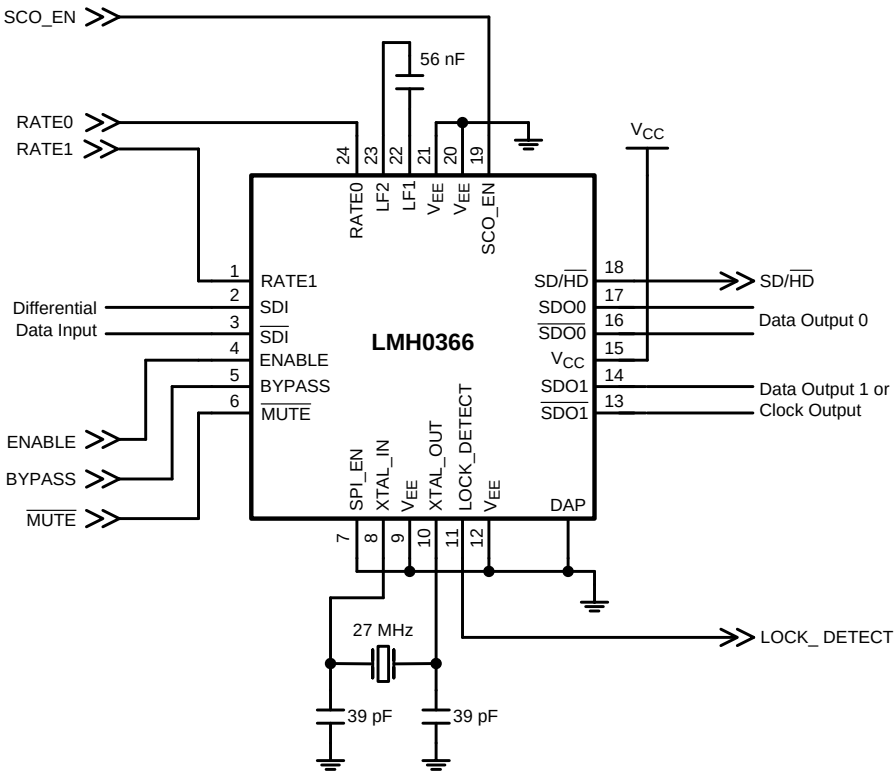


Figure 11. Application Circuit (Pin Mode)

Power Supply Recommendations

The LMH0366 requires a single 2.5V power supply. Circuit board layout and stack-up for the LMH0366 should be optimized to minimize noise to the device from switching power supplies or nearby high speed devices.

It is recommended to provide power to the LMH0366 using a linear regulator. If a switching regulator used, the power supply filtering must be adequate to filter the switching noise.

The following guidelines are recommended for supplying power to the LMH0366:

- Bypass/decouple each supply pin with a high frequency ceramic bypass capacitor (0.01 µF to 0.1 µF) placed as close as possible to the pin.
- Deploy nearby bulk capacitors (2.2 µF to 22 µF) for additional power supply filtering.
- Wherever possible, use two vias for each connection to internal power and ground planes to minimize the via parasitics.
- Use the capacitance of the power-ground system for extra bypassing by using thin dielectrics between the power and ground planes.
- Route high speed differential lines away from the device power pins to avoid coupling noise into the power supply lines.

Loop Filter Recommendations

The LMH0366 uses a 56 nF capacitor for the loop filter, connected between the LF1 and LF2 pins. Alternately, a 47 nF capacitor may be used in place of this 56 nF capacitor.

The loop filter layout should be optimized to minimize coupling between the loop filters of different devices and also to avoid noise pick up from other signals. The external loop filter capacitor should be connected as close to the device pins as possible and with maximum isolation from other signals.

It is important to keep multiple reclockers as isolated from one another as possible to avoid any interaction between the loop filters or other sensitive circuits.

The following guidelines are recommended for the loop filter layout:

- Keep the loop filter traces as short as possible; place the loop filter capacitor parallel to the device to allow for the shortest trace interconnect.
- Avoid using vias between the loop filter pins and the external loop filter capacitor.
- Remove the ground plane underneath the LF1 and LF2 pins and also in the area underneath the loop filter capacitor to increase isolation.
- Avoid running traces under the loop filter area as much as possible to increase isolation.
- When using multiple devices, place the devices as far apart from one another as possible. Avoid placing the loop filter pins of different devices next to each other.

Interfacing to 3.3V SPI

The LMH0366 may be controlled via optional SPI register access. The LMH0366 SPI pins support 2.5V LVCMOS logic levels and are compliant with JEDEC JESD8-5. Care must be taken when interfacing the SPI pins to other voltage levels.

The 2.5V LMH0366 SPI pins may be interfaced to a 3.3V compliant SPI host by using a voltage divider or level translator. One implementation is a simple resistive voltage divider as shown in Figure 12.

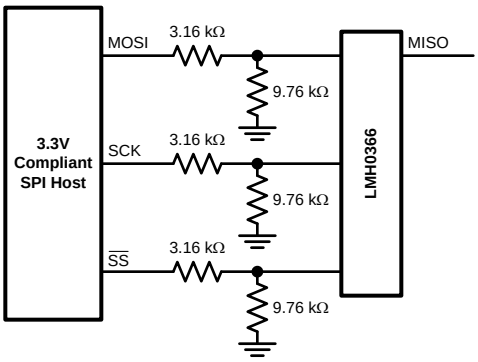


Figure 12. 3.3V SPI Interfacing

SPI Registers

Table 8. SPI Registers

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
00	Reset	7:1	RSVD	R/W	0000000	Reserved.
		0	RESET	R/W	0	Reset registers. (This bit is self-clearing.) 0: Normal operation. 1: Reset all registers to default values.
01	Device Status 1	7:5	REV_ID	R	011	Die revision.
		4	LOCK_DET	R		Lock detect. 0: Reclocker unlocked. 1: Reclocker locked.
		3:1	RSVD	R		Reserved.
		0	SIG_DET	R		Signal detect on SDI. 0: No signal detected. 1: Signal detected.
02	Reserved	7:0	RSVD	R		Reserved.
03	Device Status 2	7:5	RATE_STATUS	R		Locked data rate indication. 000: 125 Mbps. 001: 270 Mbps. 010: 1.4835 Gbps (external reference mode). 011: 1.485 Gbps (includes 1.4835 Gbps in referenceless mode). 100: 2.967 Gbps (external reference mode). 101: 2.97 Gbps (includes 2.967 Gbps in referenceless mode). 111: Unlocked.
		4	SIG_DET	R		Signal detect on SDI. 0: No signal detected. 1: Signal detected.
		3:2	RSVD	R		Reserved.
		1	GPIO1_IN_VAL	R		GPIO1 input value.
		0	GPIO0_IN_VAL	R		GPIO0 input value.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
04	GPIO0 Control	7:4	GPIO0_MODE	R/W	0000	0000: General purpose output 0. 0001: Signal detect for SDI. All others: Reserved.
		3	GPIO0_PU_EN	R/W	0	GPIO0 pullup enable. 0: Disable pullup resistor. 1: Enable pullup resistor. (1)
		2	GPIO0_PD_EN	R/W	1	GPIO0 pulldown enable. 0: Disable pulldown resistor. 1: Enable pulldown resistor. (1)
		1	GPIO0_IN_EN	R/W	1	GPIO0 input enable. 0: Input disabled (always reads 0). 1: Input enabled.
		0	GPIO0_OUT_EN	R/W	0	GPIO0 output enable. 0: Output disabled (tristate). 1: Output enabled.
05	GPIO1 Control	7:4	GPIO1_MODE	R/W	0000	0000: General purpose output 1. All others: Reserved.
		3	GPIO1_PU_EN	R/W	0	GPIO1 pullup enable. 0: Disable pullup resistor. 1: Enable pullup resistor. (1)
		2	GPIO1_PD_EN	R/W	1	GPIO1 pulldown enable. 0: Disable pulldown resistor. 1: Enable pulldown resistor. (1)
		1	GPIO1_IN_EN	R/W	1	GPIO1 input enable. 0: Input disabled (always reads 0). 1: Input enabled.
		0	GPIO1_OUT_EN	R/W	0	GPIO1 output enable. 0: Output disabled (tristate). 1: Output enabled.
06	Reserved	7:0	RSVD	R/W	00000110	Reserved.
07	Reserved	7:0	RSVD	R/W	00000110	Reserved.
08	GPIO Output Control	7:2	RSVD	R/W	001000	Reserved.
		1	GPIO1_OUT_VAL	R/W	0	Output value on GPIO1.
		0	GPIO0_OUT_VAL	R/W	0	Output value on GPIO0.
09	Output Select	7:6	RSVD	R/W	00	Reserved.
		5	PIN_MODE_OV	R/W	0	Pin override (manual mode) for SDO0 and SDO1 output selection. 0: Normal operation. SDO0 and SDO1 outputs are controlled by register 0x12 bits 2:0 (BYPASS, MUTE, and SCO_EN). 1: Use values in register 0x1E bits 6:3 (SDO0_SEL and SDO1_SEL) to manually select SDO0 and SDO1. (Values in register 0x12 bits 1:0 have no effect in this mode.)
		4:0	RSVD	R/W	00010	Reserved.
0A	Reserved	7:0	RSVD	R/W	10010000	Reserved.
0B	Reserved	7:0	RSVD	R/W	00000100	Reserved.

(1) Do not enable the pullup and pulldown resistors simultaneously.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
0C	Reserved	7:0	RSVD	R/W	00001100	Reserved.
0D	Reserved	7:0	RSVD	R/W	00100000	Reserved.
0E	Reserved	7:0	RSVD	R/W	10111011	Reserved.
0F	Reserved	7:0	RSVD	R/W	01101001	Reserved.
10	Reserved	7:0	RSVD	R/W	00111010	Reserved.
11	Driver Control 1	7:6	SDO_VOS	R/W	10	Output driver offset voltage (common mode voltage). Applies to both SDO0 and SDO1 output drivers. 00: V_{OS} = 0.8V. 01: V_{OS} = 1.0V. 10, 11: V_{OS} = 1.2V.
		5	RSVD	R/W	0	Reserved.
		4	SDO0_PD	R/W	0	SDO0 output driver power down. 0: Normal operation. 1: SDO0 output driver powered down.
		3	SDO1_PD	R/W	0	SDO1 output driver power down. 0: Normal operation. 1: SDO1 output driver powered down.
		2	EOM_SEL_SD	R/W	0	SD eye monitor mode. 0: Operate eye monitor in HD or 3G mode. 1: Operate eye monitor in SD mode.
		1	EQ_BOOST_60	R/W	0	Input FR4 equalizer boost for 60” traces. (Recommended for FR4 trace lengths longer than 40”.) 0: Normal operation. 1: Enable extra equalizer boost for 60" FR4 trace operation.
		0	SDO_INV	R/W	0	Output driver invert. Inverts the signal polarity on both SDO0 and SDO1 outputs. 0: Normal output polarity. 1: Inverted polarity on both outputs.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
12	Driver Control 2	7:6	SDO0_VOD	R/W	11	SDO0 output swing. 00: V_{SSP-P} = 400 mV_{P-P}. 01: V_{SSP-P} = 530 mV_{P-P}. 10: V_{SSP-P} = 670 mV_{P-P}. 11: V_{SSP-P} = 800 mV_{P-P}.
		5:4	SDO1_VOD	R/W	11	SDO1 output swing. 00: V_{SSP-P} = 400 mV_{P-P}. 01: V_{SSP-P} = 530 mV_{P-P}. 10: V_{SSP-P} = 670 mV_{P-P}. 11: V_{SSP-P} = 800 mV_{P-P}.
		3	RSVD	R/W	0	Reserved.
		2	BYPASS	R/W	0	Bypass reclocker. 0: Normal operation. 1: Reclocker bypassed.
		1	$\overline{\text{MUTE}}$	R/W	1	Mute outputs (only used when register 0x09 bit 5, PIN_MODE_OV, is cleared). 0: SDO0 and SDO1 outputs muted. 1: Normal operation.
		0	SCO_EN	R/W	0	Serial clock output enable on SDO1 (only used when register 0x09 bit 5, PIN_MODE_OV, is cleared). 0: SDO1 output is data. 1: SDO1 output is the serial clock.
13	Driver Control 3	7:6	SDO0_DEM	R/W	00	SDO0 output driver de-emphasis level. 00: 0 dB (no de-emphasis). 01: 3 db de-emphasis. 10: 5 dB de-emphasis. 11: 7 db de-emphaiss.
		5:4	SDO1_DEM	R/W	00	SDO1 output driver de-emphasis level. 00: 0 dB (no de-emphasis). 01: 3 db de-emphasis. 10: 5 dB de-emphasis. 11: 7 db de-emphaiss.
		3:0	RSVD	R/W	0000	Reserved.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
14	Device Control	7	MUTE_STATE	R/W	0	Sets the state of the output drivers when muted. 0: When muted, outputs are forced to logic 0. 1: When muted, outputs are forced to logic 1.
		6:5	RSVD	R/W	00	Reserved.
		4	EOM_PD	R/W	1	Eye opening monitor power down. 0: EOM enabled. 1: EOM powered down.
		3:2	EOM_VRANGE	R/W	00	Eye opening monitor voltage range. 00: ±100 mV, resolution is 3.125 mV. 01: ±200 mV, resolution is 6.25 mV. 10: ±300 mV, resolution is 9.375 mV. 11: ±400 mV, resolution is 12.5 mV.
		1	MUX2_EQ_SEL	R/W	1	Selects equalized data for the EOM and also for the bypassed data for the SDO1 output. 0: Select non-equalized data. 1: Select equalized data.
		0	MULTI_LOCK_CHK	R/W	1	Multi lock check enable. 0: Failing lock conditions once causes reclocker to lose lock. 1: Require two failing lock conditions to cause reclocker to lose lock.
15	Receiver Power Down	7:5	SIG_DET_PD_X	R/W	000	Signal detect power down for unused inputs (input channels not present on the LMH0366). 000: Signal detection powered for unused inputs. 111: Signal detection powered down for unused inputs.
		4	SIG_DET_PD	R/W	0	Signal detect power down for SDI input. 0: Normal operation. 1: Signal detection powered down.
		3:1	EQ_PD_X	R/W	000	Equalizer power down for unused inputs (input channels not present on the LMH0366). 000: Equalizer powered for unused inputs. 111: Equalizer powered down for unused inputs.
		0	EQ_PD	R/W	0	Equalizer power down for SDI input. 0: Normal operation. 1: Equalizer powered down.
16	Reserved	7:0	RSVD	R/W	01111010	Reserved.
17	Reserved	7:0	RSVD	R/W	00110110	Reserved.
18	Reserved	7:0	RSVD	R/W	00000000	Reserved.
19	Reserved	7:0	RSVD	R/W	00100000	Reserved.
1A	Reserved	7:0	RSVD	R/W	00000000	Reserved.
1B	Reserved	7:0	RSVD	R/W	00000011	Reserved.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
1C	Rate Select	7:2	RSVD	R/W	001001	Reserved.
		1:0	RATE_SEL	R/W	00	Rate mode select. Select rate mode using the following code (must set register 0x1D bit 0 to override RATE pins first). 00: Auto-rate detect - video rates (270, 1483.5, 1485, 2967, 2970 Mbps). 01: 270 Mbps. 10: 1483.5/1485 Mbps, 2967/2970 Mbps. 11: 125 Mbps.
1D	Rate Select Control	7:1	RSVD	R/W	1000000	Reserved.
		0	RATE_SEL_OV	R/W	0	Rate select override to override use of RATE pins. 0: No override. Rate mode is selected by RATE pins. 1: Override rate selection using register 0x1C bits 1:0 (RATE_SEL) instead of using RATE pins.
1E	Output Select	7	RSVD	R/W	0	Reserved.
		6:5	SDO0_SEL	R/W	00	SDO0 manual output selection. When register 0x09 bit 5 is set (to override pin mode), this field allows manual selection of the SDO0 output. 00: Reclocked data, when locked; bypassed data, when unlocked. 01: Bypassed data. 10: Muted. 11: Reclocked data, when locked; bypassed data, when unlocked.
		4:3	SDO1_SEL	R/W	01	SDO1 manual output selection. When register 0x09 bit 5 is set (to override pin mode), this field allows manual selection of the SDO1 output. 00: Recovered clock, when locked; muted, when unlocked. 01: Reclocked data, when locked; bypassed data, when unlocked. 10: Muted. 11: Bypassed data.
		2:0	RSVD	R/W	011	Reserved.
1F	Reserved	7:0	RSVD	R/W	01010101	Reserved.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
20	Input Signal Detect Control	7	SIG_DET_PRESET	R/W	0	Signal detect preset.
		6	SIG_DET_RESET	R/W	0	Signal detect reset.
		5:3	SIG_DET_LVL	R/W	011	Differential input signal detect level (V_{SDID}). 011: Assert = 112 mV, de-assert = 78 mV. 100: Assert = 142 mV, de-assert = 112 mV. 101: Assert = 180 mV, de-assert = 142 mV. 110: Assert = 218 mV, de-assert = 180 mV. 111: Assert = 256 mV, de-assert = 218 mV. All others: Reserved.
		2:0	RSVD	R/W	000	Reserved.
21	Reserved	7:0	RSVD	R/W	00000101	Reserved.
22	EOM Control 1	7	EOM_OV	R/W	0	Eye opening monitor PDAC and VDAC override. 0: EOM phase and voltage DACs are controlled automatically (in fast EOM mode and during HEO/VEO measurement). 1: EOM phase DAC and voltage DAC values are overridden with the values in register 0x22 bits 5:0 (EOM_PDAC) and register 0x23 bits 5:0 (EOM_VDAC), respectively.
		6	EOM_SEL_3G	R/W	0	3G eye monitor mode. Adds filtering to improve EOM performance at 3G data rates. 0: Operate eye monitor in HD or SD mode. 1: Operate eye monitor in 3G mode.
		5:0	EOM_PDAC	R/W	000000	Eye opening monitor phase DAC value. When register 0x22 bit 7 (EOM_OV) is set, this field controls the EOM phase DAC.
23	EOM Control 2	7:6	RSVD	R/W	01	Reserved.
		5:0	EOM_VDAC	R/W	000000	Eye opening monitor voltage DAC value. When register 0x22 bit 7 (EOM_OV) is set, this field controls the EOM voltage DAC.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
24	EOM Control 3	7	FAST_EOM	R/W	0	Fast eye opening monitor mode. 0: Normal EOM mode. 1: Fast EOM mode. (In this mode, the control software does not need to configure the phase and voltage DAC values as this occurs automatically.)
		6:5	RSVD	R/W	00	Reserved.
		4	VEO_MAX_ERR	R		Vertical eye opening maximum error. Following HEO/VEO measurement, this error bit indicates that no top or bottom of the eye was found. 0: No error. 1: Error - no top or bottom of the eye was found.
		3	NO_OPENING_ERR	R		No eye opening error. Following HEO/VEO measurement, this error bit indicates that no eye opening was found (i.e. there was no point found at which there were no hits). 0: No error. 1: Error - no eye opening was found.
		2	NO_HITS_ERR	R		No hits error. Following HEO/VEO measurement, this error bit indicates that there were no points found at which there was a hit. 0: No error. 1: Error - no hits found.
		1	GET_HEO_VEO	R/W	0	Get horizontal and vertical eye opening. Initiates measurement of the horizontal eye opening and vertical eye opening by the EOM and clears itself once the measurements are complete. 0: EOM HEO/VEO measurement is inactive or complete. 1: EOM HEO/VEO measurement active.
		0	EOM_START	R/W	0	Eye opening monitor active. Indicates that the EOM is actively searching for hits at the current phase/voltage DAC combination. In normal EOM mode, setting this bit starts the EOM counter. In fast EOM mode, this bit is set automatically. (This bit is self-clearing.) 0: EOM inactive. 1: EOM active.
25	EOM Count Status 1	7:0	EOM_COUNT[15:8]	R		Eye opening monitor hits count, bits 15:8. Upper byte of the number of hits accumulated for the previous EOM phase/voltage DAC combination.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
26	EOM Count Status 2	7:0	EOM_COUNT[7:0]	R		Eye opening monitor hits count, bits 7:0. Lower byte of the number of hits accumulated for the previous EOM phase/voltage DAC combination. In fast EOM mode (i.e. register 0x24 bit 7, FAST_EOM, is set), reading this register causes the EOM to step to the next phase/voltage DAC combination and start the next measurement.
27	Reserved	7:0	RSVD	R/W	01001000	Reserved.
28	Reserved	7:0	RSVD	R/W	01001000	Reserved.
29	EOM Timer Control	7:0	EOM_TIMER	R/W	00000001	Eye opening monitor timer. Sets the eye opening monitor timer value in units of 256 clock cycles of the divide-by-12 VCO clock.
2A	HEO Status	7:0	HEO	R		Horizontal eye opening. Following HEO/VEO measurement, indicates the measured horizontal eye opening. Valid values are between 1 and 63 decimal. A value of 64, accompanied by register 0x24 bit 2 (NO_HITS_ERR) set, indicates the lack of a zero crossing detection. A value of 0, accompanied by register 0x24 bit 3 (NO_OPENING_ERR) set, indicates a fully closed eye.
2B	VEO Status	7:0	VEO	R		Vertical eye opening. Following HEO/VEO measurement, indicates the measured vertical eye opening. Valid values are between 1 and 63 decimal. A value of 64, accompanied by register 0x24 bit 4 (VEO_MAX_ERR) set, indicates the lack of detection of the upper and lower limits of the eye.
2C	EOM Control 4	7:4	RSVD	R/W	0000	Reserved.
		3:0	EOM_MIN_HITS	R/W	0000	Eye opening monitor minimum hits. Sets the minimum required number of hits at each point in the horizontal direction to detect “closed” at that point.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
2D	PPM Counter Contol	7:3	RSVD	R/W	00000	Reserved.
		2	PPM_CNT_MODE	R/W	0	PPM counter mode. Controls the use of the PPM counter and the external reference clock when qualifying lock. 0: Normal operation. Qualify lock with the PPM counter if the reference clock is detected. 1: Ignore the PPM counter when determining lock, regardless of the presence of a reference clock (i.e. do not use the reference clock and run in referenceless mode).
		1	PPM_START	R/W	0	Manual PPM count trigger. When register 0x2D bit 0 (PPM_START_OV) is set, this bit can be used to start a manual PPM count measurement. To start another measurement, this bit must be toggled low to high. 0: Normal operation. Manual PPM count disabled. 1: Manual PPM count enabled.
		0	PPM_START_OV	R/W	0	Manual PPM count enable. Enables the use of register 0x2D bit 1 (PPM_START) to manually start a PPM count measurement. 0: Normal operation. PPM counter is controlled automatically by the LMH0366. 1: Manual PPM count operation enabled. Register 0x2D bit 2 (PPM_CNT_MODE) should be set to ignore the PPM counter so that the LMH0366 will not automatically attempt to start the PPM counter.
2E	PPM Threshold Control 1	7:0	PTCR1	R/W	11011011	1.485/2.97 Gbps low threshold, bits 15:8.
2F	PPM Threshold Control 2	7:0	PTCR2	R/W	11100110	1.485/2.97 Gbps low threshold, bits 7:0.
30	PPM Threshold Control 3	7:0	PTCR3	R/W	11011100	1.485/2.97 Gbps high threshold, bits 15:8.
31	PPM Threshold Control 4	7:0	PTCR4	R/W	00011010	1.485/2.97 Gbps high threshold, bits 7:0.
32	PPM Threshold Control 5	7:0	PTCR5	R/W	11011011	1.4835/2.967 Gbps low threshold, bits 15:8.
33	PPM Threshold Control 6	7:0	PTCR6	R/W	10101110	1.4835/2.967 Gbps low threshold, bits 7:0.
34	PPM Threshold Control 7	7:0	PTCR7	R/W	11011011	1.4835/2.967 Gbps high threshold, bits 15:8.
35	PPM Threshold Control 8	7:0	PTCR8	R/W	11100001	1.4835/2.967 Gbps high threshold, bits 7:0.
36	PPM Threshold Control 9	7:0	PTCR9	R/W	11101111	270 Mbps low threshold, bits 15:8.
37	PPM Threshold Control 10	7:0	PTCR10	R/W	11100100	270 Mbps low threshold, bits 7:0.
38	PPM Threshold Control 11	7:0	PTCR11	R/W	11110000	270 Mbps high threshold, bits 15:8.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
39	PPM Threshold Control 12	7:0	PTCR12	R/W	00011100	270 Mbps high threshold, bits 7:0.
3A	PPM Threshold Control 13	7:0	PTCR13	R/W	11011110	125 Mbps low threshold, bits 15:8.
3B	PPM Threshold Control 14	7:0	PTCR14	R/W	00011111	125 Mbps low threshold, bits 7:0.
3C	PPM Threshold Control 15	7:0	PTCR15	R/W	11011110	125 Mbps high threshold, bits 15:8.
3D	PPM Threshold Control 16	7:0	PTCR16	R/W	01010011	125 Mbps high threshold, bits 7:0.
3E	PPM Timer Control 1	7:4	RSVD	R/W	0000	Reserved.
		3:0	PPM_TIMER[11:8]	R/W	1100	PPM reference clock timer, bits 11:8. This field, along with register 0x3F bits 7:0, comprise a 12-bit value corresponding to the number of reference clock cycles in which to count VCO/12 clock cycles (the measurement period).
3F	PPM Timer Control 1	7:0	PPM_TIMER[7:0]	R/W	00000000	PPM reference clock timer, bits 7:0. This field, along with register 0x3E bits 3:0, comprise a 12-bit value corresponding to the number of reference clock cycles in which to count VCO/12 clock cycles (the measurement period).
40	Reserved	7:0	RSVD	R/W	00000000	Reserved.
41	PPM Status	7:4	RSVD	R	0000	Reserved.
		3	REF_CLK_DET	R		Reference clock detected. 0: No external reference clock detected or reference clock detector disabled. 1: External reference clock detected.
		2	RATE_1_OV_M	R		1 over M rate detect. 0: 1 over M rate not detected. 1: 1.485/1.001 or 2.970/1.001 Gbps rate detected.
		1	PPM_CNT_MET	R		PPM count in range. When register 0x41 bit 0 (PPM_CNT_RDY) is set, this bit indicates that the current PPM count measurement was in range of one of the four valid bands configured in the PTCR registers.
		0	PPM_CNT_RDY	R		PPM count ready. Indicates the completion of a PPM count measurement. 0: PPM count measurement not ready or PPM counter disabled. 1: PPM count measurement complete.
42	PPM Count Status 1	7:0	PPM_COUNT[15:8]	R		PPM cycle count, bits 15:8. This field, along with register 0x43 bits 7:0, comprise a 16-bit value corresponding to the number of VCO/12 clock cycles in the current PPM count measurement.

Table 8. SPI Registers (continued)

Addr (hex)	Name	Bits	Field	R/W	Default (binary)	Description
43	PPM Count Status 2	7:0	PPM_COUNT[7:0]	R		PPM cycle count, bits 7:0. This field, along with register 0x42 bits 7:0, comprise a 16-bit value corresponding to the number of VCO/12 clock cycles in the current PPM count measurement.
44	Reserved	7:0	RSVD	R		Reserved.
45	Reserved	7:0	RSVD	R		Reserved.

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D **Page**

- Changed layout of National Data Sheet to TI format 22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0366SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L0366SQ	Samples
LMH0366SQE/NOPB	ACTIVE	WQFN	RTW	24	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L0366SQ	Samples
LMH0366SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	RoHS & Green	SN	Level-1-260C-UNLIM		L0366SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

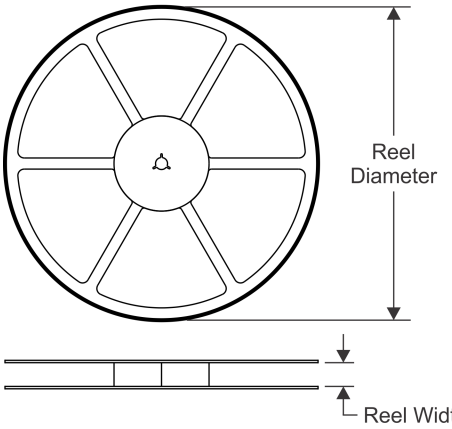
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

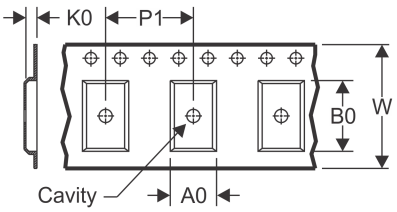
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

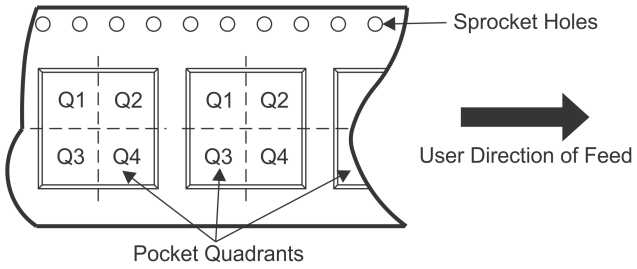


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

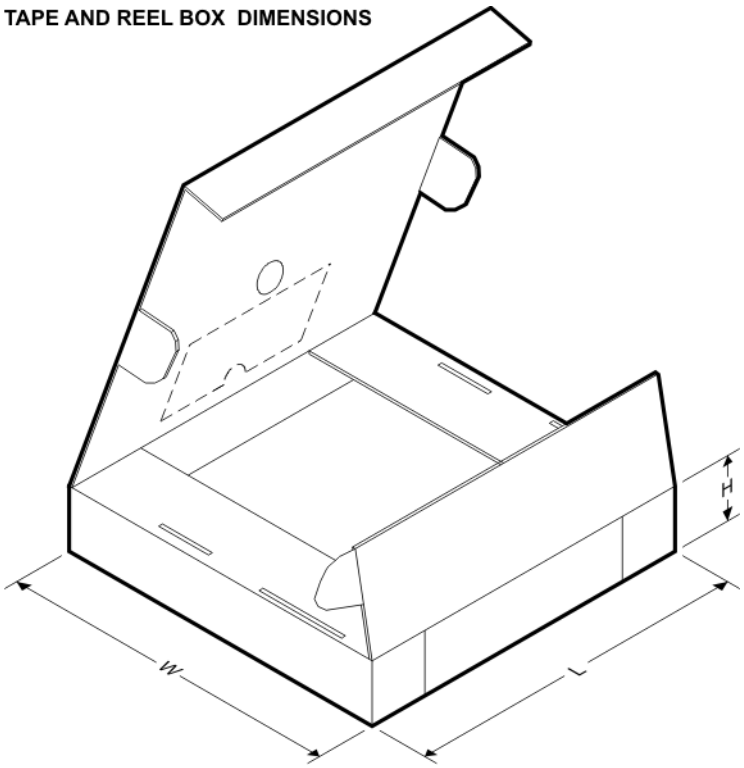
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0366SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0366SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0366SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

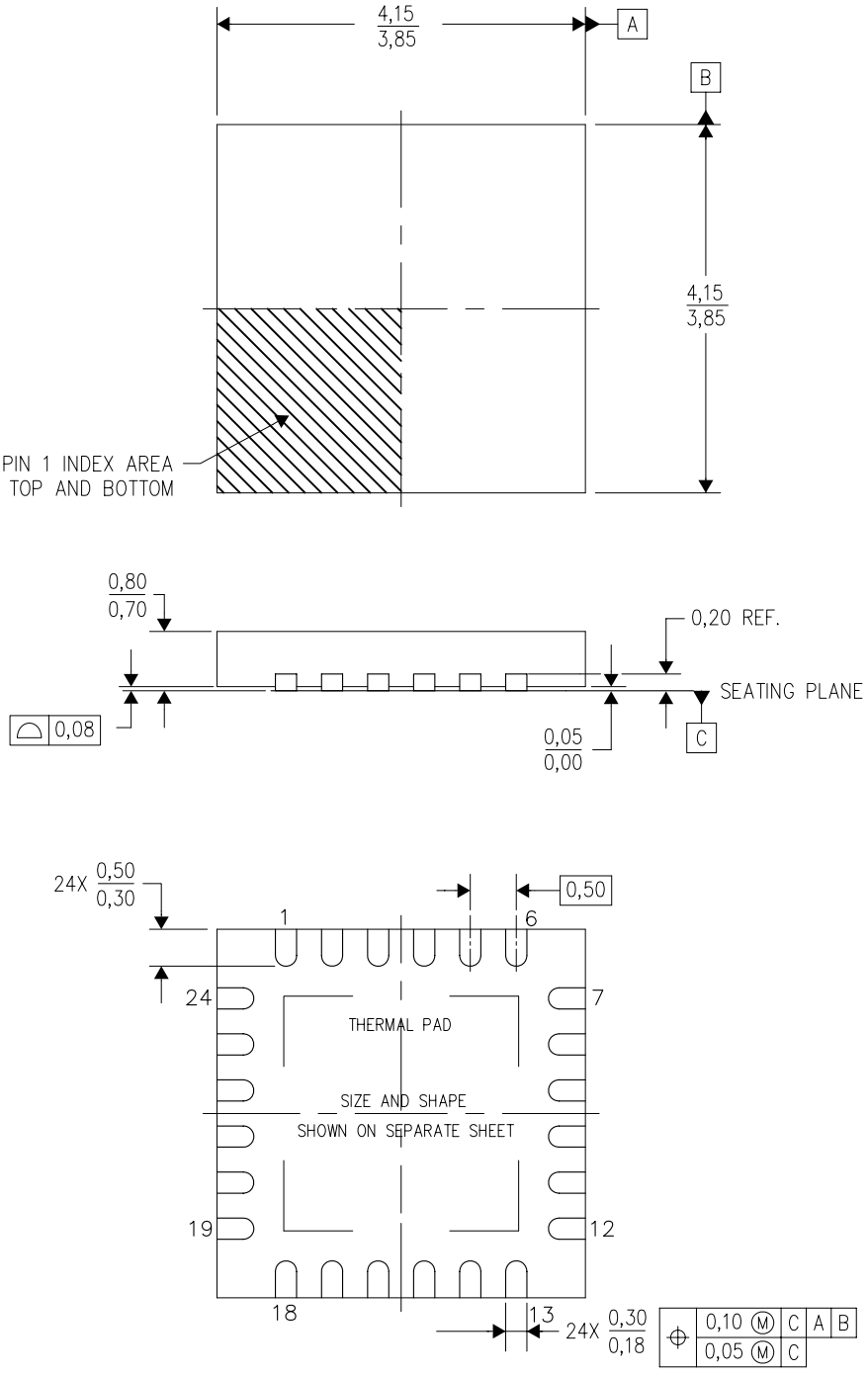
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0366SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LMH0366SQE/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0
LMH0366SQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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