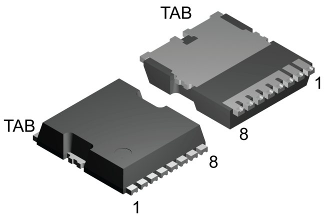
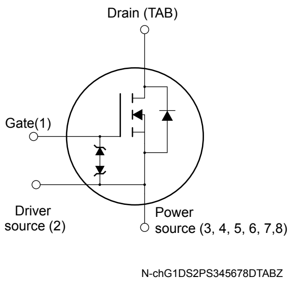
STO67N60DM6

Datasheet

N-channel 600 V, 48 mΩ typ., 33 A MDmesh DM6 Power MOSFET in a TO-LL HV package



TO-LL HV



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STO67N60DM6	600 V	59 mΩ	33 A

- Fast-recovery body diode
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q_{rr}), recovery time (t_{rr}) and excellent improvement in $R_{DS(on)}$ per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

Maturity status link
STO67N60DM6

Device summary	
Order code	STO67N60DM6
Marking	67N60DM6
Package	TO-LL HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	33	A
	Drain current (continuous) at T_C = 100 °C	21	A
I_{DM} (1)	Drain current (pulsed)	190	A
P_{TOT}	Total power dissipation at T_C = 25 °C	150	W
dv/dt (2)	Peak diode recovery voltage slope	50	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	100	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 33 A, di/dt ≤ 900 A/μs, $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V*
3. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.83	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (1)	43	
	Thermal resistance junction-ambient (2)	22	

1. *When mounted on 1 inch² FR-4 pcb, standard footprint 2 Oz copper board.*
2. *When mounted on 40x40mm FR-4 pcb, 6 cm² 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	9	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	845	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS}= 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 23.75 A		48	59	mΩ

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	3400	-	pF
C_{oss}	Output capacitance		-	280	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 480 V	-	520	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.5	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 52 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	72.5	-	nC
Q_{gs}	Gate-source charge		-	24.5	-	nC
Q_{gd}	Gate-drain charge		-	28.5	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d\ (on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 23.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	24.5	-	ns
t_r	Rise time		-	32	-	ns
$t_{d(off)}$	Turn-off delay time		-	87.5	-	ns
t_f	Fall time		-	8.6	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		33	A
I_{SDM} (1)	Source-drain current (pulsed)		-		190	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 47.5 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 47.5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	125		ns
Q_{rr}	Reverse recovery charge		-	0.6		µC
I_{RRM}	Reverse recovery current		-	9.6		A
t_{rr}	Reverse recovery time	I_{SD} = 47.5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	228		ns
Q_{rr}	Reverse recovery charge		-	2.34		µC
I_{RRM}	Reverse recovery current		-	20.5		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

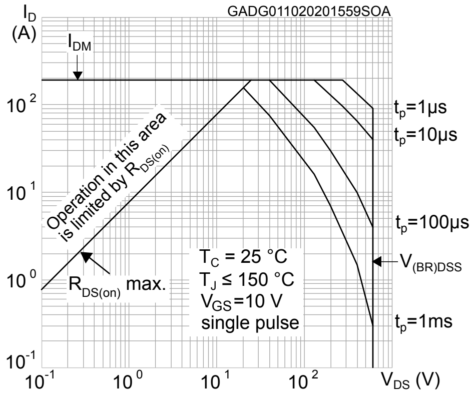


Figure 2. Maximum transient thermal impedance

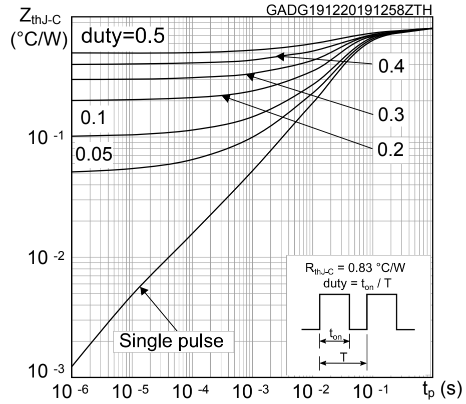


Figure 3. Typical output characteristics

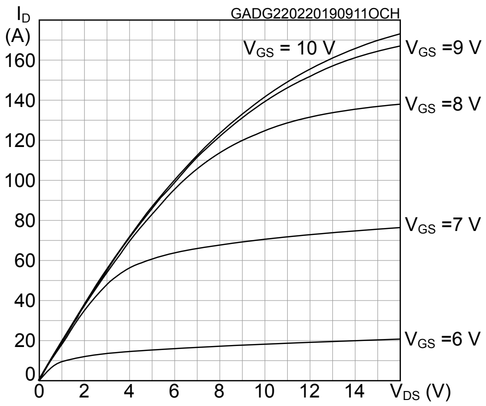


Figure 4. Typical transfer characteristics

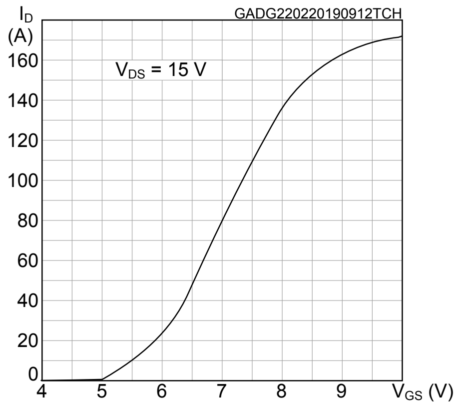


Figure 5. Typical gate charge characteristics

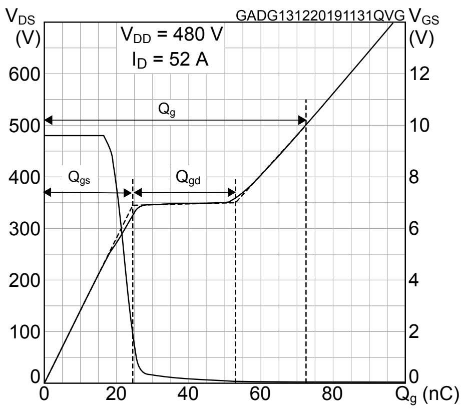


Figure 6. Typical drain-source on-resistance

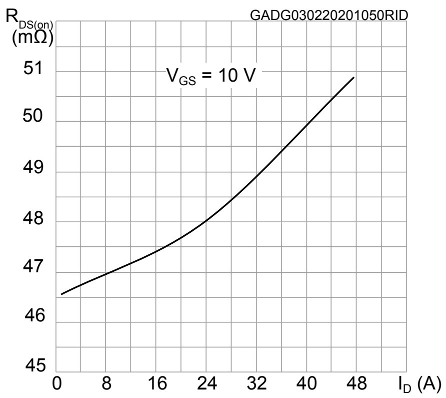


Figure 7. Typical capacitance characteristics

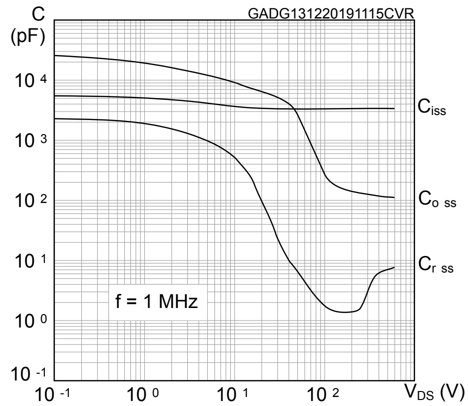


Figure 8. Normalized gate threshold vs. temperature

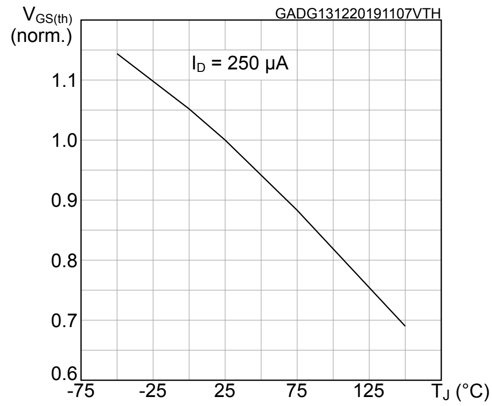


Figure 9. Normalized on-resistance vs. temperature

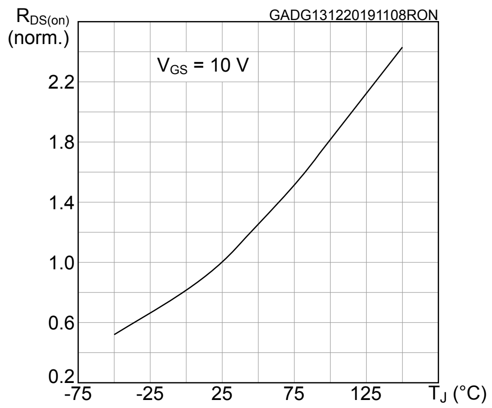


Figure 10. Normalized breakdown voltage vs temperature

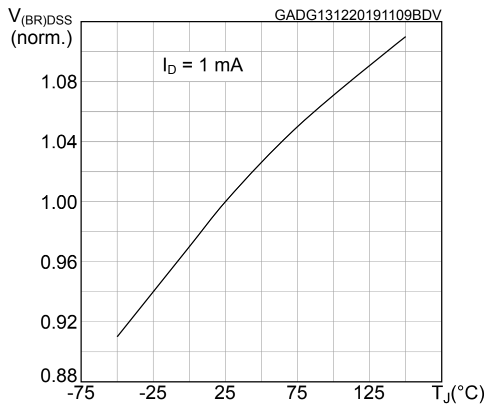


Figure 11. Output capacitance stored energy

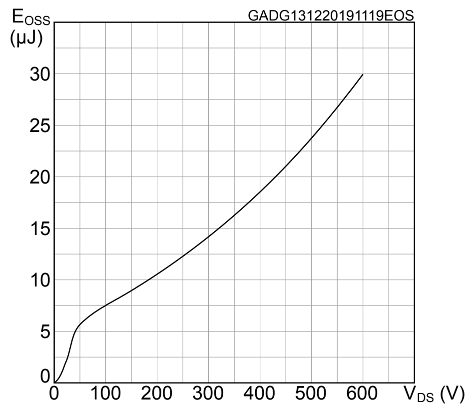
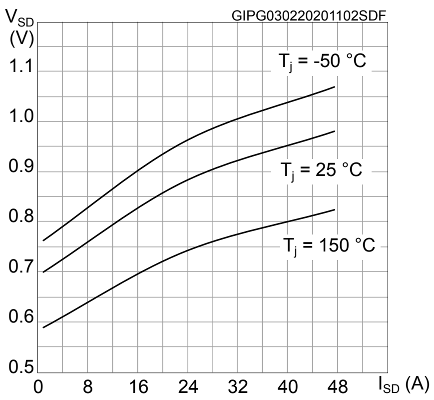


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

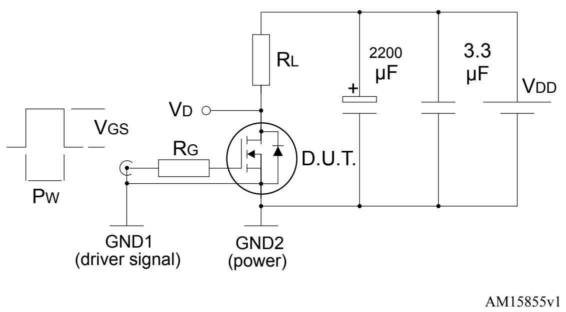


Figure 14. Test circuit for gate charge behavior

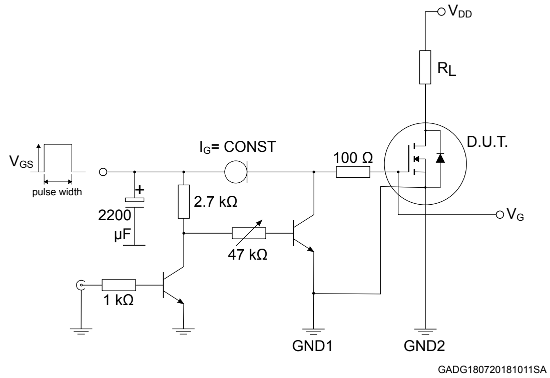


Figure 15. Test circuit for inductive load switching and diode recovery times

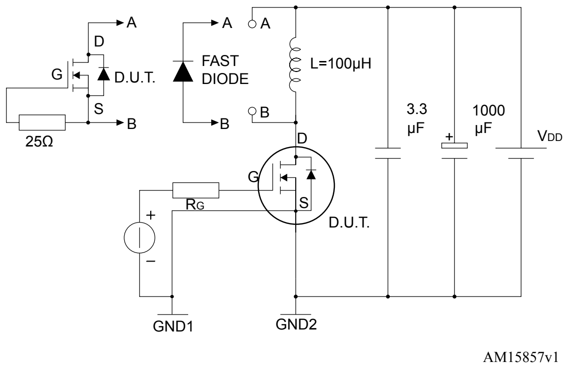


Figure 16. Unclamped inductive load test circuit

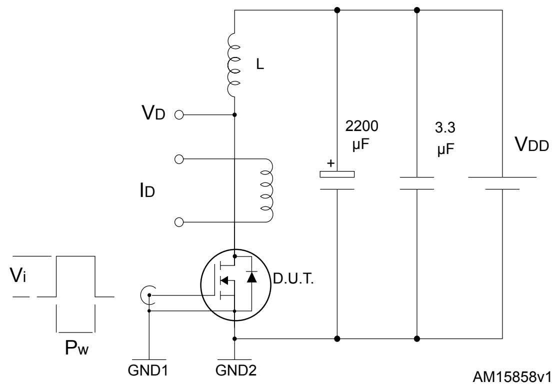


Figure 17. Unclamped inductive waveform

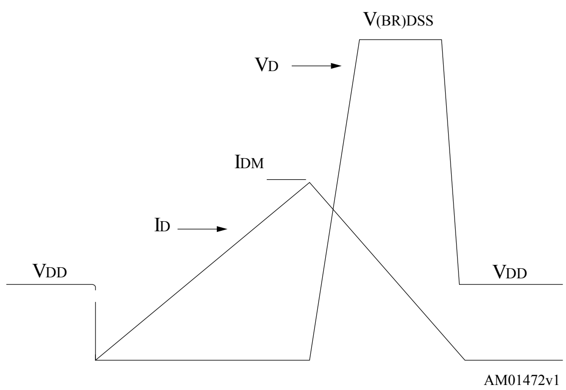
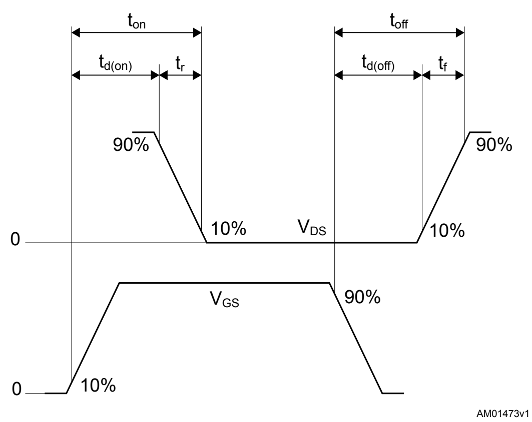


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL HV package information

Figure 19. TO-LL HV package outline

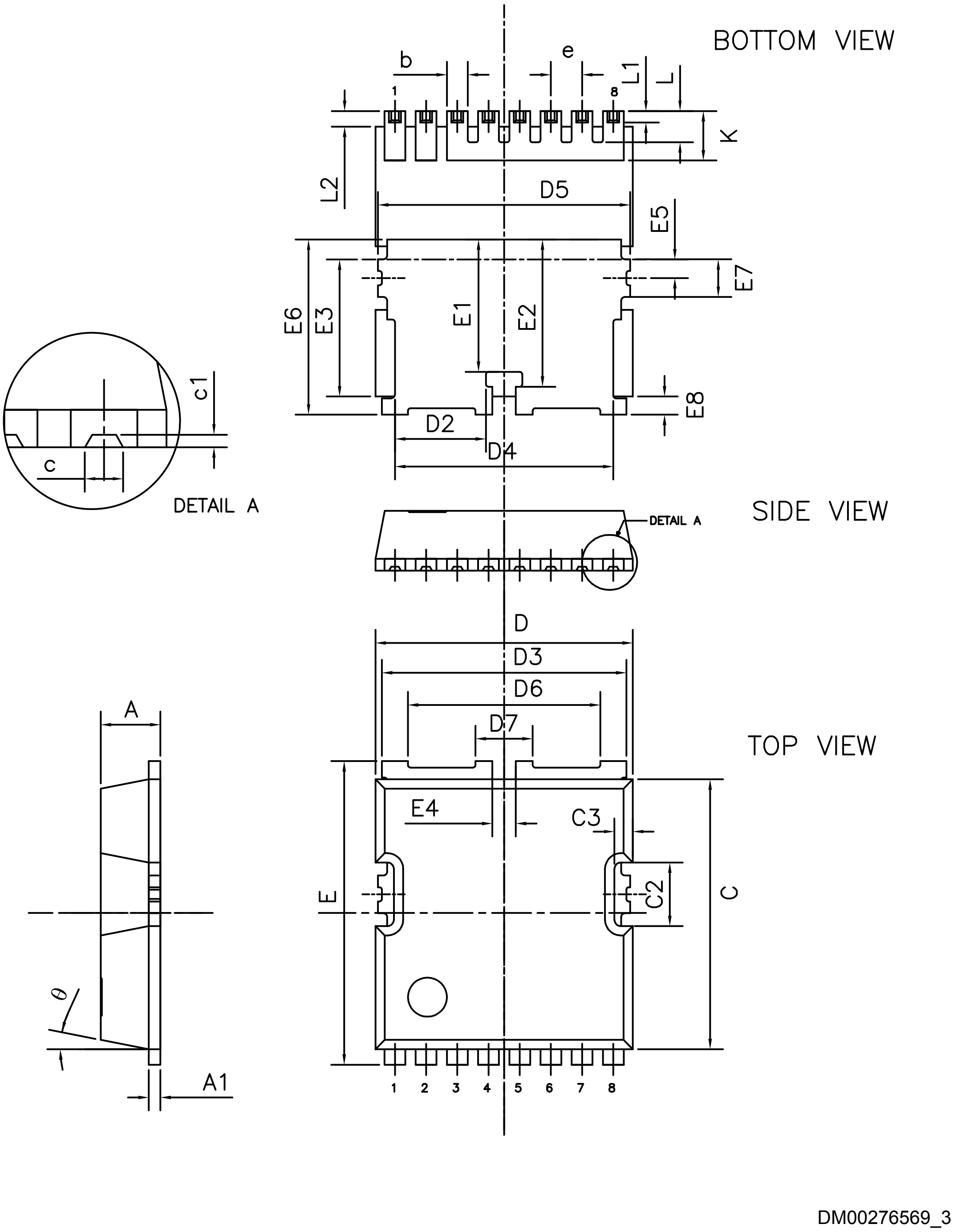
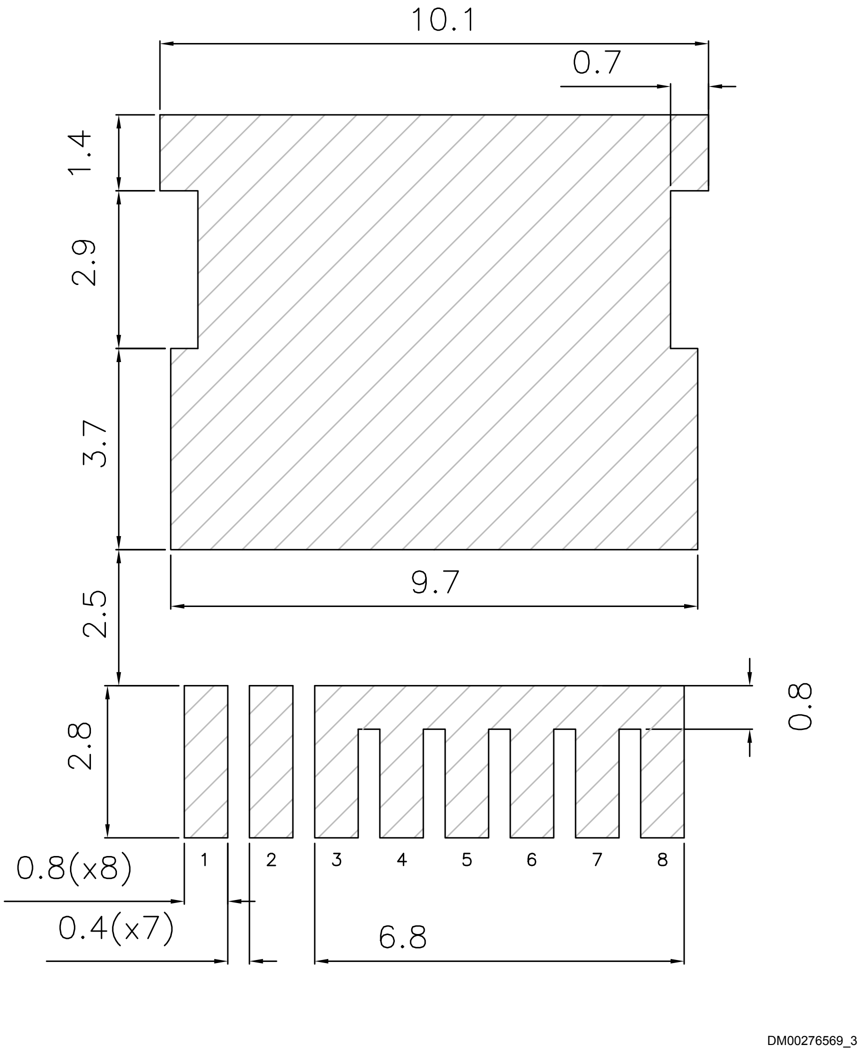


Table 8. **TO-LL HV package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.40	0.48	0.60
b		0.80	
c		0.46	
c1		0.15	
C	10.28	10.38	10.48
C2	2.35	2.45	2.55
C3		0.71	
D	9.80	9.90	10.00
D2	3.30	3.53	3.73
D3	9.30	9.40	9.50
D4	8.26	8.46	8.66
D5	9.50	9.70	9.90
D6		7.40	
D7		2.20	
e		1.20	
E	11.48	11.68	11.88
E1		5.09	
E2		5.66	
E3		5.14	
E4		0.90	
E5		0.72	
E6	6.54	6.74	6.94
E7		1.45	
E8	0.50	0.70	0.90
K	1.70	1.90	2.10
L	1.05	1.20	1.35
L1	0.25	0.35	0.45
L2	0.40	0.60	0.80
θ		11°	

Figure 20. TO-LL HV recommended footprint (dimensions are in mm)



Revision history

Table 9. **Document revision history**

Date	Revision	Changes
03-Feb-2020	1	First release.
20-Mar-2020	2	Updated title of the document, Section Features, Table 1. Absolute maximum ratings, Table 4. On /off-states and Table 7. Source-drain diode.

Contents