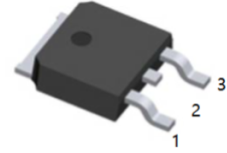


-60 V P-Channel Enhancement Mode MOSFET

DESCRIPTION

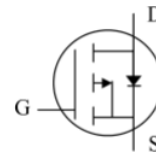
The IRFR5305TR uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.



1.G 2.D 3.S
TO-252(DPAK) top view

GENERAL FEATURES

- $V_{DS} = -60V, I_D = -30A$
- $R_{DS(ON)} < 40m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} < 55m\Omega @ V_{GS} = -4.5V$
- High Power and current handling capability
- Lead free product is acquired
- Surface Mount Package



Application

- PWM applications
- Load switch
- Power management

ABSOLUTE MAXIMUM RATINGS(TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-60	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	I _D (25°C)	-30	A
	I _D (70°C)	-20	A
	I _{DM}	-60	A
Maximum Power Dissipation	P _D	60	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 To 175	°C
Thermal Resistance, Junction-to-Ambient (Note 2)	R _{θJA}	25	°C/W

-60 V P-Channel Enhancement Mode MOSFET
ELECTRICAL CHARACTERISTICS (TA=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-48V, V _{GS} =0V			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.1	-2	-3	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-20A		31	40	mΩ
		V _{GS} =-4.5V, I _D =-20A		42	55	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-20A	5			S
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, F=1.0MHz		3060		PF
Output Capacitance	C _{oss}			300		PF
Reverse Transfer Capacitance	C _{rss}			205		PF
Turn-on Delay Time	t _{d(on)}	V _{DS} =-30V, V _{GS} =-10V, R _{GEN} =3Ω I _D =1A		14		nS
Turn-on Rise Time	t _r			20		nS
Turn-Off Delay Time	t _{d(off)}			40		nS
Turn-Off Fall Time	t _f			19		nS
Total Gate Charge	Q _g				48	
Gate-Source Charge	Q _{gs}	V _{DS} =-30V, I _D =-20A, V _{GS} =-10V		11		nC
Gate-Drain Charge	Q _{gd}			10		nC
Body Diode Reverse Recovery Time	T _{rr}	I _F =-20A, dI/dt=100A/μs		40		nS
Body Diode Reverse Recovery Charge	Q _{rr}			56		nC
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =-1A		-0.72	-1	V

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on 1in² FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

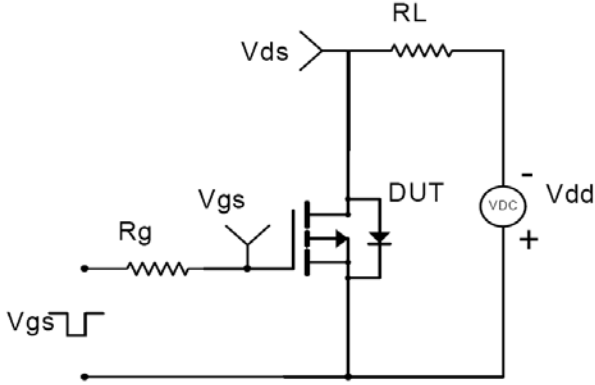


Figure 1: Switching Test Circuit

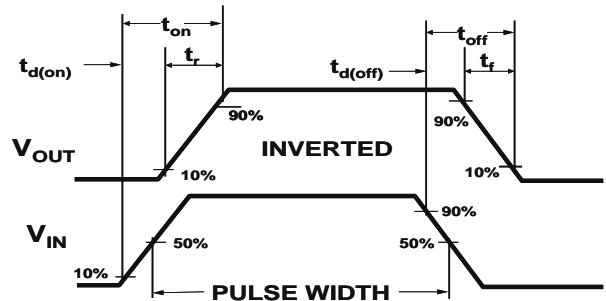


Figure 2: Switching Waveforms

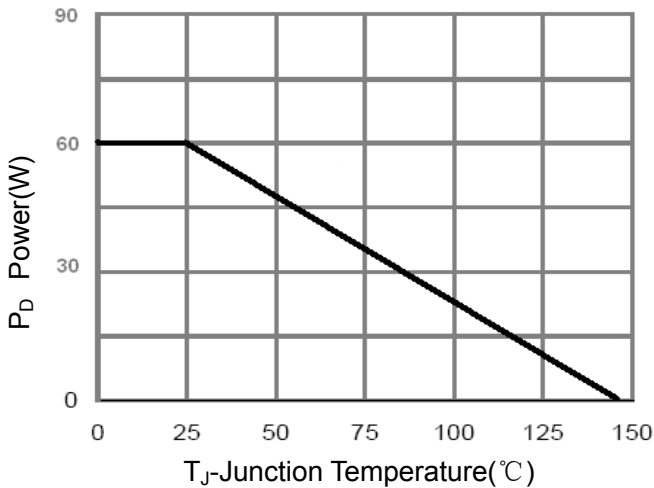


Figure 3 Power Dissipation

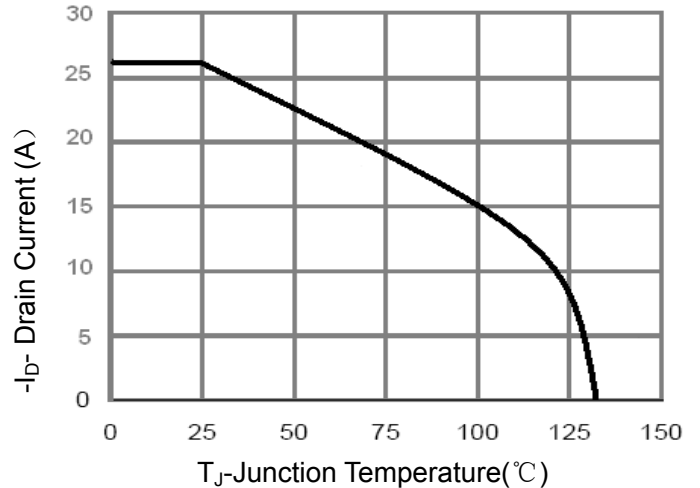


Figure 4 Drain Current

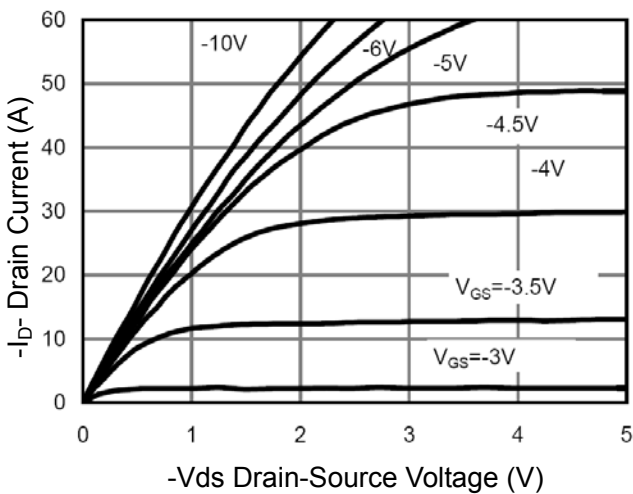


Figure 5 Output CHARACTERISTICS

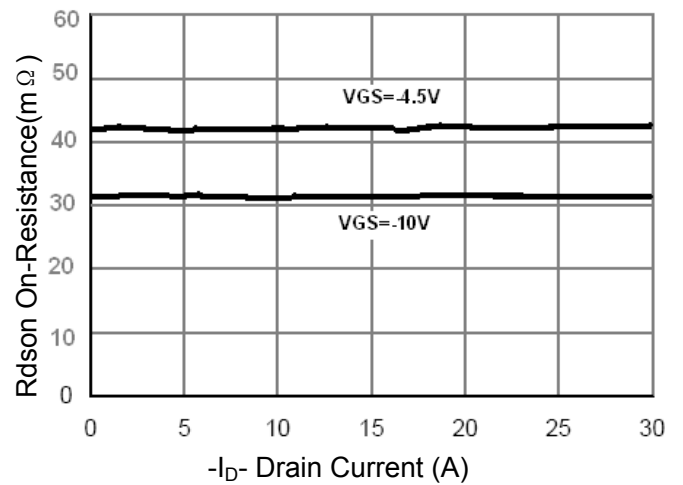


Figure 6 Drain-Source On-Resistance

-60 V P-Channel Enhancement Mode MOSFET

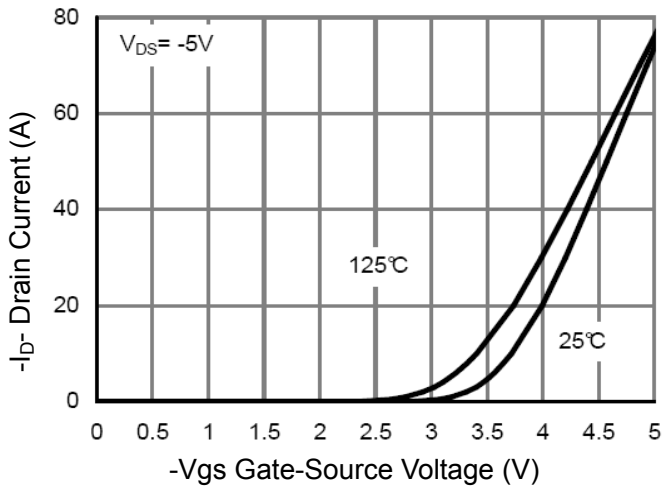


Figure 7 Transfer Characteristics

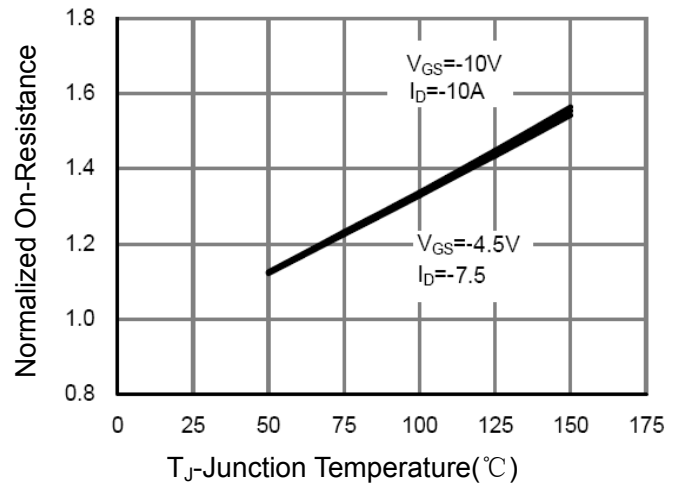


Figure 8 Drain-Source On-Resistance

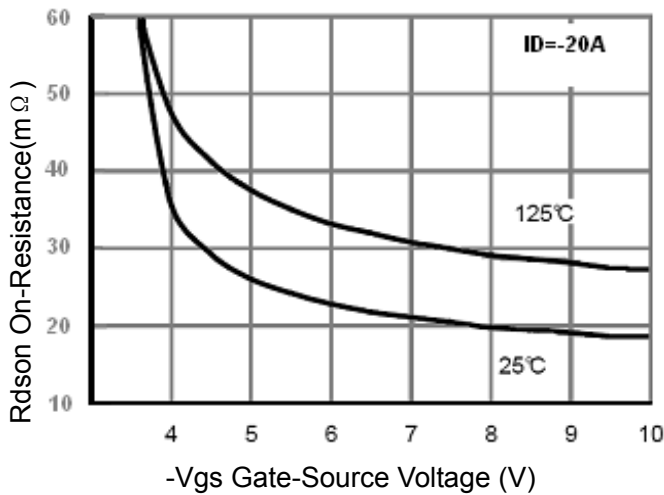


Figure 9 $R_{DS(on)}$ vs V_{GS}

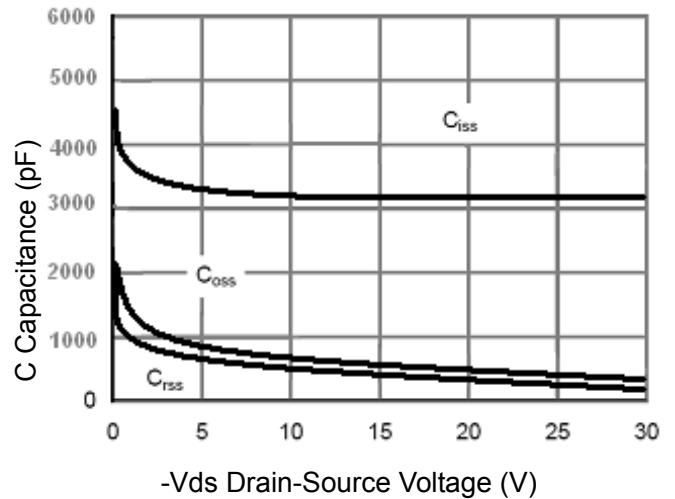


Figure 10 Capacitance vs V_{DS}

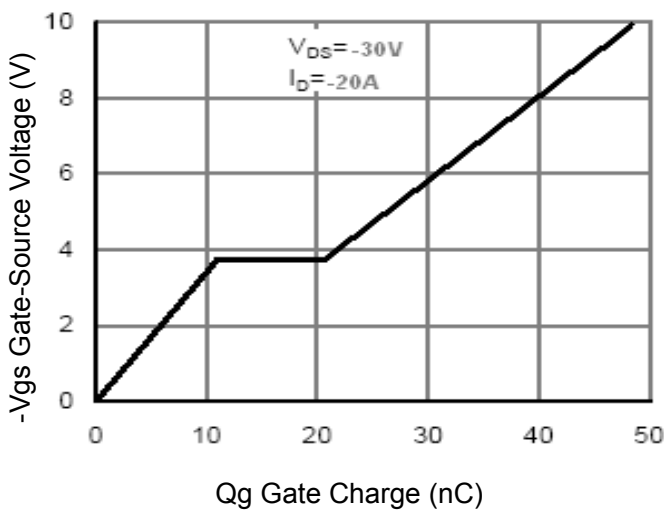


Figure 11 Gate Charge

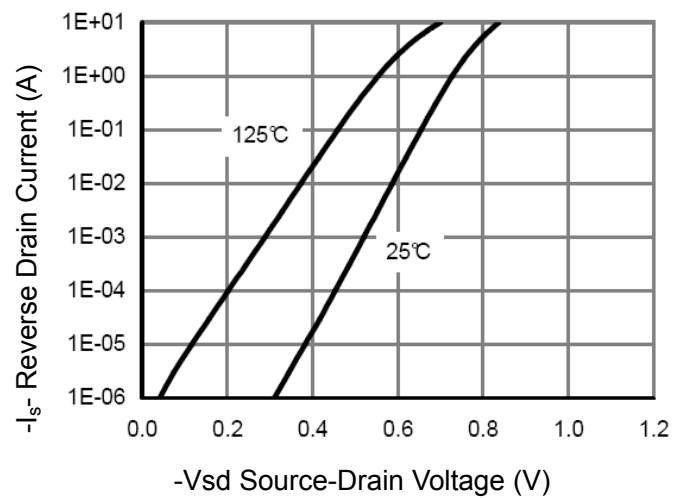


Figure 12 Source- Drain Diode Forward

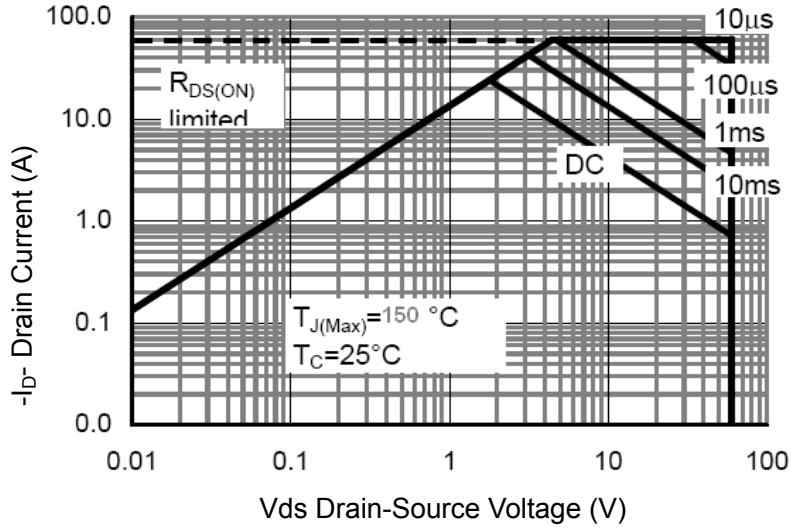


Figure 13 Safe Operation Area

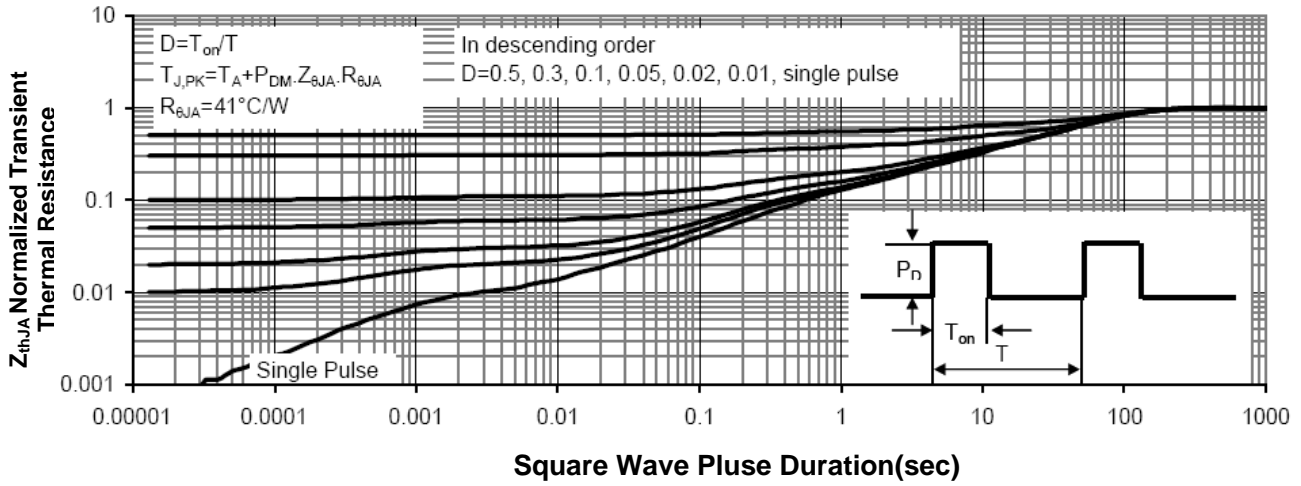
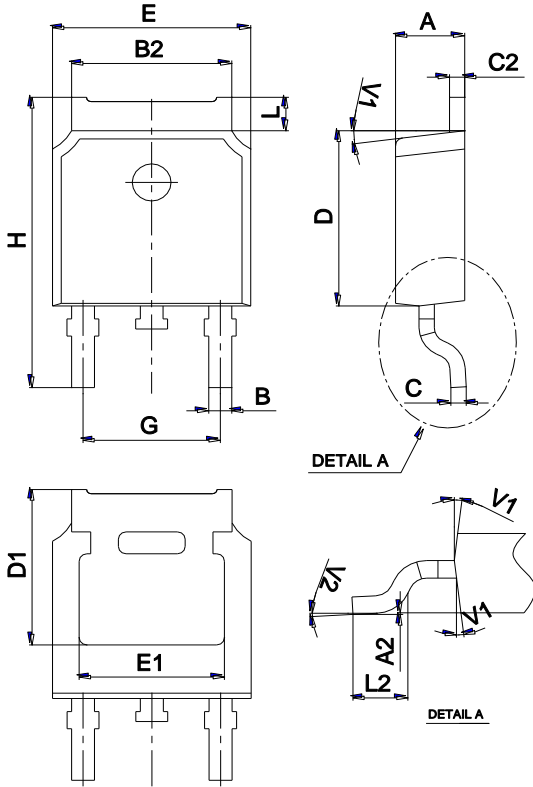


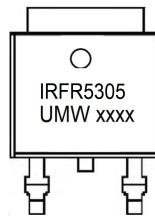
Figure 14 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRFR5305TR	TO-252	2500	Tape and reel