Integrated silicon pressure sensor, on-chip signal conditioned, temperature compensated and calibrated

Rev. 12 — 9 June 2023

Product data sheet

1 General description

The MPXx5050 series piezoresistive transducer is a state-of-the-art monolithic silicon pressure sensor designed for a wide range of applications, but particularly those employing a microcontroller or microprocessor with A/D inputs. This patented, single element transducer combines advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure.

2 Feature and benefits

- 2.5 % Maximum Error over 0 ° to 85 °C
- Ideally suited for Microprocessor or Microcontroller-based systems
- Temperature compensated over –40 ° to +125 °C
- Patented silicon shear stress strain gauge
- Durable epoxy unibody element
- Easy-to-use chip carrier option

3 Ordering information

Table 1. Ordering information

Type number	Package	Package						
	Name	Description	Version					
MPX5050DP	SENSOR4F	Pressure sensor, 5 V, 0/50 kPa, Port; Unibody package, 4 terminals; 2.54 mm pitch; 17.78 mm x 29.48 mm x 10.67 mm body	SOT1756-1					
MPXV5050DP	SENSOR6F	Pressure sensor, 5 V, 0/50 kPa, Port, SO8, plastic, small outline package; 8 terminals; 2.54 mm pitch; 12.06 mm x 12.06 mm x 7.62 mm body	SOT1693-1					
MPXV5050GP	SO8	Pressure sensor, 5 V, 0/50 kPa, Port, 8 terminals; 2.54 mm pitch; 12.06 mm x 12.06 mm x 3.38 mm body body	SOT1693-3					
MPXV5050GC6T1	SO8	Pressure sensor, 5 V, 0/540 kPa, small outline package, Port, 8 terminals; 2.54 mm pitch; 10.67 mm x 10.67 mm x 12.96 mm body	SOT18454-1					



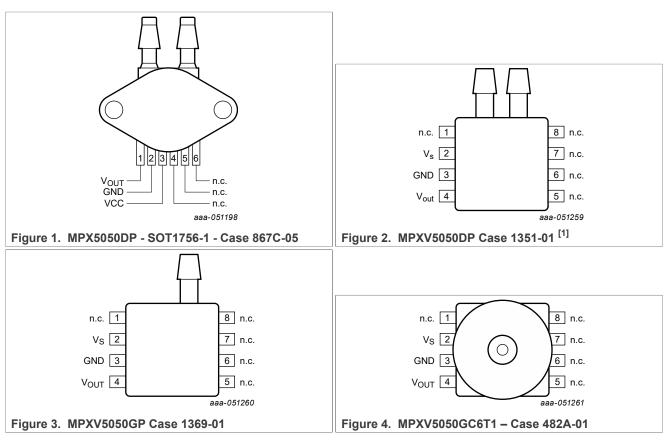
3.1 Ordering options

Table 2. Ordering options

ORDERING INFORMATION									
Device Name	Case	# of Ports			F	Pressure Type			
Device Name	No.	None	Single	Dual	Gauge	Differential	Absolute	Marking	
Unibody Package (MPX5050 Series)									
MPX5050DP	867C			•		•		MPX5050DP	
Small Outline Packa	age (MPX)	/5050 Sei	ries)						
MPXV5050GP	1369		•		•			MPXV5050GP	
MPXV5050DP	1351			•		•		MPXV5050DP	
MPXV5050GC6T1	482A		•		•			MPXV5050G	

4 Pinning information

4.1 Pinning



[1] Refer to <u>Table 4</u> and style 2 in <u>Figure 13</u> in <u>Section 7 "Package outline"</u>

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4.2 Pin description

Table 3. Pin descriptions - MPX5050DP

Symbol	Pin	Description
V _{OUT}	1	V _{OUT}
Ground	2	Ground
V _{CC}	3	Supply voltage
N.C.	4	No connection.
N.C.	5	No connection.
N.C.	6	No connection.

Table 4. Pin descriptions - MPXV5050GC6T1, MPXV5050DP, and MPXV5050GP

Symbol	Pin	Description
N.C.	1	No connect
V _S	2	Supply voltage
Ground	3	Ground
V _{OUT}	4	V _{OUT}
N.C.	5	No connect
N.C.	6	No connect
N.C.	7	No connect
N.C.	8	No connect

5 Limiting values

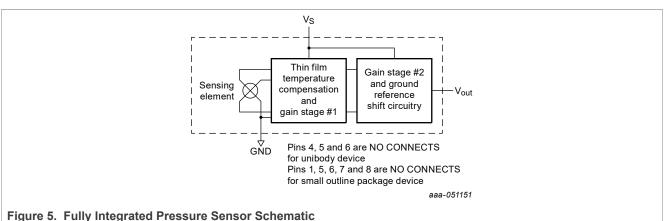
Table 5. Limiting values ^[1]

Rating	Symbol	Value	Unit
Maximum pressure (P1 > P2)	P _{max}	200	kPa
Storage temperature	T _{stg}	-40 to +125	°C
Operating temperature	T _A	-40 to +125	°C

[1] Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Figure 5 shows a block diagram of the internal circuitry integrated on a pressure sensor chip.

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Recommended operating conditions 6

Table 6. Recommended operating conditions

(V_S = 5.0 Vdc, T_A = 25 °C unless otherwise noted, P1 > P2. Decoupling circuit shown in Figure 8 required to meet electrical specifications.)

Characteristic	Symbol	Min	Тур	Мах	Unit
Pressure Range ^[1]	P _{OP}	0	_	50	kPa
Supply Voltage ^[2]	Vs	4.75	5.0	5.25	Vdc
Supply Current	Ι _ο		7.0	10	mAdc
Minimum Pressure Offset ^[3] (0 °C to 85 °C) @ $V_S = 5.0$ Volts	V _{off}	0.088	0.2	0.313	Vdc
Full Scale Output ^[4] (0 °C to 85 °C) @ $V_S = 5.0$ Volts	V _{FSO}	4.587	4.7	4.813	Vdc
Full Scale Span ^[5] (0 °C to 85 °C) @ V _S = 5.0 Volts	V _{FSS}		4.5		Vdc
Accuracy ^[6] (0 °C to 85 °C)	—			±2.5	%V _{FSS}
Sensitivity	V/P		90	_	mV/kPa
Response Time ^[7]	t _R		1.0	_	ms
Output Source Current at Full Scale Output	I _{o+}		0.1	_	mAdc
Warm-Up Time ^[8]	_		20	_	ms
Offset Stability ^[9]	_		±0.5	_	%V _{FSS}

1.0 kPa (kiloPascal) equals 0.145 psi. [1]

Device is ratiometric within this specified excitation range. [2] [3]

Offset (Voff) is defined as the output voltage at the minimum rated pressure.

Full Scale Output (V_{FSO}) is defined as the output voltage at the maximum or full rated pressure.

[4] [5] Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.

[6] Accuracy (error budget) consists of the following:

Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.

Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.

Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the minimum or maximum rated pressure at 25 °C.

TcSpan: Output deviation over the temperature range of 0 °C to 85 °C, relative to 25 °C.

TcOffset: Output deviation with minimum pressure applied, over the temperature range of 0 °C to 85 °C, relative to 25 °C.

Variation from Nominal: The variation from nominal values, for Offset or Full Scale Span, as a percent of V_{FSS} at 25 °C.

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MPX5050

- [7] Response Time is defined as the time for the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.
- [8] Warm-up Time is defined as the time required for the product to meet the specified output voltage after the Pressure has been stabilized.
- [9] Offset Stability is the product's output deviation when subjected to 1000 hours of Pulsed Pressure, Temperature Cycling with Bias Test.

6.1 On-chip Temperature Compensation and Calibration

<u>Figure 7</u> illustrates the Differential/Gauge Sensing Chip in the basic chip carrier (Case 867). A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the sensor diaphragm.

The MPX5050/MPXV5050G series pressure sensor operating characteristics, and internal reliability and qualification tests are based on use of dry air as the pressure media. Media, other than dry air, may have adverse effects on sensor performance and long-term reliability. Contact the factory for information regarding media compatibility in your application.

<u>Figure 6</u> shows the sensor output signal relative to pressure input. Typical, minimum, and maximum output curves are shown for operation over a temperature range of 0 °C to 85 °C using the decoupling circuit shown in <u>Figure 8</u>. The output will saturate outside of the specified pressure range.

<u>Figure 8</u> shows the recommended decoupling circuit for interfacing the output of the integrated sensor to the A/D input of a microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

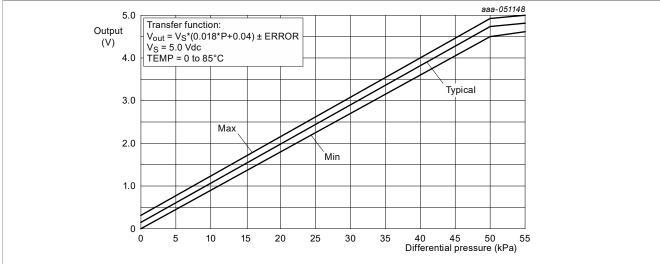
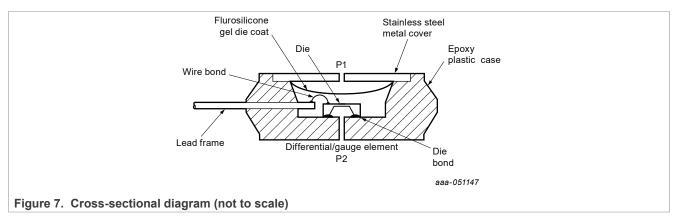


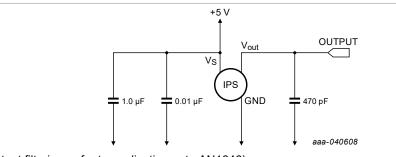
Figure 6. Output vs. pressure differential



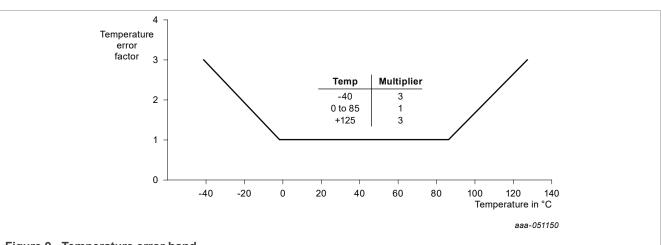
Nominal Transfer Value:

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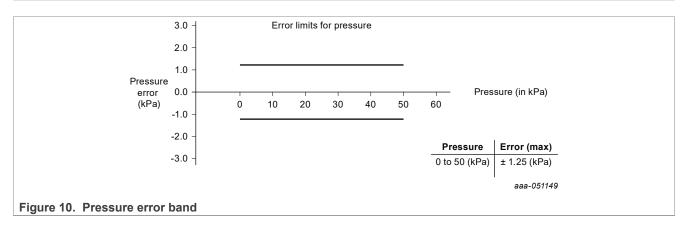
 $V_{OUT} = V_S (P \times 0.018 + 0.04)$ $\pm (Pressure \ Error \times Temp. \ Factor \times 0.018 \quad V_S)$ $V_S = 5.0 \ V \ \pm 0.25 \ Vdc$



(For additional output filtering, refer to application note AN1646) Figure 8. Recommended power supply decoupling and output filtering







6.2 Pressure (P1)/Vacuum (P2) side identification table

NXP Semiconductors designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing fluorosilicone gel which protects the die from harsh media. The MPX pressure sensor is designed to operate with positive differential pressure applied, P1 > P2.

The Pressure (P1) side may be identified by using <u>Table 7</u>:

Table 7. Pressure (P1) side identification

Part Number	Case Type	Pressure (P1) Side Identifier
MPX5050DP	867C	Side with Part Marking
MPXV5050GP	1369	Side with Port Attached
MPXV5050DP	1351	Side with Part Marking
MPXV5050GC6/T1	482A	Vertical Port Attached

7 Package outline

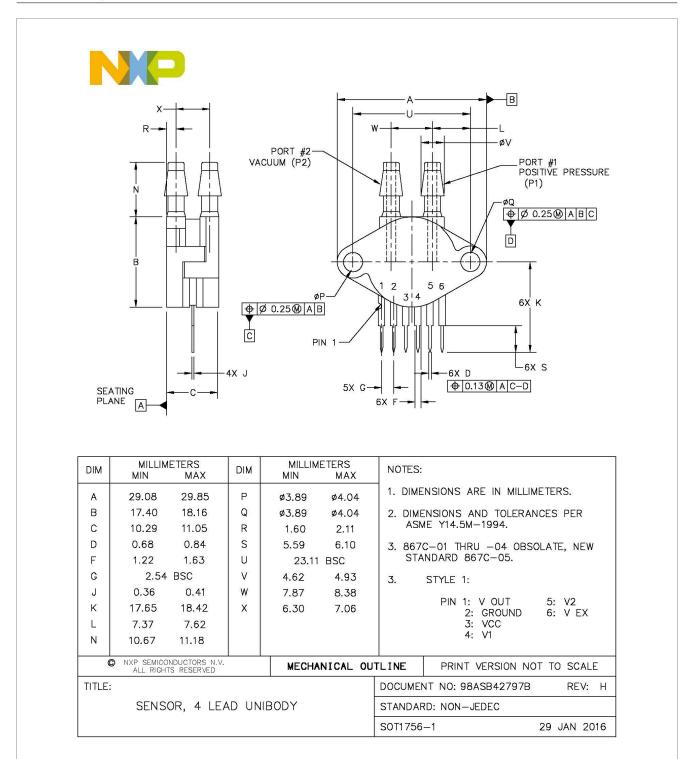


Figure 11. MPX5050DP - SOT17560-1 - Case 867C package outline ¹

¹ Refer to <u>Section 4.2 "Pin description"</u>, <u>Table 3</u>

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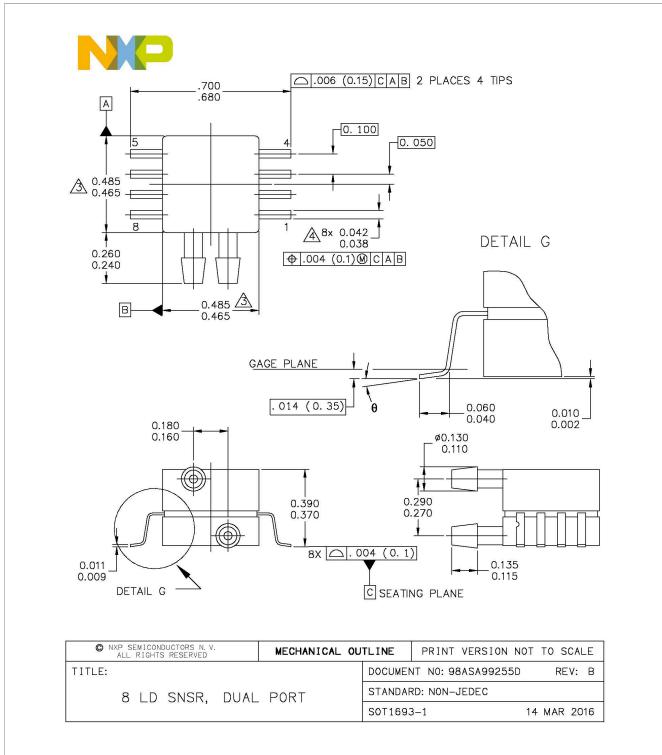


Figure 12. MPX5050DP - SOT1693-1 - Case 1351-01 package outline

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NOTES:			
1. CONTROLLING DIMENSION: INCH			
2. INTERPRET DIMENSIONS AND TOL	ERANCES PER ASME	Y14.5M-	1994.
A DIMENSIONS DO NOT INCLUDE MO MOLD FLASH AND PROTRUSIONS	DLD FLASH OR PPRO SHALL NOT EXCEED	TRUSIONS	S. R SIDE.
A DIMENSION DOES NOT INCLUDE D PROTRUSION SHALL BE .008 MA	AMBAR PROTRUSION XIMUM.	I. ALLOWA	BLE DAMBAR
STYLE 1: PIN 1: PIN 2: PIN 3: PIN 4: PIN 5:	GND +Vout Vs -Vout	E 2: PIN 1: PIN 2: PIN 3: PIN 4: PIN 5:	Vs GND Vout
PIN 6. PIN 7: PIN 7: PIN 8:	N/C N/C	PIN 5. PIN 6: PIN 7: PIN 8:	N/C N/C
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² Style 1 is not applicable for the parts covered by this data sheet.

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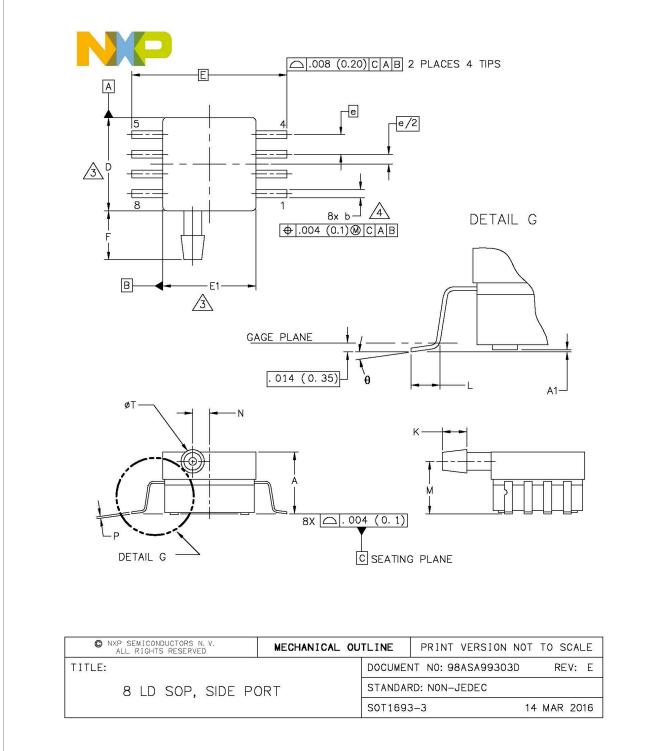


Figure 14. MPX5050GP - SOT1693-3 - Case 1369-01 package outline

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NOTES:

- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

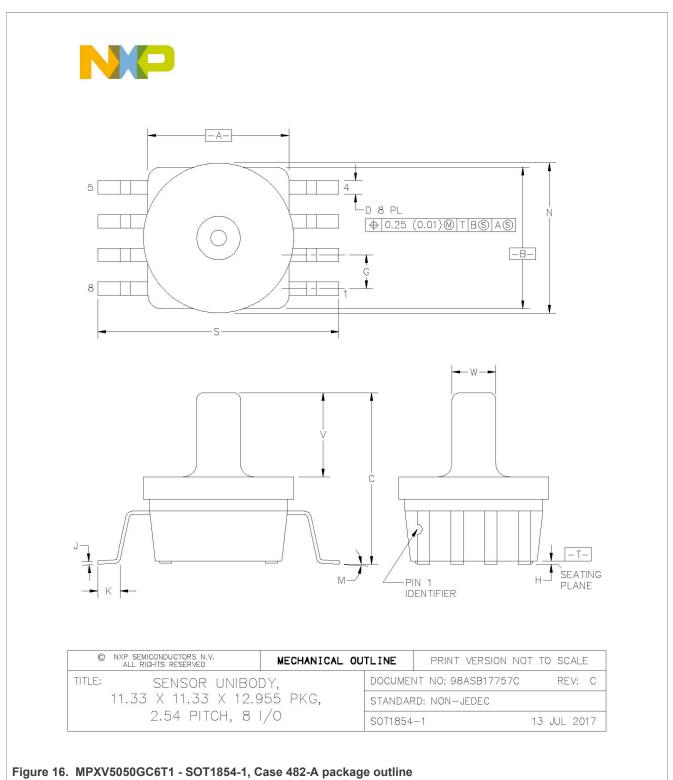
A DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.

A DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

	INC	HES	MILLIMETERS			11	NCHES	MILLI	METERS
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
А	.300	.330	7.62	8.38	θ	0.	7'	0.	7.
A1	.002	.010	0.05	0.25	=				
ь	.038	.042	0.96	1.07			· · · · · · · · · · · · · · · · · · ·		
D	.465	.485	11.81	12.32	-				
E	.717	BSC	18	.21 BSC	-				
E1	.465	.485	11.81	12.32	-				
е	.100	BSC	2.	54 BSC	<u></u>		19 <u>11</u> 11		<u></u>
F	.245	.255	6.22	6.47	-				
К	.120	.130	3.05	3.30	-				
L.	.061	.071	1.55	1.80	-				
м	.270	.290	6.86	7.36	-				
Ν	.080	.090	2.03	2.28	-				
Ρ	.009	.011	0.23	0.28	-		1 <u></u> 1		
Т	.115	.125	2.92	3.17					
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Figure 15. MPX5050GP - SOT1693-3 - Case 1369-01 package outline notes

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NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSION 'A' AND 'B' DO NOT INCLUDE MOLD PROTUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
- 5. ALL VERTICAL SURFACES 5' TYPICAL DRAFT.

	INCH	IES	MILLI	METERS			
DIM	MIN	MAX	MIN	MAX			
А	0.415	0.425	10.54	10.79			
В	0.415	0.425	10.54	10.79			
С	0.500	0.520	12.70	13.21			
D	0.038	0.042	0.96	1.07			
G	0.100	BSC	2.54	BSC			
Н	0.002	0.010	0.05	0.25			
J	0.009	0.011	0.23	0.28			
К	0.061	0.071	1.55	1.80			
М	0°	7°	0°	7°			
N	0.444	0.448	11.28	11.38			
S	0.709	0.725	18.01	18.41			
V	0.245	0.255	6.22	6.48			
W	0.115	0.125	2.92	3.17			
	NVD CENICOND	UCTORS N.V.				Ĩ	
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	2.5	54 PITCH	H, 8 I/(C	SOT1854	1	13 JUL 2017

Figure 17. MPXV5050GC6T1 - SOT1854-1, Case 482-A package outline notes

8 Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MPX5050 v.12	20230609	Product data sheet		MPX5050 v.11
Modifications	guidelines of NXF name where appr Revised all image <u>Section 3</u> , remove MPVZ5050GW7U <u>Section 3.1</u> , inser <u>Section 4</u> , <u>Section</u> <u>Section 5</u> , renam <u>Semiconductors 6</u> <u>Section 6</u> , renam	ropriate. es to conform to NXP Se ed MPX505D, MPX505C J from the table. rted new table. <u>n 4.1</u> , and <u>Section 4.2</u> , ir ed "Maximum ratings" so document heirarchy for o	I texts have been ad miconductor image GP, MPX505GP1, Ministred new sections ection to "Limiting valuata sheets. istics" to "Recomme D and MPX5050GP	apted to the new company guidelines. PXV5050GC6U and s. llues" to conform to NXP nded operating conditions".

9 Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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MPX5050

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Integrated silicon pressure sensor, on-chip signal conditioned, temperature compensated and calibrated

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