



BTA/BTB08 and T8 Series

SNUBBERLESS™, LOGIC LEVEL & STANDARD

8A TRIACs

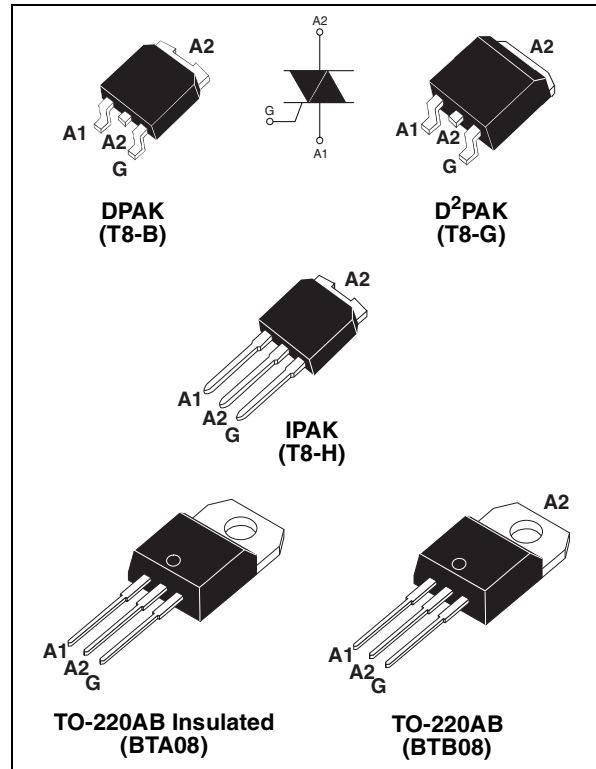
MAIN FEATURES:

Symbol	Value	Unit
$I_{T(RMS)}$	8	A
V_{DRM}/V_{RRM}	600 and 800	V
$I_{GT}(Q_1)$	5 to 50	mA

DESCRIPTION

Available either in through-hole or surface-mount packages, the BTA/BTB08 and T8 triac series is suitable for general purpose AC switching. They can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits... or for phase control operation in light dimmers, motor speed controllers,...

The snubberless versions (BTA/BTB...W and T8 series) are specially recommended for use on inductive loads, thanks to their high commutation performances. By using an internal ceramic pad, the BTA series provides voltage insulated tab (rated at 2500V RMS) complying with UL standards (File ref.: E81734)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		Value	Unit	
$I_{T(RMS)}$	RMS on-state current (full sine wave)	DPAK / D ² PAK IPAK / TO-220AB $T_c = 110^\circ\text{C}$	8	A
		TO-220AB Ins. $T_c = 100^\circ\text{C}$		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	F = 50 Hz t = 20 ms	80	A
		F = 60 Hz t = 16.7 ms	84	
I^2t	I^2t Value for fusing	tp = 10 ms	36	A ² s
di/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, tr ≤ 100 ns	F = 120 Hz $T_j = 125^\circ\text{C}$	50	A/μs
I_{GM}	Peak gate current	tp = 20 μs $T_j = 125^\circ\text{C}$	4	A
$P_{G(AV)}$	Average gate power dissipation	$T_j = 125^\circ\text{C}$	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range		- 40 to + 150 - 40 to + 125	°C

BTA/BTB08 and T8 Series

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise specified)

■ SNUBBERLESS™ and LOGIC LEVEL (3 Quadrants)

Symbol	Test Conditions	Quadrant		T8		BTA/BTB08				Unit
				T810	T835	TW	SW	CW	BW	
I _{GT} (1)	V _D = 12 V R _L = 30 Ω	I - II - III	MAX.	10	35	5	10	35	50	mA
V _{GT}		I - II - III	MAX.	1.3						V
V _{GD}	V _D = V _{DRM} R _L = 3.3 kΩ T _j = 125°C	I - II - III	MIN.	0.2						V
I _H (2)	I _T = 100 mA		MAX.	15	35	10	15	35	50	mA
I _L	I _G = 1.2 I _{GT}	I - III	MAX.	25	50	10	25	50	70	mA
		II		30	60	15	30	60	80	
dV/dt (2)	V _D = 67 %V _{DRM} gate open T _j = 125°C		MIN.	40	400	20	40	400	1000	V/μs
(dl/dt) _c (2)	(dV/dt) _c = 0.1 V/μs T _j = 125°C		MIN.	5.4	-	3.5	5.4	-	-	A/ms
	(dV/dt) _c = 10 V/μs T _j = 125°C			2.8	-	1.5	2.8	-	-	
	Without snubber T _j = 125°C			-	4.5	-	-	4.5	7	

■ STANDARD (4 Quadrants)

Symbol	Test Conditions	Quadrant		BTA/BTB08		Unit
				C	B	
I _{GT} (1)	V _D = 12 V R _L = 30 Ω	I - II - III IV	MAX.	25 50	50 100	mA
V _{GT}		ALL	MAX.	1.3		V
V _{GD}	V _D = V _{DRM} R _L = 3.3 kΩ T _j = 125°C	ALL	MIN.	0.2		V
I _H (2)	I _T = 500 mA		MAX.	25	50	mA
I _L	I _G = 1.2 I _{GT}	I - III - IV	MAX.	40	50	mA
		II		80	100	
dV/dt (2)	V _D = 67 %V _{DRM} gate open T _j = 125°C		MIN.	200	400	V/μs
(dV/dt) _c (2)	(dl/dt) _c = 3.5 A/ms T _j = 125°C		MIN.	5	10	V/μs

STATIC CHARACTERISTICS

Symbol	Test Conditions			Value	Unit
V _{TM} (2)	I _{TM} = 11 A t _p = 380 μs	T _j = 25°C	MAX.	1.55	V
V _{to} (2)	Threshold voltage	T _j = 125°C	MAX.	0.85	V
R _d (2)	Dynamic resistance	T _j = 125°C	MAX.	50	mΩ
I _{DRM}	V _{DRM} = V _{RRM}	T _j = 25°C	MAX.	5	μA
I _{RRM}		T _j = 125°C		1	mA

Note 1: minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: for both polarities of A2 referenced to A1

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit	
$R_{th(j-c)}$	Junction to case (AC)		DPAK / D ² PAK IPAK / TO-220AB	1.6	°C/W
			TO-220AB Insulated	2.5	
$R_{th(j-a)}$	Junction to ambient	S = 1 cm ²	D ² PAK	45	°C/W
		S = 0.5 cm ²	DPAK	70	
			TO-220AB TO-220AB Insulated	60	
			IPAK	100	

S = Copper surface under tab

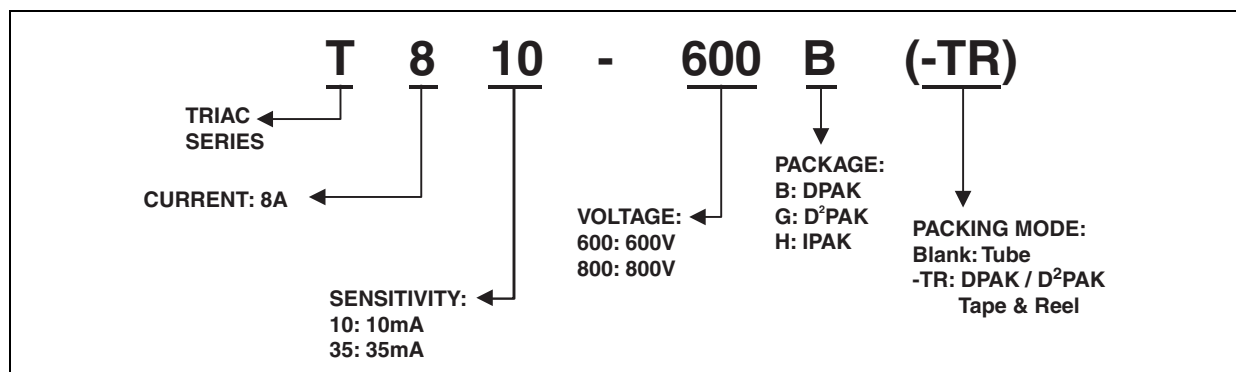
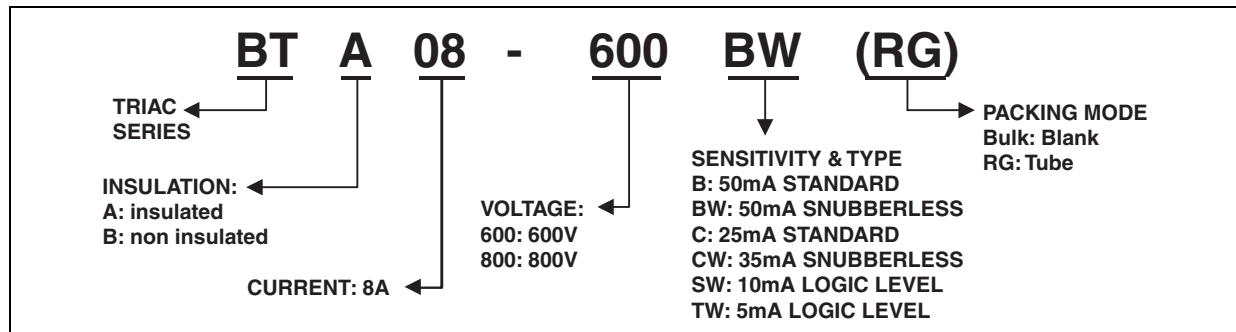
PRODUCT SELECTOR

Part Number	Voltage (xxx)		Sensitivity	Type	Package
	600 V	800 V			
BTA/BTB08-xxxB	X	X	50 mA	Standard	TO-220AB
BTA/BTB108-xxxBW	X	X	50 mA	Snubberless	TO-220AB
BTA/BTB08-xxxC	X	X	25 mA	Standard	TO-220AB
BTA/BTB08-xxxCW	X	X	35 mA	Snubberless	TO-220AB
BTA/BTB08-xxxSW	X	X	10 mA	Logic level	TO-220AB
BTA/BTB08-xxxTW	X	X	5 mA	Logic level	TO-220AB
T810-xxxB	X	X	10 mA	Logic level	DPAK
T810-xxxH	X	X	10 mA	Logic level	IPAK
T810-xxxG	X	X	10 mA	Logic level	D ² PAK
T835-xxxB	X	X	35mA	Snubberless	DPAK
T835-xxxG	X	X	35 mA	Snubberless	D ² PAK
T835-xxxH	X	X	35 mA	Snubberless	IPAK

BTB: non insulated TO-220AB package

BTA/BTB08 and T8 Series

ORDERING INFORMATION



OTHER INFORMATION

Part Number	Marking	Weight	Base quantity	Packing mode
BTA/BTB08-xxxzy	BTA/BTB08xxxzy	2.3 g	250	Bulk
BTA/BTB08-xxxzyRG	BTA/BTB08-xxxzy	2.3 g	50	Tube
T8yy-xxxB	T8yyxxx	0.3 g	75	Tube
T8yy-xxxB-TR	T8yyxxx	0.3 g	2500	Tape & reel
T8yy-xxxH	T8yyxxx	0.4 g	75	Tube
T8yy-xxxG	T8yyxxx	1.5 g	50	Tube
T8yy-xxxG-TR	T8yyxxx	1.5 g	1000	Tape & reel

Note: xxx = voltage, yy = sensitivity, z = type

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

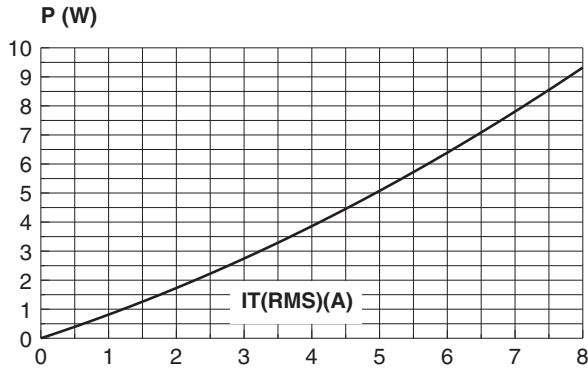


Fig. 2-1: RMS on-state current versus case temperature (full cycle).

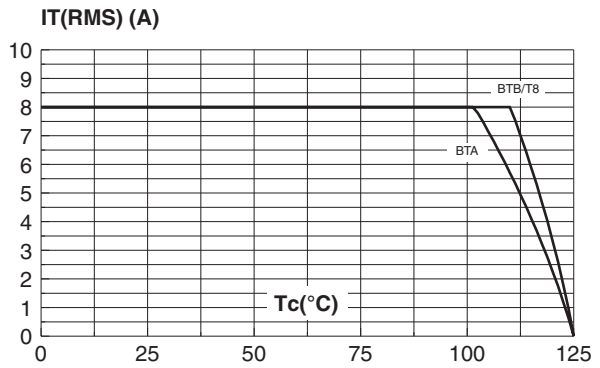


Fig. 2-2: RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm), full cycle.

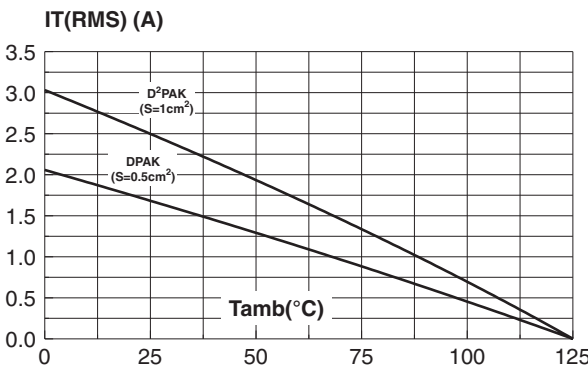


Fig. 3: Relative variation of thermal impedance versus pulse duration.

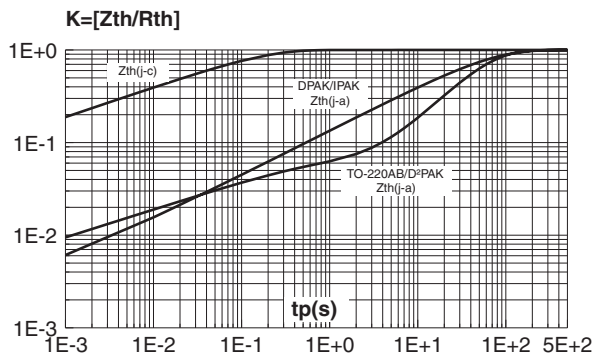


Fig. 4: On-state characteristics (maximum values).

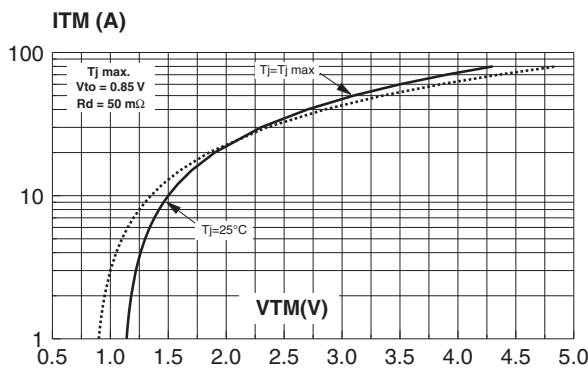


Fig. 5: Surge peak on-state current versus number of cycles.

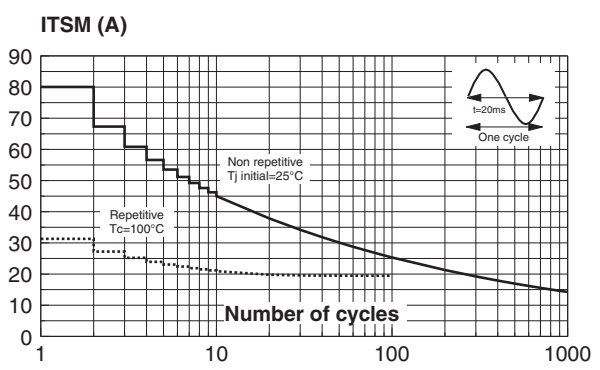


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ms}$, and corresponding value of I^2t .

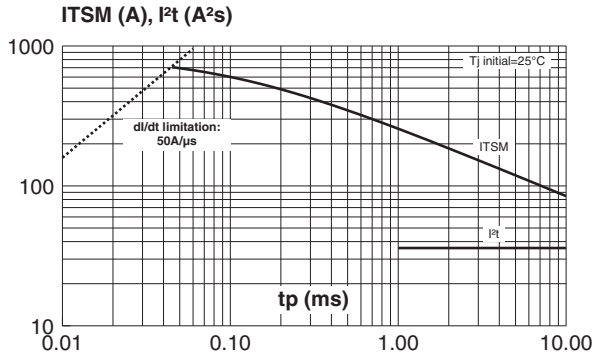


Fig. 8-1: Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values). Snubberless & Logic Level Types

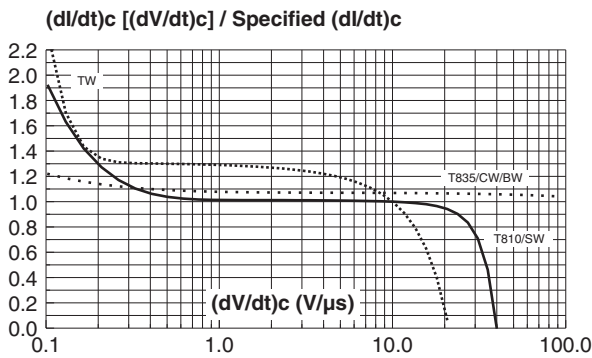


Fig. 9: Relative variation of critical rate of decrease of main current versus junction temperature.

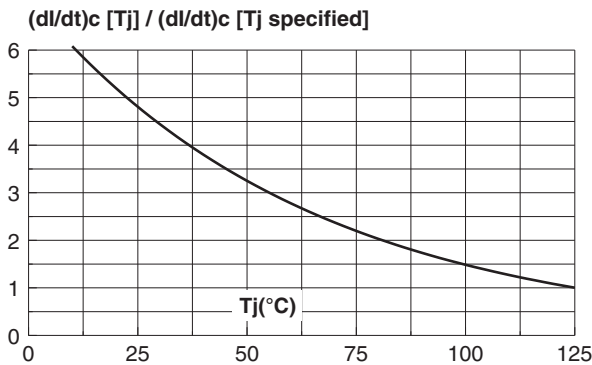


Fig. 7: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

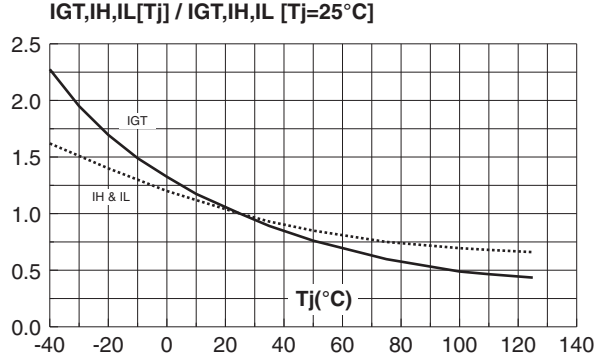


Fig. 8-2: Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values). Standard Types

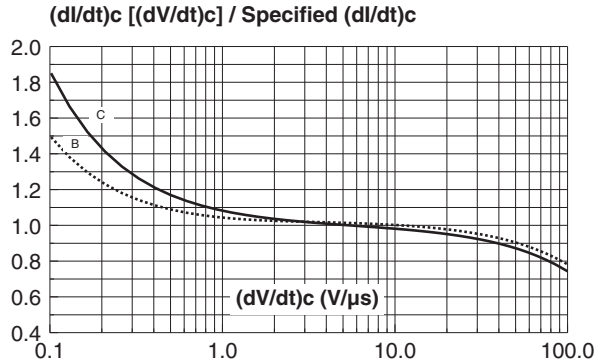
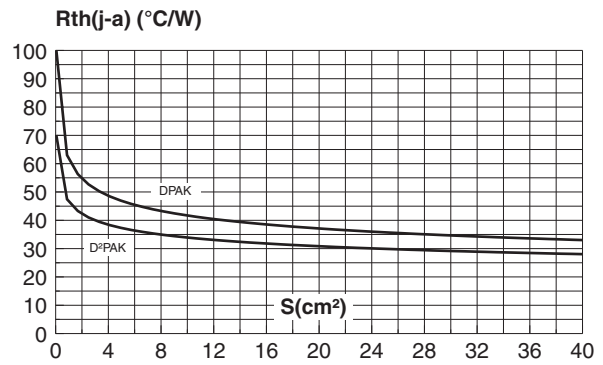
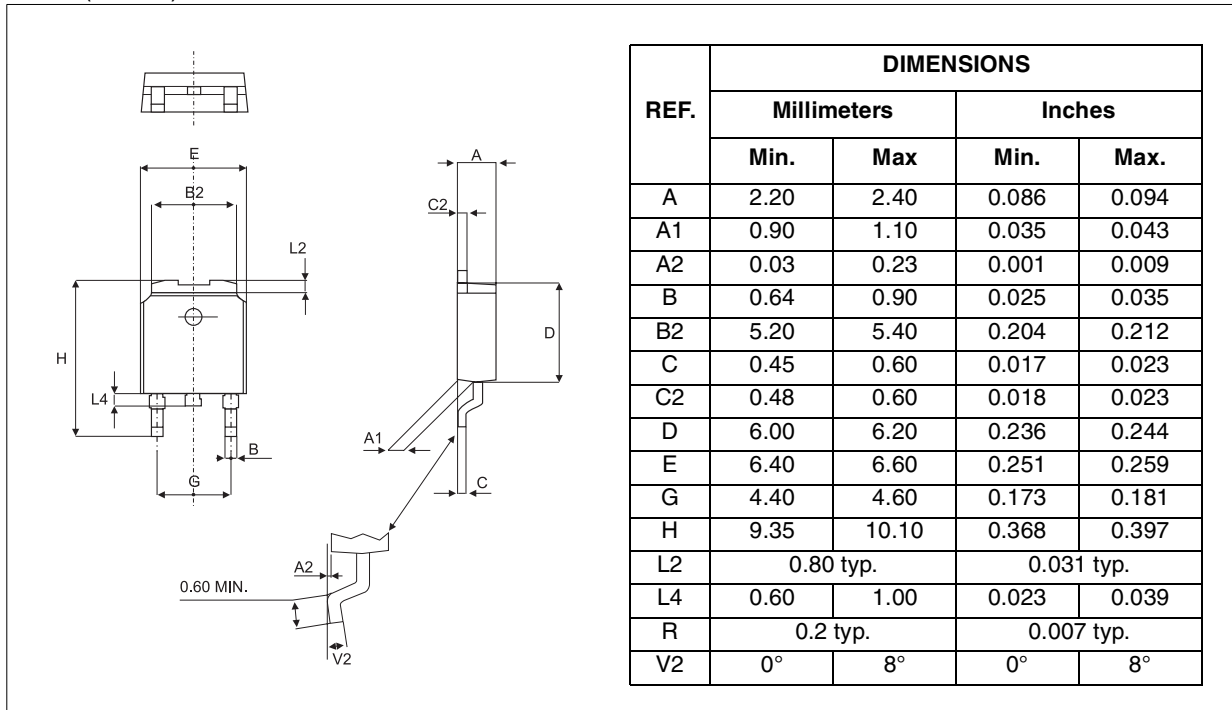


Fig. 10: DPAK and D²PAK Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 µm).



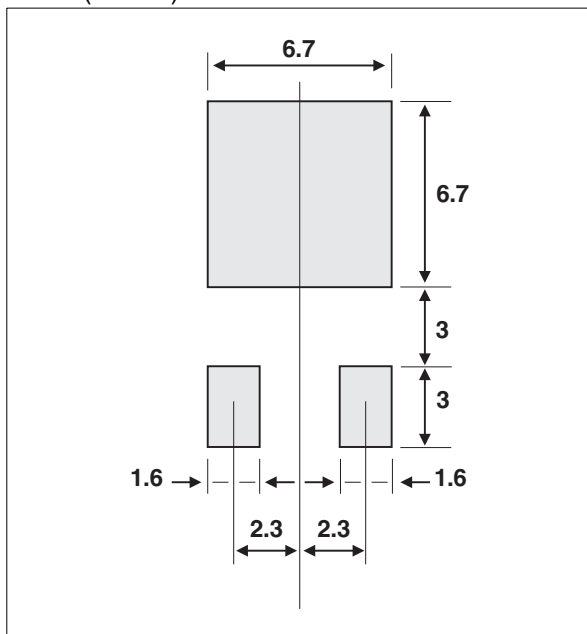
PACKAGE MECHANICAL DATA

DPAK (Plastic)



FOOTPRINT DIMENSIONS (in millimeters)

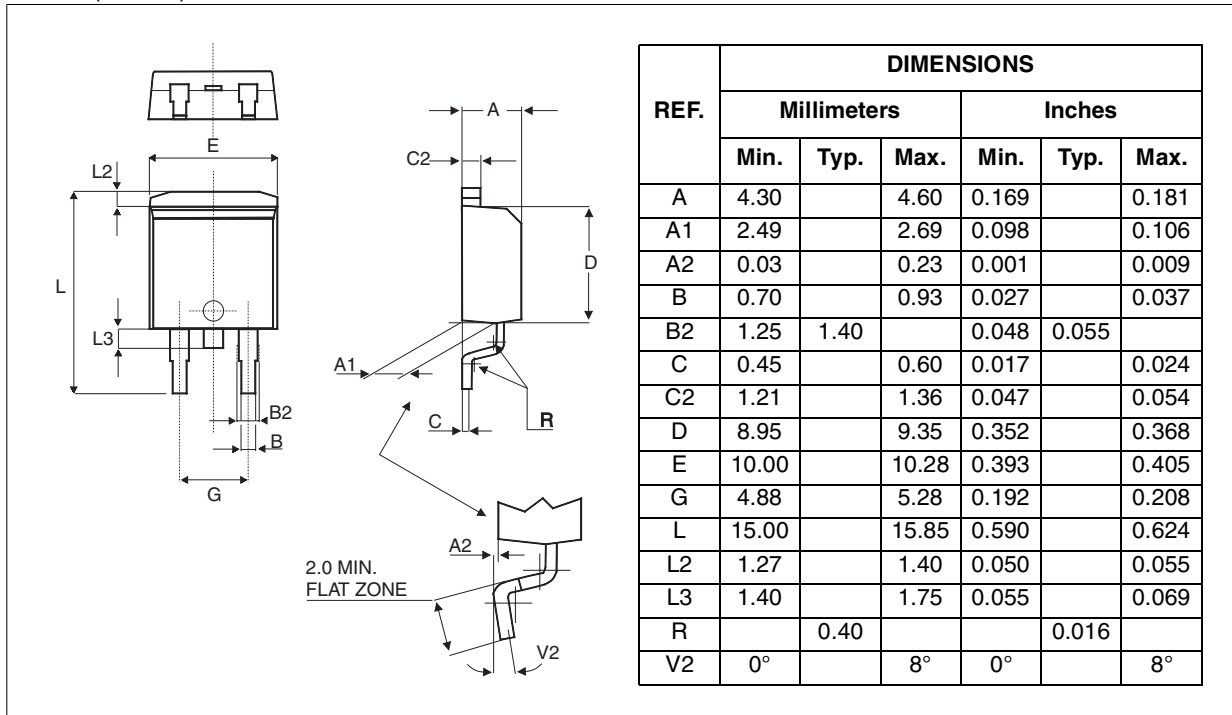
DPAK (Plastic)



BTA/BTB08 and T8 Series

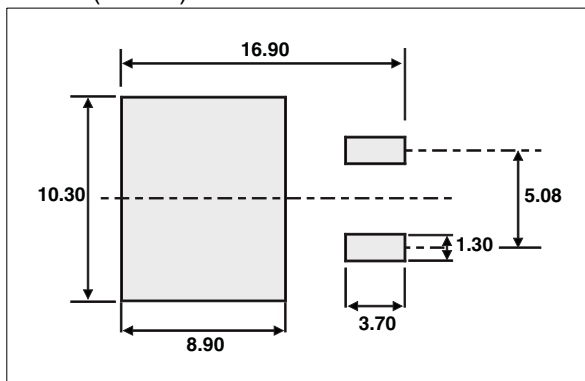
PACKAGE MECHANICAL DATA

D²PAK (Plastic)



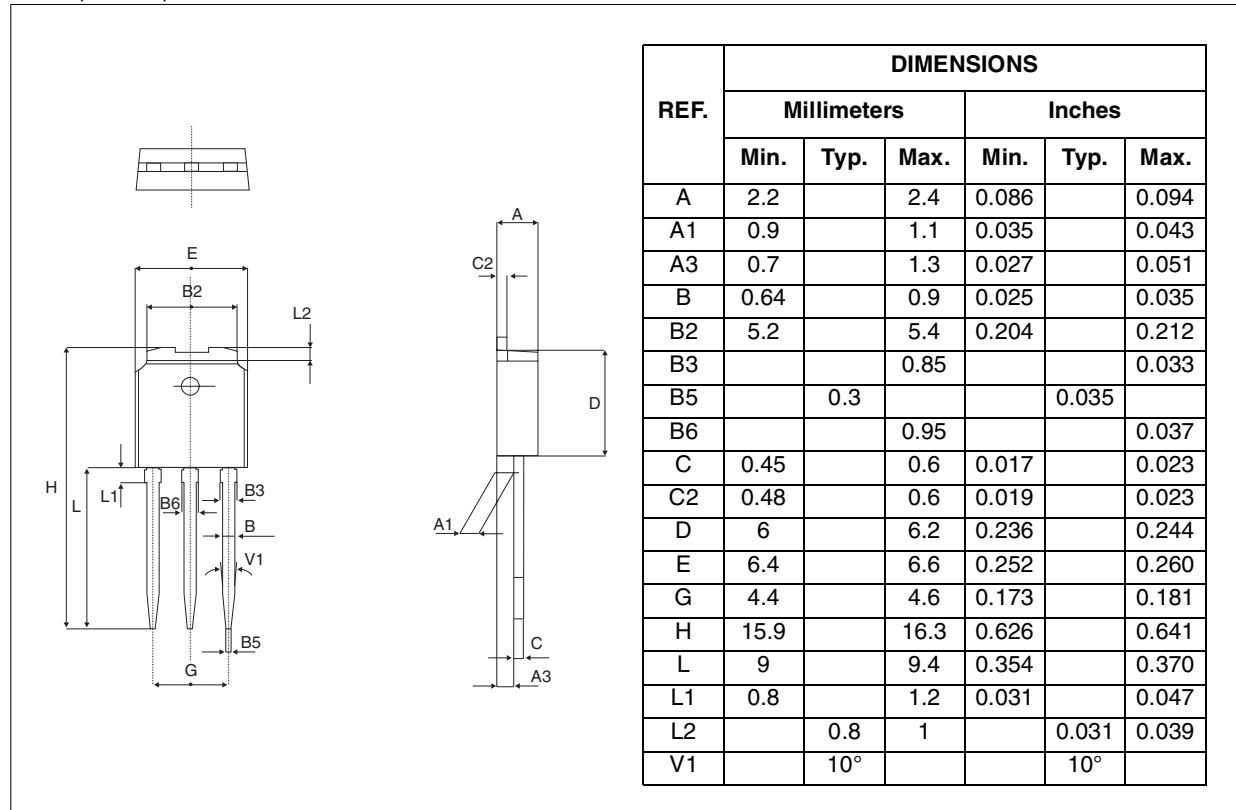
FOOTPRINT DIMENSIONS (in millimeters)

D²PAK (Plastic)



PACKAGE MECHANICAL DATA

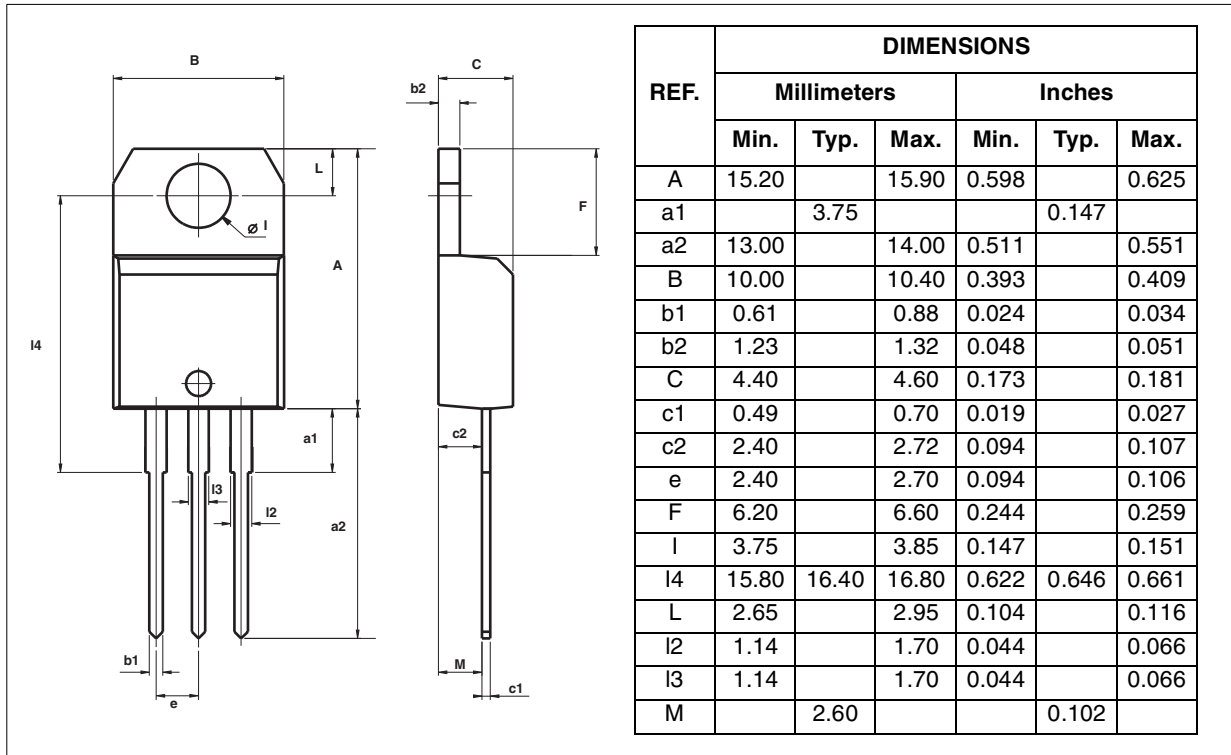
IPAK (Plastic)



BTA/BTB08 and T8 Series

PACKAGE MECHANICAL DATA

TO-220AB Ins.



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.
All other names are the property of their respective owners

© 2003 STMicroelectronics - All rights reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States

www.st.com