SLAS344D − JANUARY 2002 − REVISED AUGUST 2004

- **Low Supply-Voltage Range, 1.8 V to 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 280 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 1.1 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Five Power Saving Modes**
- **Wake-Up From Standby Mode in less than 6 μs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **12-Bit A/D Converter With Internal Reference, Sample-and-Hold and Autoscan Feature**
- **16-Bit Timer_B With Three† or Seven‡ Capture/Compare-With-Shadow Registers**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **On-Chip Comparator**
- **Serial Communication Interface (USART), Select Asynchronous UART or Synchronous SPI by Software:**
  - **Two USARTs (USART0, USART1) — MSP430x44x Devices**
  - **One USART (USART0) — MSP430x43x Devices**
- **Brownout Detector**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Integrated LCD Driver for Up to 160 Segments**
- **Family Members Include:**
  - **MSP430F435: 16KB+256B Flash Memory, 512B RAM**
  - **MSP430F436: 24KB+256B Flash Memory, 1KB RAM**
  - **MSP430F437: 32KB+256B Flash Memory, 1KB RAM**
  - **MSP430F447: 32KB+256B Flash Memory, 1KB RAM**
  - **MSP430F448: 48KB+256B Flash Memory, 2KB RAM**
  - **MSP430F449: 60KB+256B Flash Memory, 2KB RAM**
- **For Complete Module Descriptions, See The *MSP430x4xx Family User's Guide*, Literature Number SLAU056**

† 'F435, 'F436, and 'F437 devices

‡ 'F447, 'F448, and 'F449 devices

description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6μs.

The MSP430x43x and the MSP430x44x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, one or two universal serial synchronous/asynchronous communication interfaces (USART), 48 I/O pins, and a liquid crystal driver (LCD) with up to 160 segments.

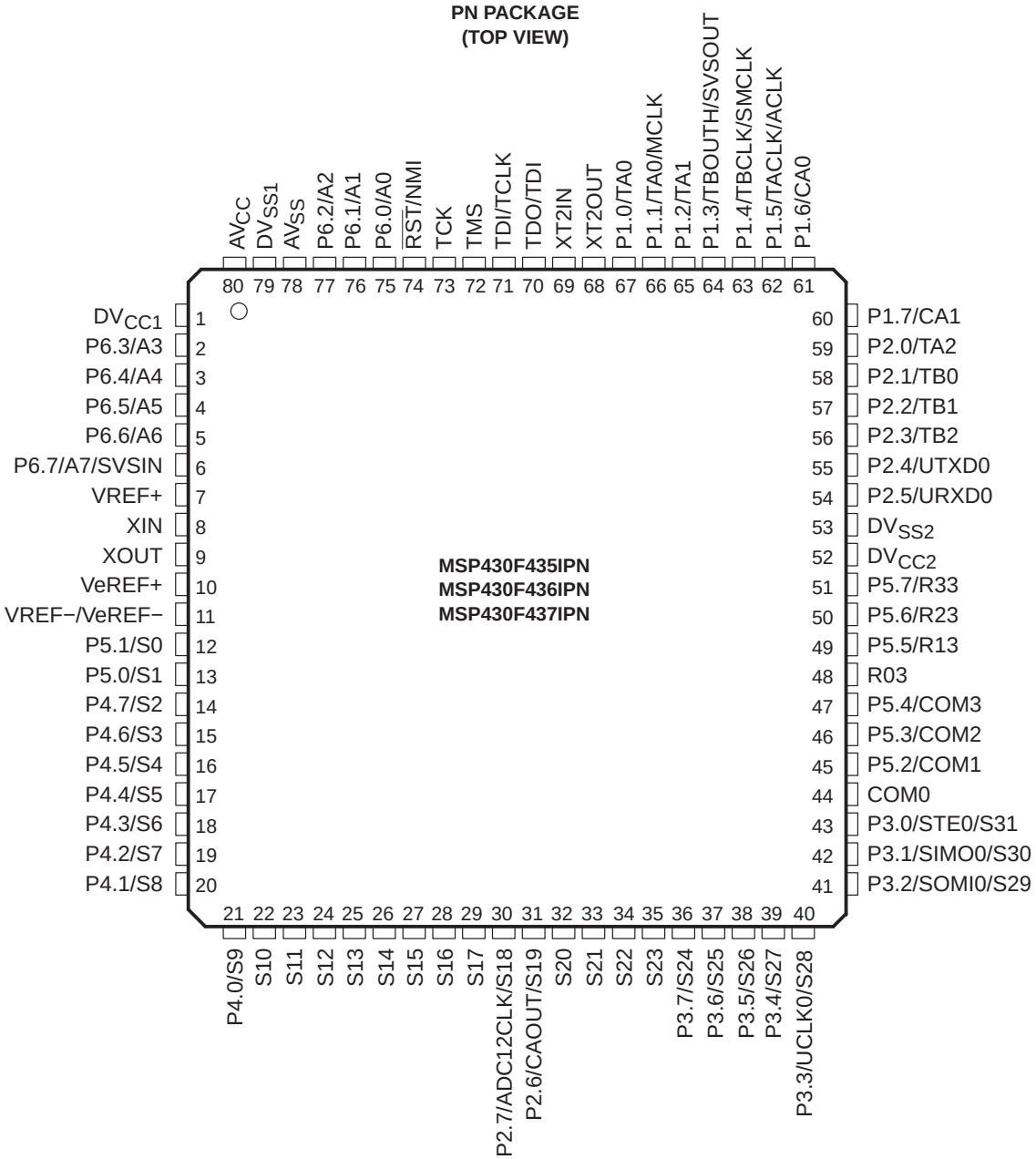
Typical applications include sensor systems that capture analog signals, convert them to digital values, and process and transmit the data to a host system, or process this data and displays it on a LCD panel. The timers make the configurations ideal for industrial control applications such as ripple counters, digital motor control, EE-meters, hand-held meters, etc. The hardware multiplier enhances the performance and offers a broad code and hardware-compatible family solution.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC 80-PIN QFP (PN)	PLASTIC 100-PIN QFP (PZ)
−40°C to 85°C	MSP430F435IPN MSP430F436IPN MSP430F437IPN	MSP430F435IPZ MSP430F436IPZ MSP430F437IPZ MSP430F447IPZ MSP430F448IPZ MSP430F449IPZ

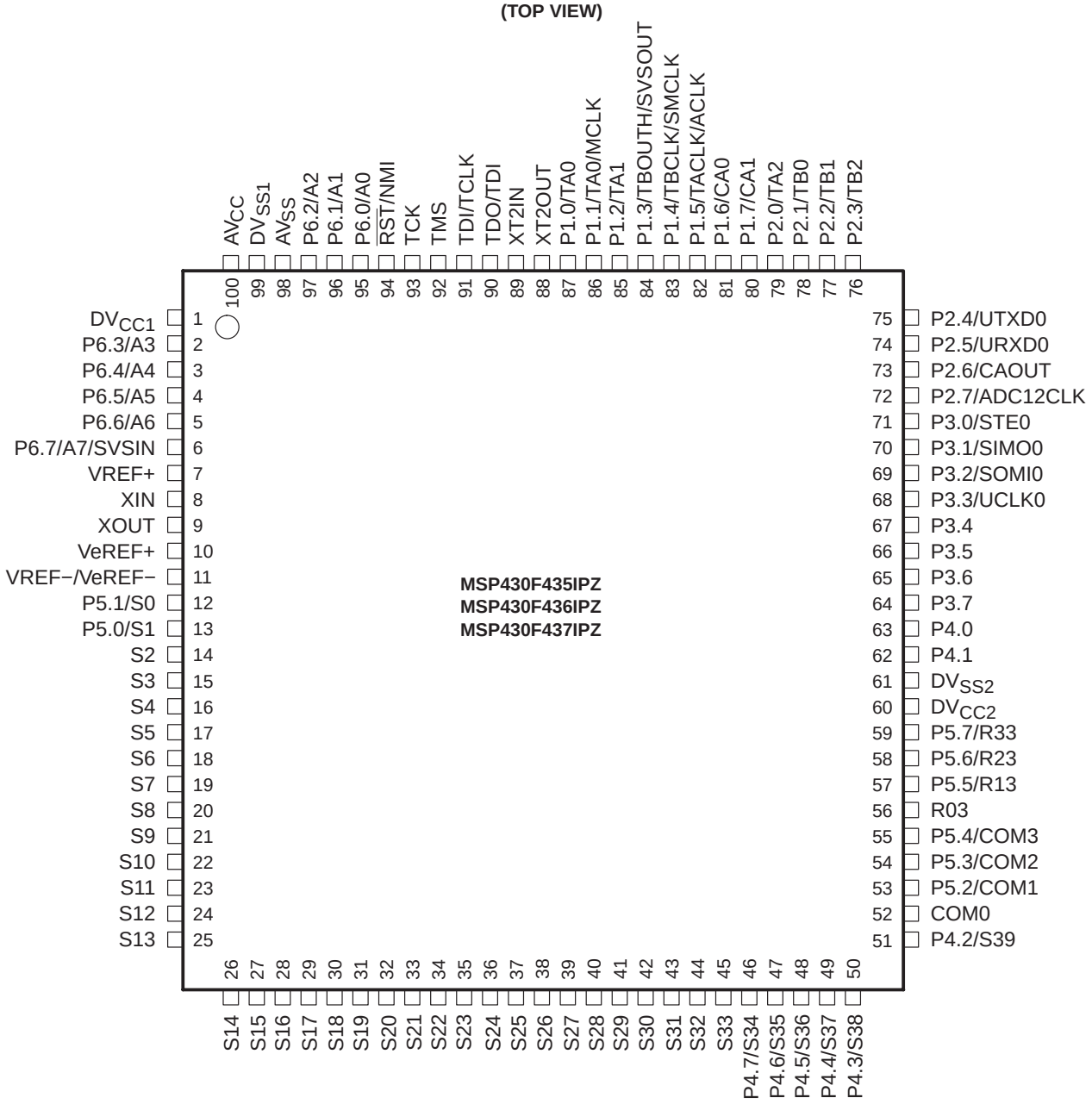
pin designation, MSP430x435IPN, MSP430x436IPN, MSP430x437IPN

PN PACKAGE
(TOP VIEW)



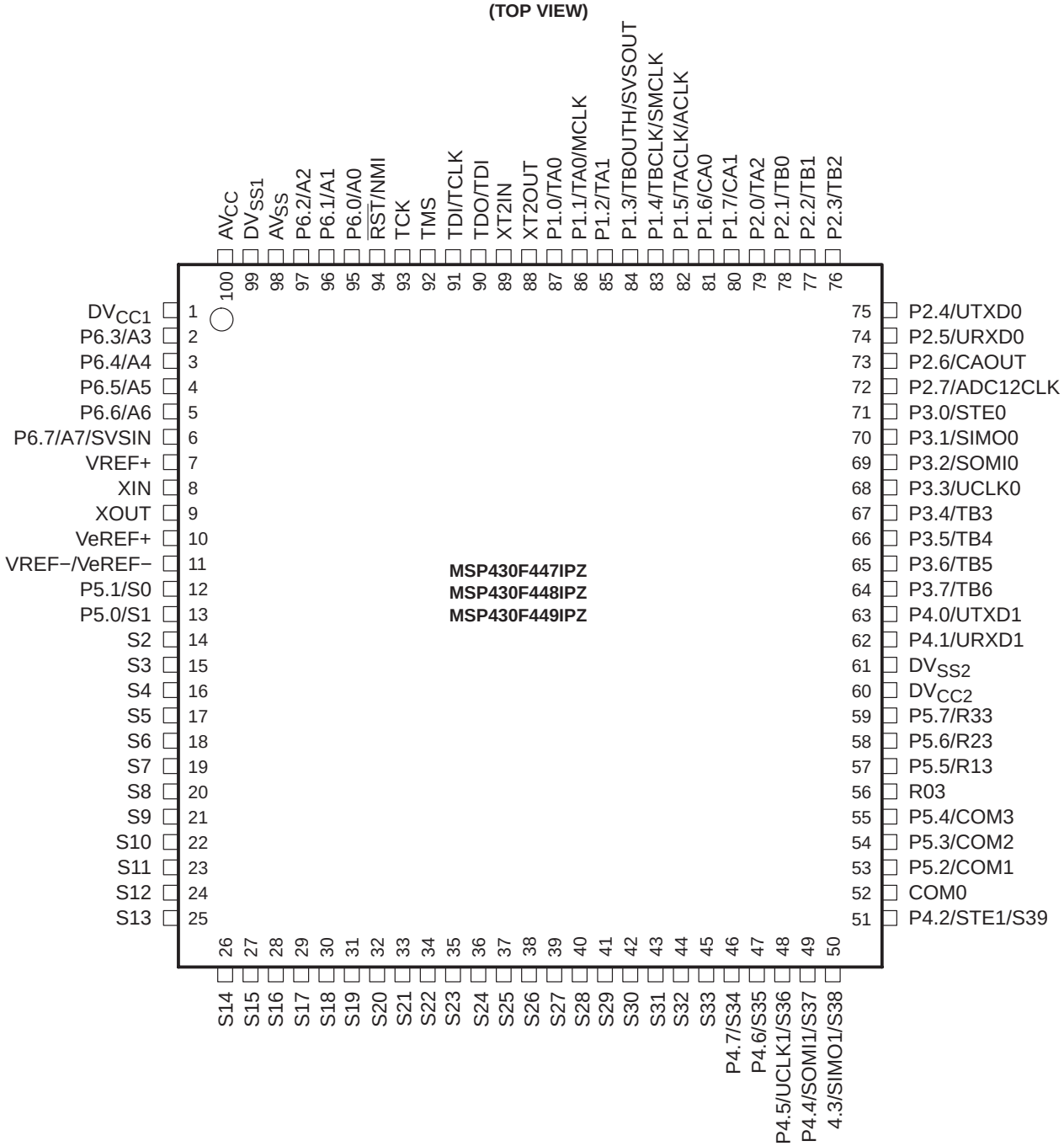
pin designation, MSP430x435IPZ, MSP430x436IPZ, MSP430x437IPZ

PZ PACKAGE
(TOP VIEW)

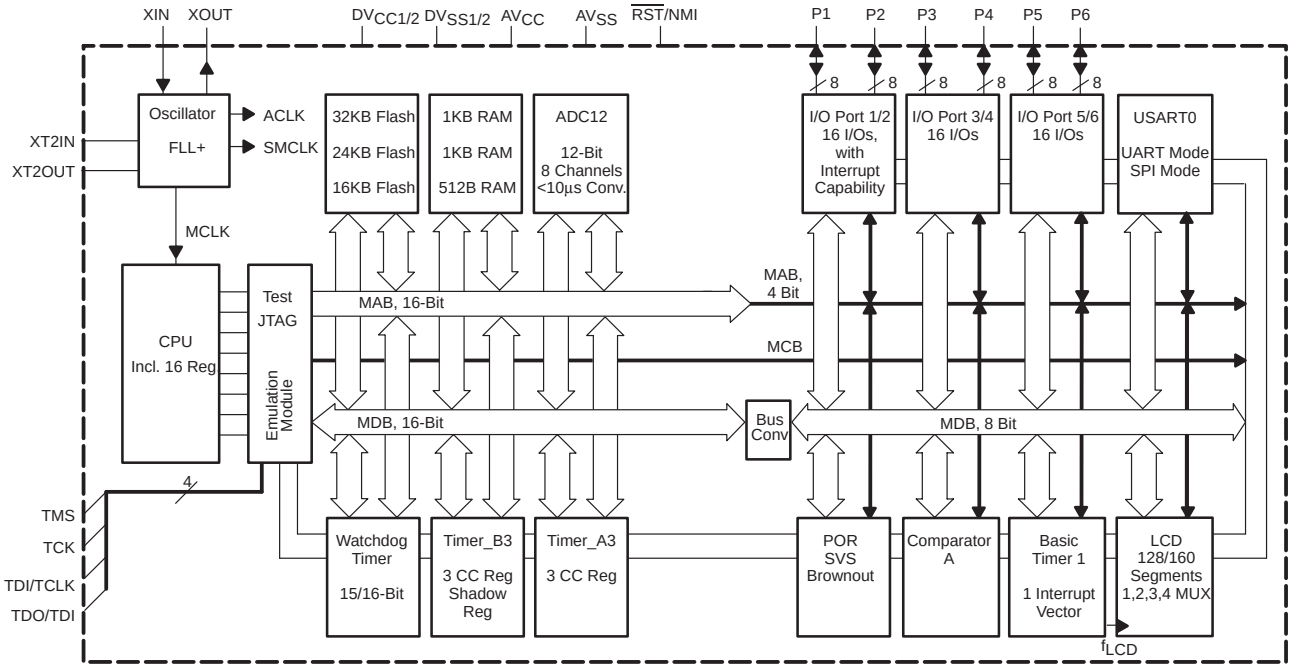


pin designation, MSP430x447IPZ, MSP430x448IPZ, MSP430x449IPZ

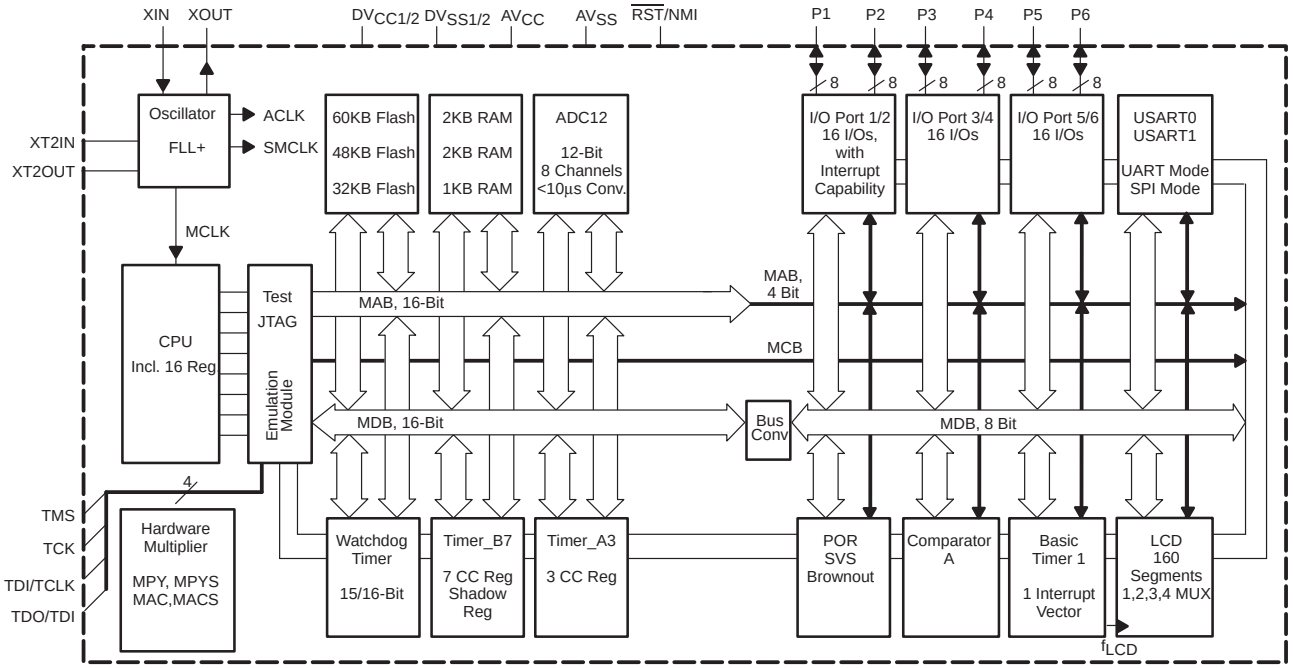
PZ PACKAGE
(TOP VIEW)



MSP430x43x functional block diagrams



MSP430x44x functional block diagrams



MSP430x43x Terminal Functions

TERMINAL					DESCRIPTION
PN		I/O	PZ		I/O	
NAME	NO.		NAME	NO.		
DV_{CC1}	1		DV_{CC1}	1		Digital supply voltage, positive terminal.
P6.3/A3	2	I/O	P6.3/A3	2	I/O	General-purpose digital I/O / analog input a3—12-bit ADC
P6.4/A4	3	I/O	P6.4/A4	3	I/O	General-purpose digital I/O / analog input a4—12-bit ADC
P6.5/A5	4	I/O	P6.5/A5	4	I/O	General-purpose digital I/O / analog input a5—12-bit ADC
P6.6/A6	5	I/O	P6.6/A6	5	I/O	General-purpose digital I/O / analog input a6—12-bit ADC
P6.7/A7/SVSIN	6	I/O	P6.7/A7/SVSIN	6	I/O	General-purpose digital I/O / analog input a7—12-bit ADC, analog / input to brownout, supply voltage supervisor
V_{REF+}	7	O	V_{REF+}	7	O	Output of positive terminal of the reference voltage in the ADC
XIN	8	I	XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	XOUT	9	O	Output terminal of crystal oscillator XT1
Ve_{REF+}	10	I	Ve_{REF+}	10	I	Input for an external reference voltage to the ADC
V_{REF-}/Ve_{REF-}	11	I	V_{REF-}/Ve_{REF-}	11	I	Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage.
P5.1/S0	12	I/O	P5.1/S0	12	I/O	General-purpose digital I/O / LCD segment output 0
P5.0/S1	13	I/O	P5.0/S1	13	I/O	General-purpose digital I/O / LCD segment output 1
P4.7/S2	14	I/O	S2	14	O	General-purpose digital I/O / LCD segment output 2
P4.6/S3	15	I/O	S3	15	O	General-purpose digital I/O / LCD segment output 3
P4.5/S4	16	I/O	S4	16	O	General-purpose digital I/O / LCD segment output 4
P4.4/S5	17	I/O	S5	17	O	General-purpose digital I/O / LCD segment output 5
P4.3/S6	18	I/O	S6	18	O	General-purpose digital I/O / LCD segment output 6
P4.2/S7	19	I/O	S7	19	O	General-purpose digital I/O / LCD segment output 7
P4.1/S8	20	I/O	S8	20	O	General-purpose digital I/O / LCD segment output 8
P4.0/S9	21	I/O	S9	21	O	General-purpose digital I/O / LCD segment output 9
S10	22	O	S10	22	O	LCD segment output 10
S11	23	O	S11	23	O	LCD segment output 11
S12	24	O	S12	24	O	LCD segment output 12
S13	25	O	S13	25	O	LCD segment output 13
S14	26	O	S14	26	O	LCD segment output 14
S15	27	O	S15	27	O	LCD segment output 15
S16	28	O	S16	28	O	LCD segment output 16
S17	29	O	S17	29	O	LCD segment output 17
P2.7/ADC12CLK/ S18	30	I/O	S18	30	O	General-purpose digital I/O / conversion clock—12-bit ADC / LCD segment output 18
P2.6/CAOUT/S19	31	I/O	S19	31	O	General-purpose digital I/O / Comparator_A output / LCD segment output 19
S20	32	O	S20	32	O	LCD segment output 20
S21	33	O	S21	33	O	LCD segment output 21
S22	34	O	S22	34	O	LCD segment output 22
S23	35	O	S23	35	O	LCD segment output 23
P3.7/S24	36	I/O	S24	36	O	General-purpose digital I/O / LCD segment output 24
P3.6/S25	37	I/O	S25	37	O	General-purpose digital I/O / LCD segment output 25
P3.5/S26	38	I/O	S26	38	O	General-purpose digital I/O / LCD segment output 26
P3.4/S27	39	I/O	S27	39	O	General-purpose digital I/O / LCD segment output 27

MSP430x43x Terminal Functions (Continued)

TERMINAL						DESCRIPTION
PN		I/O	PZ		I/O	
NAME	NO.		NAME	NO.		
P3.3/UCLK0/S28	40	I/O	S28	40	O	General-purpose digital I/O / ext. clock i/p—USART0/UART or SPI mode, clock o/p—USART0/SPI mode / LCD segment output 28
P3.2/SOMI0/S29	41	I/O	S29	41	O	General-purpose digital I/O / slave out/master in of USART0/SPI mode / LCD segment output 29
P3.1/SIMO0/S30	42	I/O	S30	42	O	General-purpose digital I/O / slave out/master out of USART0/SPI mode / LCD segment output 30
P3.0/STE0/S31	43	I/O	S31	43	O	General-purpose digital I/O / slave transmit enable-USART0/SPI mode / LCD segment output 31
			S32	44	O	LCD segment output 32
			S33	45	O	LCD segment output 33
			P4.7/S34	46	I/O	General-purpose digital I/O / LCD segment output 34
			P4.6/S35	47	I/O	General-purpose digital I/O / LCD segment output 35
			P4.5/S36	48	I/O	General-purpose digital I/O / LCD segment output 36
			P4.4/S37	49	I/O	General-purpose digital I/O / LCD segment output 37
			P4.3/S38	50	I/O	General-purpose digital I/O / LCD segment output 38
			P4.2/S39	51	I/O	General-purpose digital I/O / LCD segment output 39
COM0	44	O	COM0	52	O	COM0−3 are used for LCD backplanes.
P5.2/COM1	45	I/O	P5.2/COM1	53	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
P5.3/COM2	46	I/O	P5.3/COM2	54	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
P5.4/COM3	47	I/O	P5.4/COM3	55	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
R03	48	I	R03	56	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	49	I/O	P5.5/R13	57	I/O	General-purpose digital I/O / input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	50	I/O	P5.6/R23	58	I/O	General-purpose digital I/O / input port of second most positive analog LCD level (V2)
P5.7/R33	51	I/O	P5.7/R33	59	I/O	General-purpose digital I/O / output port of most positive analog LCD level (V1)
DV_{CC2}	52		DV_{CC2}	60		Digital supply voltage, positive terminal.
DV_{SS2}	53		DV_{SS2}	61		Digital supply voltage, negative terminal.
			P4.1	62	I/O	General-purpose digital I/O
			P4.0	63	I/O	General-purpose digital I/O
			P3.7	64	I/O	General-purpose digital I/O
			P3.6	65	I/O	General-purpose digital I/O
			P3.5	66	I/O	General-purpose digital I/O
			P3.4	67	I/O	General-purpose digital I/O
			P3.3/UCLK0	68	I/O	General-purpose digital I/O / external clock input—USART0/UART or SPI mode, clock output—USART0/SPI mode
			P3.2/SOMI0	69	I/O	General-purpose digital I/O / slave out/master in of USART0/SPI mode
			P3.1/SIMO0	70	I/O	General-purpose digital I/O / slave in/master out of USART0/SPI mode
			P3.0/STE0	71	I/O	General-purpose digital I/O / slave transmit enable USART0/SPI mode
			P2.7/ADC12CLK	72	I/O	General-purpose digital I/O / conversion clock—12-bit ADC
			P2.6/CAOUT	73	I/O	General-purpose digital I/O / Comparator_A output
P2.5/URXD0	54	I/O	P2.5/URXD0	74	I/O	General-purpose digital I/O / receive data in—USART0/UART mode

MSP430x43x Terminal Functions (Continued)

TERMINAL						DESCRIPTION
PN		I/O	PZ		I/O	
NAME	NO.		NAME	NO.		
P2.4/UTXD0	55	I/O	P2.4/UTXD0	75	I/O	General-purpose digital I/O / transmit data out—USART0/UART mode
P2.3/TB2	56	I/O	P2.3/TB2	76	I/O	General-purpose digital I/O / Timer_B3 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output
P2.2/TB1	57	I/O	P2.2/TB1	77	I/O	General-purpose digital I/O / Timer_B3 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output
P2.1/TB0	58	I/O	P2.1/TB0	78	I/O	General-purpose digital I/O / Timer_B3 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output
P2.0/TA2	59	I/O	P2.0/TA2	79	I/O	General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output
P1.7/CA1	60	I/O	P1.7/CA1	80	I/O	General-purpose digital I/O / Comparator_A input
P1.6/CA0	61	I/O	P1.6/CA0	81	I/O	General-purpose digital I/O / Comparator_A input
P1.5/TACLK/ ACLK	62	I/O	P1.5/TACLK/ ACLK	82	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8)
P1.4/TBCLK/ SMCLK	63	I/O	P1.4/TBCLK/ SMCLK	83	I/O	General-purpose digital I/O / input clock TBCLK—Timer_B3 / submain system clock SMCLK output
P1.3/TBOUTH/ SVSOUT	64	I/O	P1.3/TBOUTH/ SVSOUT	84	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B3 TB0 to TB2 / SVS: output of SVS comparator
P1.2/TA1	65	I/O	P1.2/TA1	85	I/O	General-purpose digital I/O / Timer_A, Capture: CCI1A input, compare: Out1 output
P1.1/TA0/MCLK	66	I/O	P1.1/TA0/MCLK	86	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0B input / MCLK output. Note: TA0 is only an input on this pin / BSL receive
P1.0/TA0	67	I/O	P1.0/TA0	87	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit
XT2OUT	68	O	XT2OUT	88	O	Output terminal of crystal oscillator XT2
XT2IN	69	I	XT2IN	89	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
TDO/TDI	70	I/O	TDO/TDI	90	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TDI/TCLK	71	I	TDI/TCLK	91	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TMS	72	I	TMS	92	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	73	I	TCK	93	I	Test clock. TCK is the clock input port for device programming and test.
$\overline{\text{RST}}$/NMI	74	I	$\overline{\text{RST}}$/NMI	94	I	General-purpose digital I/O / reset input or nonmaskable interrupt input port
P6.0/A0	75	I/O	P6.0/A0	95	I/O	General-purpose digital I/O / analog input a0 − 12-bit ADC
P6.1/A1	76	I/O	P6.1/A1	96	I/O	General-purpose digital I/O / analog input a1 − 12-bit ADC
P6.2/A2	77	I/O	P6.2/A2	97	I/O	General-purpose digital I/O / analog input a2 − 12-bit ADC
AV_{SS}	78		AV_{SS}	98		Analog supply voltage, negative terminal. Supplies SVS, brownout, oscillator, FLL+, comparator_A, ADC12, port 1, and LCD resistive divider circuitry.
DV_{SS1}	79		DV_{SS1}	99		Digital supply voltage, negative terminal.
AV_{CC}	80		AV_{CC}	100		Analog supply voltage, positive terminal. Supplies SVS, brownout, oscillator, FLL+, comparator_A, ADC12, port 1, and LCD resistive divider circuitry; must not power up prior to DV_{CC1}/DV_{CC2}.

MSP430x44x Terminal Functions

TERMINAL PN NAME	NO.	I/O	DESCRIPTION
DV_{CC1}	1		Digital supply voltage, positive terminal.
P6.3/A3	2	I/O	General-purpose digital I/O / analog input a3—12-bit ADC
P6.4/A4	3	I/O	General-purpose digital I/O / analog input a4—12-bit ADC
P6.5/A5	4	I/O	General-purpose digital I/O / analog input a5—12-bit ADC
P6.6/A6	5	I/O	General-purpose digital I/O / analog input a6—12-bit ADC
P6.7/A7/SVSIN	6	I/O	General-purpose digital I/O / analog input a7—12-bit ADC / analog input to brownout, supply voltage supervisor
V_{REF+}	7	O	Output of positive terminal of the reference voltage in the ADC
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
Ve_{REF+}	10	I	Input for an external reference voltage to the ADC
V_{REF-}/Ve_{REF-}	11	I	Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
P5.1/S0	12	I/O	General-purpose digital I/O / LCD segment output 0
P5.0/S1	13	I/O	General-purpose digital I/O / LCD segment output 1
S2	14	O	LCD segment output 2
S3	15	O	LCD segment output 3
S4	16	O	LCD segment output 4
S5	17	O	LCD segment output 5
S6	18	O	LCD segment output 6
S7	19	O	LCD segment output 7
S8	20	O	LCD segment output 8
S9	21	O	LCD segment output 9
S10	22	O	LCD segment output 10
S11	23	O	LCD segment output 11
S12	24	O	LCD segment output 12
S13	25	O	LCD segment output 13
S14	26	O	LCD segment output 14
S15	27	O	LCD segment output 15
S16	28	O	LCD segment output 16
S17	29	O	LCD segment output 17
S18	30	O	LCD segment output 18
S19	31	O	LCD segment output 19
S20	32	O	LCD segment output 20
S21	33	O	LCD segment output 21
S22	34	O	LCD segment output 22
S23	35	O	LCD segment output 23
S24	36	O	LCD segment output 24
S25	37	O	LCD segment output 25
S26	38	O	LCD segment output 26
S27	39	O	LCD segment output 27
S28	40	O	LCD segment output 28

MSP430x44x Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
PN NAME	NO.		
S29	41	O	LCD segment output 29
S30	42	O	LCD segment output 30
S31	43	O	LCD segment output 31
S32	44	O	LCD segment output 32
S33	45	O	LCD segment output 33
P4.7/S34	46	I/O	General-purpose digital I/O / LCD segment output 34
P4.6/S35	47	I/O	General-purpose digital I/O / LCD segment output 35
P4.5/UCLK1/S36	48	I/O	General-purpose digital I/O / external clock input—USART1/UART or SPI mode, clock output—USART1/SPI MODE / LCD segment output 36
P4.4/SOMI1/S37	49	I/O	General-purpose digital I/O / slave out/master in of USART1/SPI mode / LCD segment output 37
P4.3/SIMO1/S38	50	I/O	General-purpose digital I/O / slave in/master out of USART1/SPI mode / LCD segment output 38
P4.2/STE1/S39	51	I/O	General-purpose digital I/O / slave transmit enable—USART1/SPI mode / LCD segment output 39
COM0	52	O	COM0−3 are used for LCD backplanes.
P5.2/COM1	53	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
P5.3/COM2	54	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
P5.4/COM3	55	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
R03	56	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	57	I/O	General-purpose digital I/O / Input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	58	I/O	General-purpose digital I/O / Input port of second most positive analog LCD level (V2)
P5.7/R33	59	I/O	General-purpose digital I/O / Output port of most positive analog LCD level (V1)
DV_{CC2}	60		Digital supply voltage, positive terminal.
DV_{SS2}	61		Digital supply voltage, negative terminal.
P4.1/URXD1	62	I/O	General-purpose digital I/O / receive data in—USART1/UART mode
P4.0/UTXD1	63	I/O	General-purpose digital I/O / transmit data out—USART1/UART mode
P3.7/TB6	64	I/O	General-purpose digital I/O / Timer_B7 CCR6 / Capture: CCI6A/CCI6B input, compare: Out6 output
P3.6/TB5	65	I/O	General-purpose digital I/O / Timer_B7 CCR5 / Capture: CCI5A/CCI5B input, compare: Out5 output
P3.5/TB4	66	I/O	General-purpose digital I/O / Timer_B7 CCR4 / Capture: CCI4A/CCI4B input, compare: Out4 output
P3.4/TB3	67	I/O	General-purpose digital I/O / Timer_B7 CCR3 / Capture: CCI3A/CCI3B input, compare: Out3 output
P3.3/UCLK0	68	I/O	General-purpose digital I/O / external clock input—USART0/UART or SPI mode, clock output—USART0/SPI mode
P3.2/SOMI0	69	I/O	General-purpose digital I/O / slave out/master in of USART0/SPI mode
P3.1/SIMO0	70	I/O	General-purpose digital I/O / slave in/master out of USART0/SPI mode
P3.0/STE0	71	I/O	General-purpose digital I/O / slave transmit enable—USART0/SPI mode
P2.7/ADC12CLK	72	I/O	General-purpose digital I/O / conversion clock—12-bit ADC
P2.6/CAOUT	73	I/O	General-purpose digital I/O / Comparator_A output
P2.5/URXD0	74	I/O	General-purpose digital I/O / receive data in—USART0/UART mode
P2.4/UTXD0	75	I/O	General-purpose digital I/O / transmit data out—USART0/UART mode
P2.3/TB2	76	I/O	General-purpose digital I/O / Timer_B7 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output
P2.2/TB1	77	I/O	General-purpose digital I/O / Timer_B7 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output
P2.1/TB0	78	I/O	General-purpose digital I/O / Timer_B7 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output
P2.0/TA2	79	I/O	General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output
P1.7/CA1	80	I/O	General-purpose digital I/O / Comparator_A input

MSP430x44x Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
PN			
NAME	NO.		
P1.6/CA0	81	I/O	General-purpose digital I/O / Comparator_A input
P1.5/TACLK/ ACLK	82	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8)
P1.4/TBCLK/ SMCLK	83	I/O	General-purpose digital I/O / input clock TBCLK—Timer_B7 / submain system clock SMCLK output
P1.3/TBOUTH/ SVSOUT	84	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B7 TB0 to TB6 / SVS: output of SVS comparator
P1.2/TA1	85	I/O	General-purpose digital I/O / Timer_A, Capture: CCI1A input, compare: Out1 output
P1.1/TA0/MCLK	86	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0B input / MCLK output. Note: TA0 is only an input on this pin / BSL receive
P1.0/TA0	87	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit
XT2OUT	88	O	Output terminal of crystal oscillator XT2
XT2IN	89	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
TDO/TDI	90	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TDI/TCLK	91	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TMS	92	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	93	I	Test clock. TCK is the clock input port for device programming and test.
$\overline{\text{RST}}$/NMI	94	I	Reset input or nonmaskable interrupt input port
P6.0/A0	95	I/O	General-purpose digital I/O, analog input a0—12-bit ADC
P6.1/A1	96	I/O	General-purpose digital I/O, analog input a1—12-bit ADC
P6.2/A2	97	I/O	General-purpose digital I/O, analog input a2—12-bit ADC
AV_{SS}	98		Analog supply voltage, negative terminal. Supplies SVS, brownout, oscillator, FLL+, comparator_A, ADC12, port 1, and LCD resistive divider circuitry.
DV_{SS1}	99		Digital supply voltage, negative terminal.
AV_{CC}	100		Analog supply voltage, positive terminal. Supplies SVS, brownout, oscillator, FLL+, comparator_A, ADC12, port 1, and LCD resistive divider circuitry; must not power up prior to DV_{CC1}/DV_{CC2}.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 −−−> R5
Single operands, destination only	e.g. CALL R8	PC −−>(TOS), R8−−> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 −−> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)−−> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) −−> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) −−> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) −−> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) −−> R11 R10 + 2−−> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 −−> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    FLL+ Loop control remains active
- Low-power mode 1 (LPM1);
  - CPU is disabled
    FLL+ Loop control is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 2 (LPM2);
  - CPU is disabled
    MCLK and FLL+ loop control and DCOCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled
    ACLK is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh − 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 3. Interrupt Sources, Flags, and Vectors of 4xx Configurations

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer_B7†	TBCCR0 CCIFG (see Note 2)	Maskable	0FFFAh	13
Timer_B7†	TBCCR1 to TBCCR6 CCIFGs TBIFG (see Notes 1 and 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog Timer	WDTIFG	Maskable	0FFF4h	10
USART0 Receive	URXIFG0	Maskable	0FFF2h	9
USART0 Transmit	UTXIFG0	Maskable	0FFF0h	8
ADC12	ADC12IFG (see Notes 1 and 2)	Maskable	0FFEEh	7
Timer_A3	TACCR0 CCIFG (see Note 2)	Maskable	0FFECh	6
Timer_A3	TACCR1 and TACCR2 CCIFGs, TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	5
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	4
USART1 Receive‡	URXIFG1	Maskable	0FFE6h	3
USART1 Transmit‡	UTXIFG1	Maskable	0FFE4h	2
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

† ’43x uses Timer_B3 with TBCCR0, 1 and 2 CCIFG flags, and TBIFG. ’44x uses Timer_B7 with TBCCR0 CCIFG, TBCCR1 to TBCCR6 CCIFGs, and TBIFG

‡ USART1 is implemented in ’44x only.

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable can not disable it.

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h	UTXIE0	URXIE0	ACCVIE	NMIIE			OFIE	WDTIE
	rw–0	rw–0	rw–0	rw–0			rw–0	rw–0

WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash access violation interrupt enable

URXIE0: USART0: UART and SPI receive-interrupt enable

UTXIE0: USART0: UART and SPI transmit-interrupt enable

Address	7	6	5	4	3	2	1	0
01h	BTIE		UTXIE1	URXIE1				
	rw–0		rw–0	rw–0				

URXIE1: USART1: UART and SPI receive-interrupt enable (MSP430F44x devices only)

UTXIE1: USART1: UART and SPI transmit-interrupt enable (MSP430F44x devices only)

BTIE: Basic timer interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h	UTXIFG0	URXIFG0		NMIIFG			OFIFG	WDTIFG
	rw–1	rw–0		rw–0			rw–1	rw–(0)

WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power up or a reset condition at the $\overline{RST}$/NMI pin in reset mode.

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{RST}$/NMI pin

URXIFG0: USART0: UART and SPI receive flag

UTXIFG0: USART0: UART and SPI transmit flag

Address	7	6	5	4	3	2	1	0
03h	BTIFG		UTXIFG1	URXIFG1				
	rw		rw–1	rw–0				

URXIFG1: USART1: UART and SPI receive flag (MSP430F44x devices only)

UTXIFG1: USART1: UART and SPI transmit flag (MSP430F44x devices only)

BTIFG: Basic timer flag

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h	UTXE0	URXE0 USPIE0						
	rw–0	rw–0						

URXE0: USART0: UART mode receive enable

UTXE0: USART0: UART mode transmit enable

USPIE0: USART0: SPI mode transmit and receive enable

Address	7	6	5	4	3	2	1	0
05h			UTXE1	URXE1 USPIE1				
			rw–0	rw–0				

URXE1: USART1: UART mode receive enable (MSP430F44x devices only)

UTXE1: USART1: UART mode transmit enable (MSP430F44x devices only)

USPIE1: USART1: SPI mode transmit and receive enable (MSP430F44x devices only)

Legend: rw:	**Bit Can Be Read and Written**
rw–0,1:	**Bit Can Be Read and Written. It Is Reset or Set by PUC.**
rw–(0,1):	**Bit Can Be Read and Written. It Is Reset or Set by POR.**
	SFR Bit Not Present in Device

memory organization

		MSP430F435	MSP430F436	MSP430F437 MSP430F447	MSP430F448	MSP430F449
Memory Main: interrupt vector Main: code memory	Size Flash Flash	16KB 0FFFFh − 0FFE0h 0FFFFh − 0C000h	24KB 0FFFFh − 0FFE0h 0FFFFh − 0A000h	32KB 0FFFFh − 0FFE0h 0FFFFh − 08000h	48KB 0FFFFh − 0FFE0h 0FFFFh − 04000h	60KB 0FFFFh − 0FFE0h 0FFFFh − 01100h
Information memory	Size Flash	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h
Boot memory	Size ROM	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h
RAM	Size	512 Byte 03FFh − 0200h	1KB 05FFh − 0200h	1KB 05FFh − 0200h	2KB 09FFh − 0200h	2KB 09FFh − 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h

bootstrap loader (BSL)

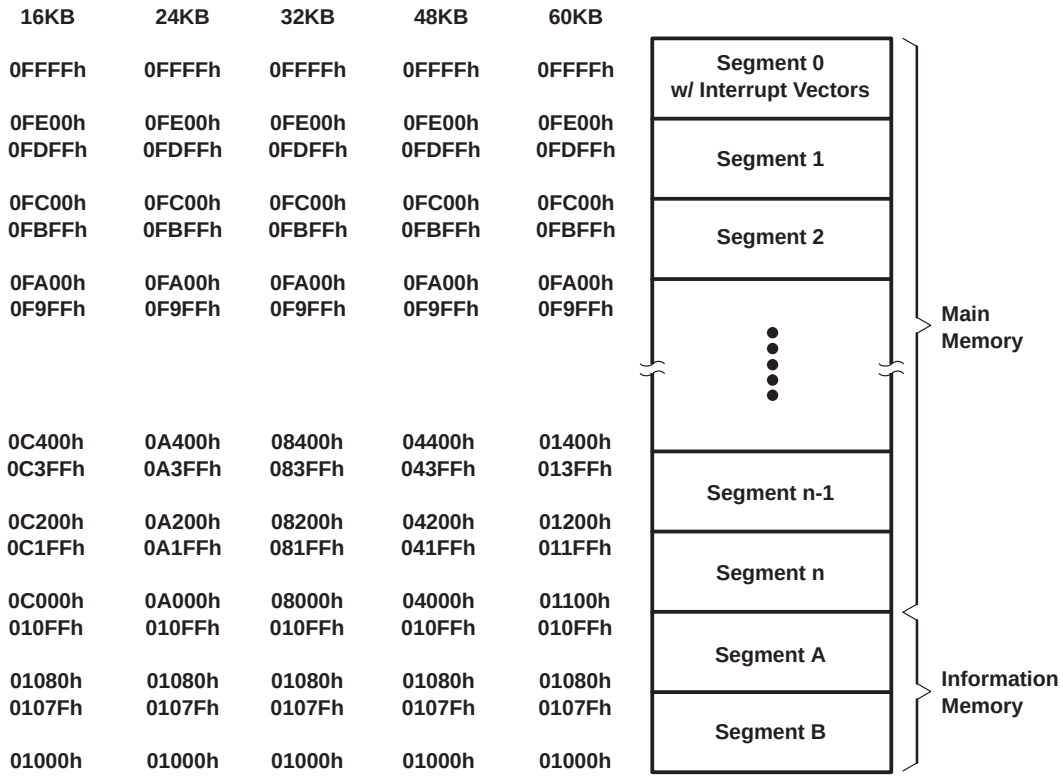
The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

BSL Function	PN Package Pins	PZ Package Pins
Data Transmit	67 - P1.0	87 - P1.0
Data Receive	66 - P1.1	86 - P1.1

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0−n.
  Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User's Guide*, literature number SLAU056.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

oscillator and system clock

The clock system in the MSP430x43x and MSP43x44x family of devices is supported by the FLL+ module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low-power consumption. The FLL+ features a digital frequency locked loop (FLL) hardware which in conjunction with a digital modulator stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8.

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

hardware multiplier (MSP430x44x Only)

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16, 16×8, 8×16, and 8×8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

USART0

The MSP430x43x and the MSP430x44x have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

USART1 (MSP430x44x Only)

The MSP430x44x has a second hardware universal synchronous/asynchronous receive transmit (USART1) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels. Operation of USART1 is identical to USART0.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections

Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
PN	PZ					PN	PZ
62 - P1.5	82 - P1.5	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
62 - P1.5	82 - P1.5	$\overline{\text{TACLK}}$	INCLK				
67 - P1.0	87 - P1.0	TA0	CCI0A	CCR0	TA0	67 - P1.0	87 - P1.0
66 - P1.1	86 - P1.1	TA0	CCI0B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
65 - P1.2	85 - P1.2	TA1	CCI1A	CCR1	TA1	14 - P1.2	85 - P1.2
		CAOUT (internal)	CCI1B			ADC12 (internal)	
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
59 - P2.0	79 - P2.0	TA2	CCI2A	CCR2	TA2	15 - P1.3	79 - P2.0
		ACLK (internal)	CCI2B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

timer_B3 (MSP430x43x Only)

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

timer_B7 (MSP430x44x Only)

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_B3/B7 Signal Connections†							
Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
PN	PZ					PN	PZ
63 - P1.4	83 - P1.4	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
63 - P1.4	83 - P1.4	$\overline{\text{TBCLK}}$	INCLK				
58 - P2.1	78 - P2.1	TB0	CCI0A	CCR0	TB0	58 - P2.1	78 - P2.1
58 - P2.1	78 - P2.1	TB0	CCI0B			ADC12 (internal)	
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
57 - P2.2	77 - P2.2	TB1	CCI1A	CCR1	TB1	57 - P2.2	77 - P2.2
57 - P2.2	77 - P2.2	TB1	CCI1B			ADC12 (internal)	
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
56 - P2.3	76 - P2.3	TB2	CCI2A	CCR2	TB2	56 - P2.3	76 - P2.3
56 - P2.3	76 - P2.3	TB2	CCI2B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
	67 - P3.4	TB3	CCI3A	CCR3	TB3		67 - P3.4
	67 - P3.4	TB3	CCI3B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
	66 - P3.5	TB4	CCI4A	CCR4	TB4		66 - P3.5
	66 - P3.5	TB4	CCI4B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
	65 - P3.6	TB5	CCI5A	CCR5	TB5		65 - P3.6
	65 - P3.6	TB5	CCI5B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
	64 - P3.7	TB6	CCI6A	CCR6	TB6		64 - P3.7
		ACLK (internal)	CCI6B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

† Timer_B3 implements three capture/compare blocks (CCR0, CCR1 and CCR2 only).

comparator_A

The primary function of the comparator_A module is to support precision slope analog−to−digital conversions, battery−voltage supervision, and monitoring of external analog signals.

ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

Basic Timer1

The Basic Timer1 has two independent 8-bit timers which can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 can be used to generate periodic interrupts and clock for the LCD module.

LCD drive

The LCD driver generates the segment and common signals required to drive an LCD display. The LCD controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_B7/ Timer_B3 (see Note 1)	Capture/compare register 6	TBCCR6	019Eh
	Capture/compare register 5	TBCCR5	019Ch
	Capture/compare register 4	TBCCR4	019Ah
	Capture/compare register 3	TBCCR3	0198h
	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 6	TBCCTL6	018Eh
	Capture/compare control 5	TBCCTL5	018Ch
	Capture/compare control 4	TBCCTL4	018Ah
	Capture/compare control 3	TBCCTL3	0188h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Reserved		017Eh
	Reserved		017Ch
	Reserved		017Ah
	Reserved		0178h
	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Reserved		016Eh
	Reserved		016Ch
	Reserved		016Ah
	Reserved		0168h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Hardware Multiplier (MSP430x44x only)	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Second operand	OP2	0138h
	Multiply signed + accumulate/operand1	MACS	0136h
	Multiply + accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h

NOTE 1: Timer_B7 in the MSP430x44x family has seven CCRs; Timer_B3 in the MSP430x43x family has three CCRs.

peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
ADC12	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
	ADC memory-control register15	ADC12MCTL15	08Fh
	ADC memory-control register14	ADC12MCTL14	08Eh
	ADC memory-control register13	ADC12MCTL13	08Dh
	ADC memory-control register12	ADC12MCTL12	08Ch
	ADC memory-control register11	ADC12MCTL11	08Bh
	ADC memory-control register10	ADC12MCTL10	08Ah
	ADC memory-control register9	ADC12MCTL9	089h
	ADC memory-control register8	ADC12MCTL8	088h
	ADC memory-control register7	ADC12MCTL7	087h
	ADC memory-control register6	ADC12MCTL6	086h
	ADC memory-control register5	ADC12MCTL5	085h
	ADC memory-control register4	ADC12MCTL4	084h
	ADC memory-control register3	ADC12MCTL3	083h
	ADC memory-control register2	ADC12MCTL2	082h
	ADC memory-control register1	ADC12MCTL1	081h
	ADC memory-control register0	ADC12MCTL0	080h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
LCD	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDCTL	090h
USART1 (Only in ‘x44x)	Transmit buffer	U1TXBUF	07Fh
	Receive buffer	U1RXBUF	07Eh
	Baud rate	U1BR1	07Dh
	Baud rate	U1BR0	07Ch
	Modulation control	U1MCTL	07Bh
	Receive control	U1RCTL	07Ah
	Transmit control	U1TCTL	079h
	USART control	U1CTL	078h
USART0	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate	U0BR1	075h
	Baud rate	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
BrownOUT, SVS	SVS control register (Reset by brownout signal)	SVSCTL	056h
FLL+ Clock	FLL+ Control1	FLL_CTL1	054h
	FLL+ Control0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter2	BTCNT2	047h
	BT counter1	BTCNT1	046h
	BT control	BTCTL	040h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special functions	SFR module enable2	ME2	005h
	SFR module enable1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} . . . . . −0.3 V to 4.1 V
Voltage applied to any pin (see Note) . . . . . −0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg}: (unprogrammed device) . . . . . −55°C to 150°C
(programmed device) . . . . . −40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

recommended operating conditions

			MIN	NOM	MAX	UNITS
Supply voltage during program execution V_{CC} (AV_{CC} = DV_{CC1} = DV_{CC2} = V_{CC})		MSP430F43x, MSP430F44x	1.8		3.6	V
Supply voltage during flash memory programming V_{CC} (AV_{CC} = DV_{CC1} = DV_{CC2} = V_{CC})		MSP430F43x, MSP430F44x	2.7		3.6	V
Supply voltage during program execution, SVS enabled (see Note 1) V_{CC} (AV_{CC} = DV_{CC1} = DV_{CC2} = V_{CC})		MSP430F43x, MSP430F44x	2		3.6	V
Supply voltage, V_{SS} (AV_{SS} = DV_{SS1} = DV_{SS2} = V_{SS})			0		0	V
Operating free-air temperature range, T_A		MSP430x43x, MSP430x44x	−40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2)	LF selected, XTS_FLL=0	Watch crystal		32.768		kHz
	XT1 selected, XTS_FLL=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS_FLL=1	Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	

NOTES: 1. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the supply voltage is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

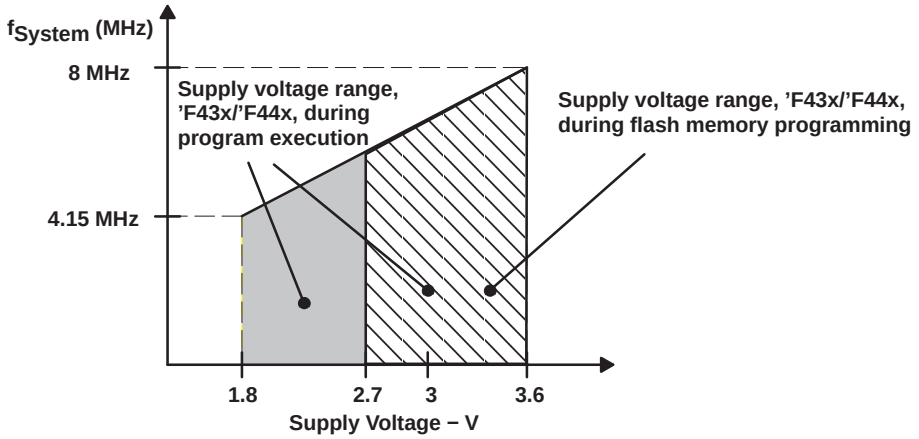


Figure 1. Frequency vs Supply Voltage, MSP430F43x or MSP430F44x

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS_FLL=0, SELM=(0,1)	T_A = −40°C to 85°C	V_{CC} = 2.2 V		280	350	µA
			V_{CC} = 3 V		420	560	
$I_{(LPM0)}$	Low-power mode, (LPM0) (see Note 1)	T_A = −40°C to 85°C	V_{CC} = 2.2 V		32	45	µA
			V_{CC} = 3 V		55	70	
$I_{(LPM2)}$	Low-power mode, (LPM2), f(MCLK) = f (SMCLK) = 0 MHz, f(ACLK) = 32,768 Hz, SCG0 = 0 (see Note 2)	T_A = −40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 (see Note 3)	T_A = −40°C	V_{CC} = 2.2 V		1	1.5	µA
		T_A = 25°C			1.1	1.5	
		T_A = 60°C			2	3	
		T_A = 85°C			3.5	6	
		T_A = −40°C	V_{CC} = 3 V		1.8	2.2	µA
		T_A = 25°C			1.6	1.9	
		T_A = 60°C			2.5	3.5	
		T_A = 85°C			4.2	7.5	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (see Note 2)	T_A = −40°C	V_{CC} = 2.2 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 60°C			0.7	1.1	
		T_A = 85°C			1.7	3	
		T_A = −40°C	V_{CC} = 3 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 60°C			0.8	1.2	
		T_A = 85°C			1.9	3.5	

NOTES: 1. Timer_B is clocked by $f_{(DCOCLK)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
3. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumption in LPM3 is measured with active Basic Timer1 and LCD (ACLK selected). The current consumption of the Comparator_A and the SVS module are specified in the respective sections. The LPM3 currents are characterized with a KDS Daishinku DT−38 (6 pF) crystal and OSCCAPx=1h.

Current consumption of active mode versus system frequency, F-version:

$$I_{(AM)} = I_{(AM)\ [1\ MHz]} \times f_{(System)}\ [MHz]$$

Current consumption of active mode versus supply voltage, F-version:

$$I_{(AM)} = I_{(AM)\ [3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SCHMITT-trigger inputs − ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis (V_{IT+} − V_{IT-})	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

standard inputs − $\overline{\text{RST}}$/NMI; JTAG: TCK, TMS, TDI/TCLK

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 2.2 V / 3 V	V_{SS}		V_{SS}+0.6	V
V_{IH}	High-level input voltage		0.8×V_{CC}		V_{CC}	V

inputs Px.x, TAx, TBx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, Timer_B capture timing	TA0, TA1, TA2	2.2 V	62			ns
		TB0, TB1, TB2, TB3, TB4, TB5, TB6 (see Note 2)	3 V	50			
$f_{(TAext)}$	Timer_A, Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
$f_{(TBext)}$			3 V			10	
$f_{(TAint)}$	Timer_A, Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
$f_{(TBint)}$			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ cycle and time parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.
2. Seven capture/compare registers in ’x44x and three capture/compare registers in ’x43x.

leakage current (see Notes 1 and 2)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current	Port P1	Port 1: $V_{(P1.x)}$	V_{CC} = 2.2 V/3 V			±50	nA
$I_{lkg(P6.x)}$		Port P6	Port 6: $V_{(P6.x)}$				±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input and there must be no optional pullup or pulldown resistor.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs − ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = −1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}−0.25		V_{CC}	V
		$I_{OH(max)}$ = −6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}−0.6		V_{CC}	
		$I_{OH(max)}$ = −1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}−0.25		V_{CC}	
		$I_{OH(max)}$ = −6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}−0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	(1 ≤ x ≤ 6, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ±1.5 mA	V_{CC} = 2.2 V	DC		5	MHz
			V_{CC} = 3 V	DC		7.5	
$f_{(ACLK)}$ $f_{(MCLK)}$ $f_{(SMCLK)}$	P1.1/TA0/MCLK, P1.5/TACLK/ ACLK P1.4/TBCLK/SMCLK	C_L = 20 pF				$f_{(System)}$	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.5/TACLK/ACLK, C_L = 20 pF V_{CC} = 2.2 V / 3 V	$f_{(ACLK)} = f_{(LFXT1)} = f_{(XT1)}$	40%		60%	
			$f_{(ACLK)} = f_{(LFXT1)} = f_{(LF)}$	30%		70%	
			$f_{(ACLK)} = f_{(LFXT1)}$		50%		
		P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50%− 15 ns	50%	50%+ 15 ns	
		P1.4/TBCLK/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(SMCLK)} = f_{(XT2)}$	40%		60%	
			$f_{(SMCLK)} = f_{(DCOCLK)}$	50%− 15 ns	50%	50%+ 15 ns	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs − Ports P1, P2, P3, P4, P5, and P6 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

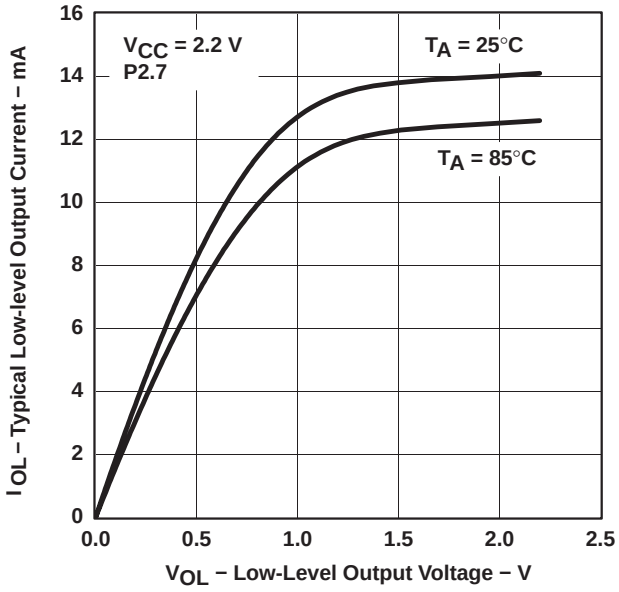


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

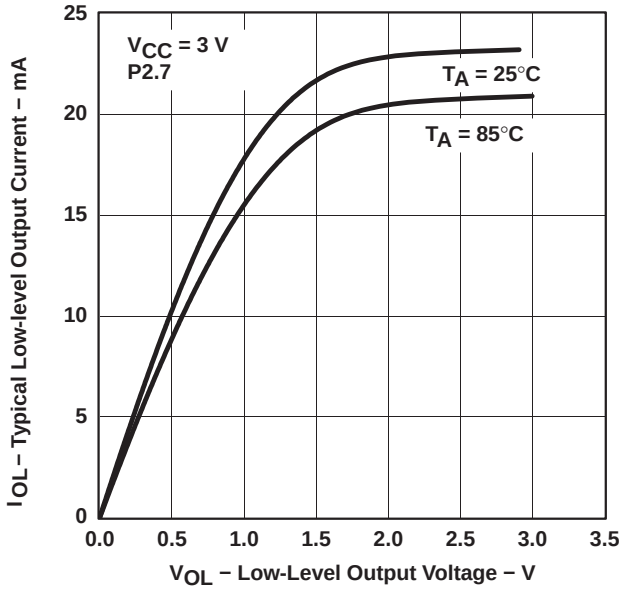


Figure 3

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

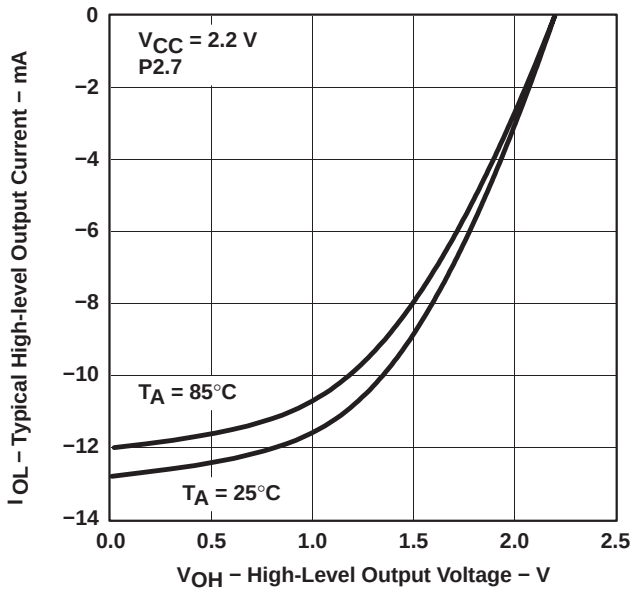


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

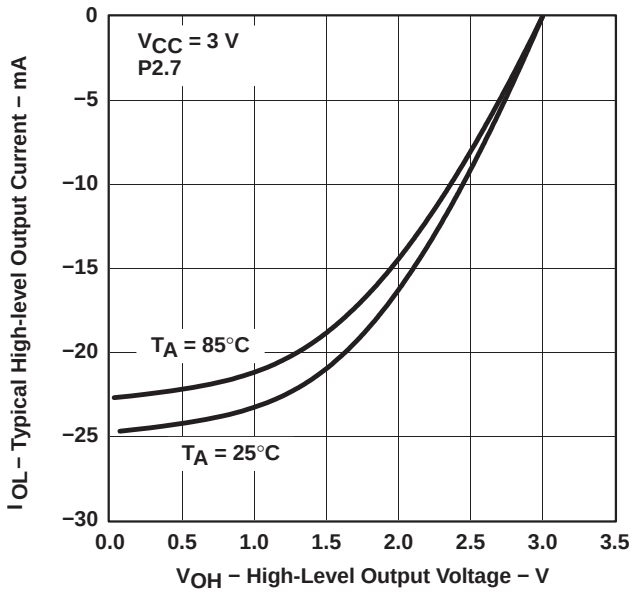


Figure 5

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(33)}$	Analog voltage	Voltage at P5.7/R33	V_{CC} = 3 V	2.5		V_{CC} + 0.2	V
$V_{(23)}$		Voltage at P5.6/R23			$[V_{(33)}-V_{(03)}] \times 2/3 + V_{(03)}$		
$V_{(13)}$		Voltage at P5.5/R13			$[V_{(33)}-V_{(03)}] \times 1/3 + V_{(03)}$		
$V_{(33)} - V_{(03)}$		Voltage at R33 to R03		2.5		V_{CC} + 0.2	
$I_{(R03)}$	Input leakage	R03 = V_{SS}	No load at all segment and common lines, V_{CC} = 3 V			±20	nA
$I_{(R13)}$		P5.5/R13 = $V_{CC}/3$				±20	
$I_{(R23)}$		P5.6/R23 = $2 \times V_{CC}/3$				±20	
$V_{(Sxx0)}$	Segment line voltage	$I_{(Sxx)}$ = −3 µA,	V_{CC} = 3 V	$V_{(03)}$		$V_{(03)}$ − 0.1	V
$V_{(Sxx1)}$				$V_{(13)}$		$V_{(13)}$ − 0.1	
$V_{(Sxx2)}$				$V_{(23)}$		$V_{(23)}$ − 0.1	
$V_{(Sxx3)}$				$V_{(33)}$		$V_{(33)}$ + 0.1	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V / 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2V / 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 6 and Figure 7	PCA0=1, CARSEL=1, CAREF=3, No load at P1.6/CA0 and P1.7/CA1; T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
V_{IC}	Common-mode input voltage range	CAON=1	V_{CC} = 2.2 V / 3 V	0		V_{CC}−1	V
V_p−V_S	Offset voltage	See Note 2	VCC = 2.2 V / 3 V	−30		30	mV
V_{hys}	Input hysteresis	CAON = 1	V_{CC} = 2.2 V / 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	160	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics

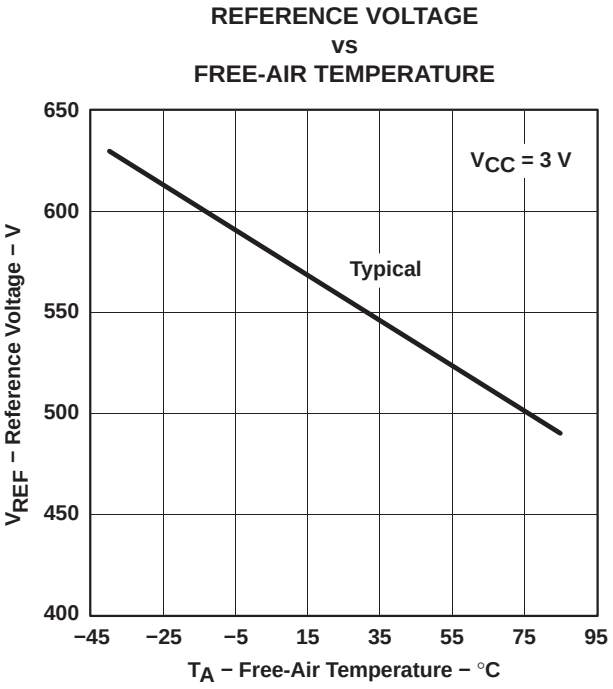


Figure 6. $V_{(RefVT)}$ vs Temperature

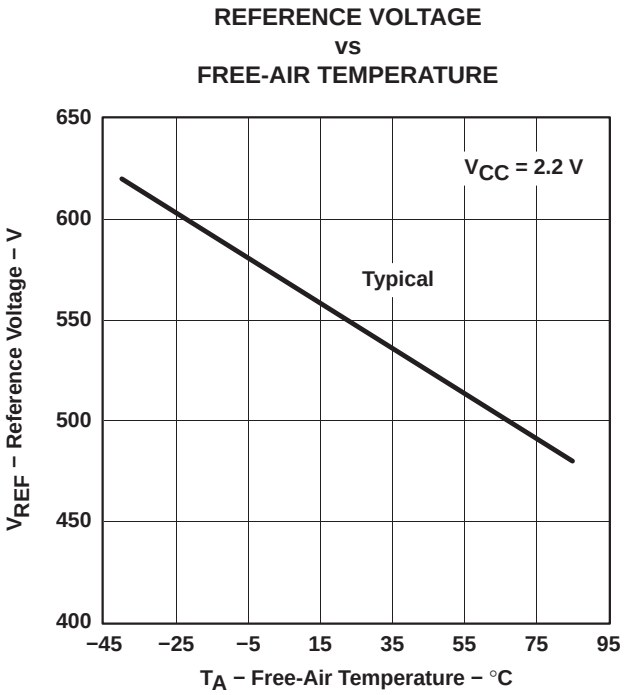


Figure 7. $V_{(RefVT)}$ vs Temperature

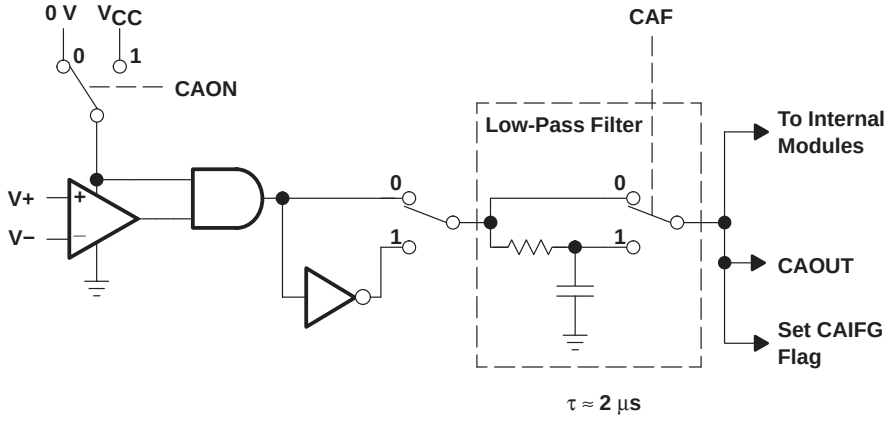


Figure 8. Block Diagram of Comparator_A Module

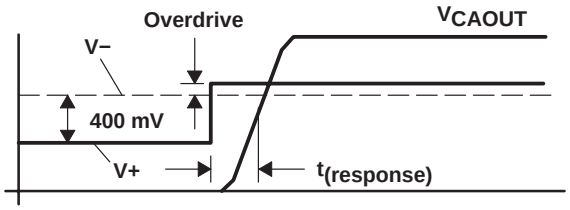


Figure 9. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout (see Note 2)				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10 through Figure 12)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)	70	130	180	mV
$t_{(reset)}$		Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide (SLAU056)* for more information on the brownout/SVS circuit.

typical characteristics

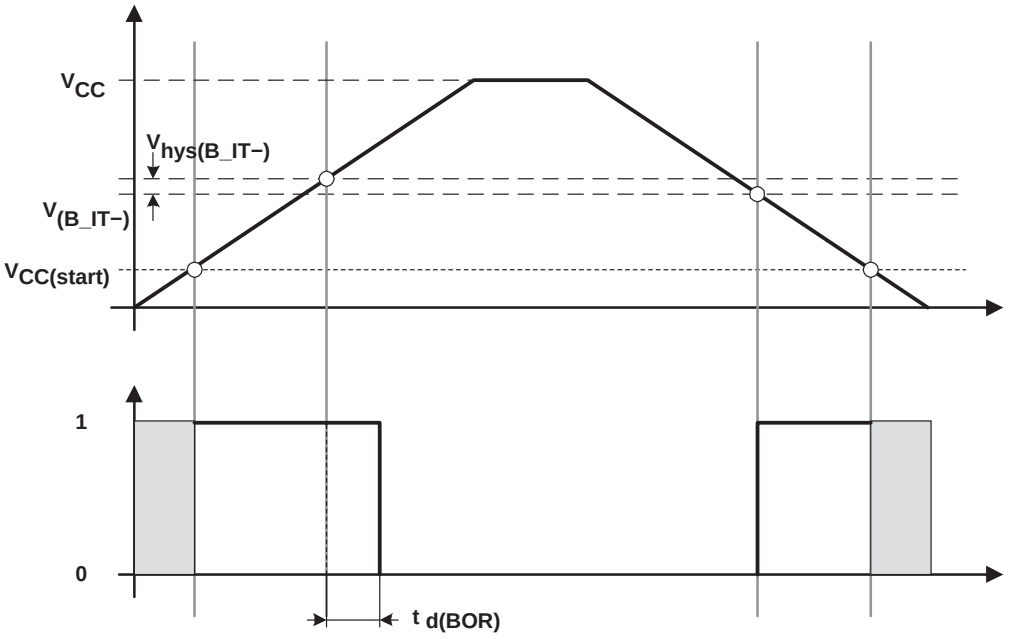


Figure 10. POR/Brownout Reset (BOR) vs Supply Voltage

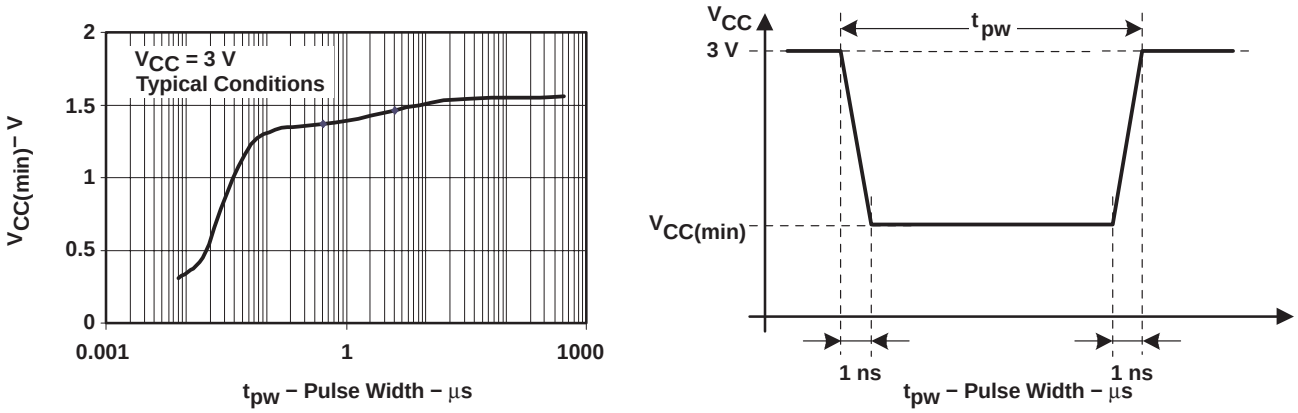


Figure 11. $V_{CC(min)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

typical characteristics (Continued)

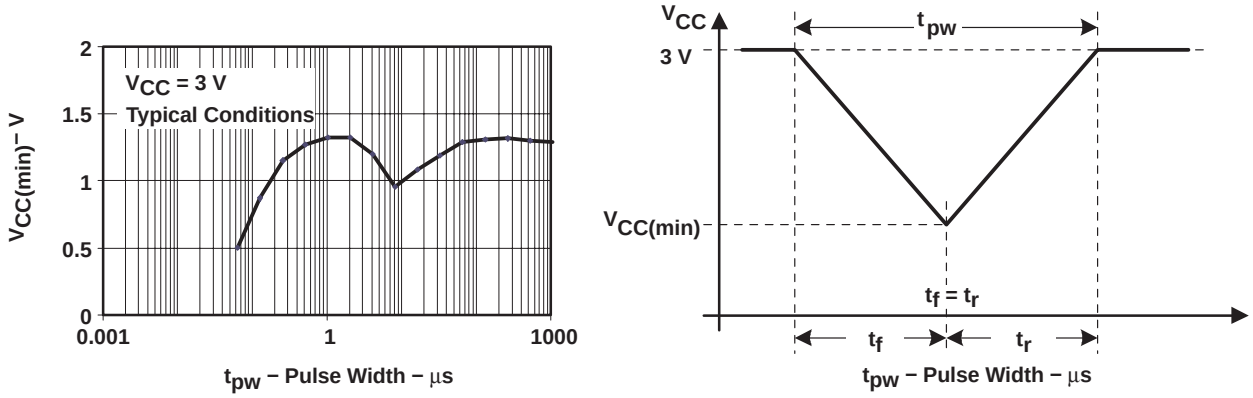


Figure 12. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SVS (supply voltage supervisor/monitor)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 13)		5		150	µs
	$dV_{CC}/dt \le 30$ V/ms				2000	µs
$t_{d(SVSon)}$	SVSon, switch from VLD=0 to VLD ≠ 0, V_{CC} = 3 V		20		150	µs
t_{settle}	VLD ≠ 0‡				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \le 3$ V/s (see Figure 13)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 13)	VLD = 1	70	120	155	mV
		VLD = 2 .. 14	$V_{(SVS\_IT-)}$ x 0.004		$V_{(SVS\_IT-)}$ x 0.008	
	$V_{CC}/dt \le 3$ V/s (see Figure 13), external voltage applied on A7	VLD = 15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61†	
		VLD = 13	3.24	3.5	3.76†	
		VLD = 14	3.43	3.7†	3.99†	
	$V_{CC}/dt \le 3$ V/s (see Figure 13), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

† The recommended operating voltage range is limited to 3.6 V.

‡ t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTE 1: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

typical characteristics

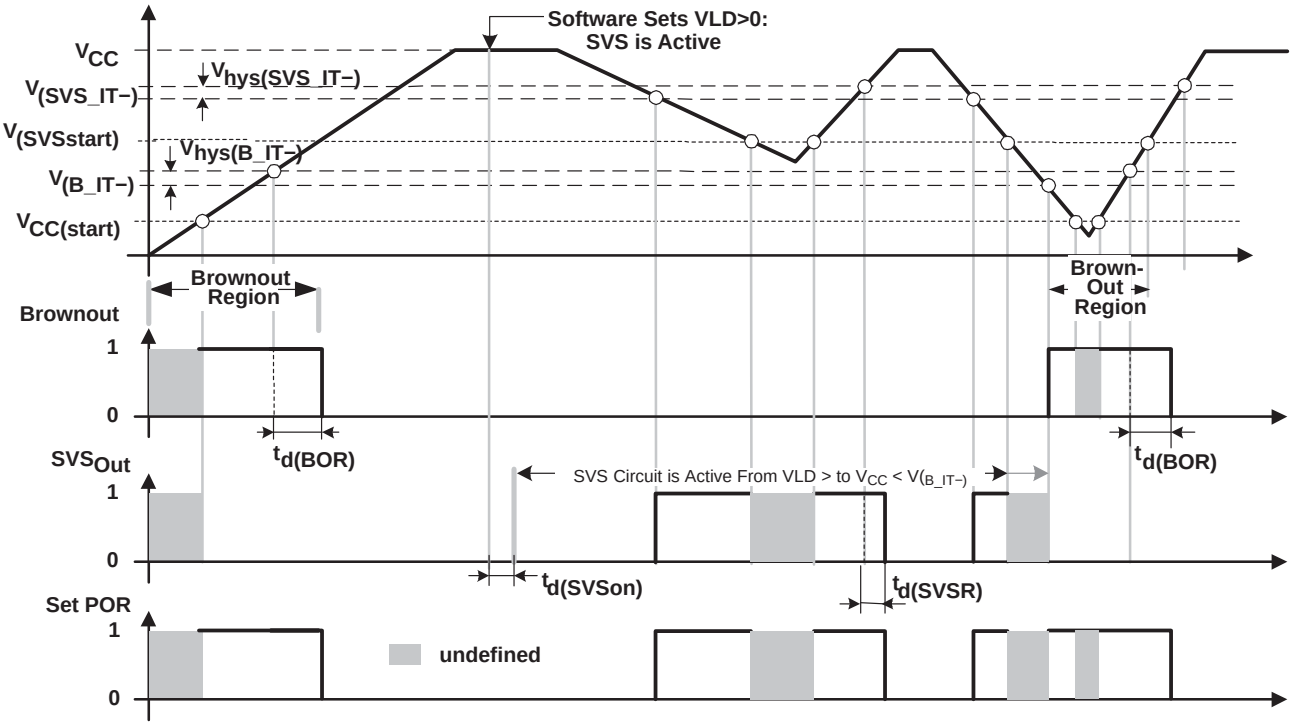


Figure 13. SVS Reset (SVSR) vs Supply Voltage

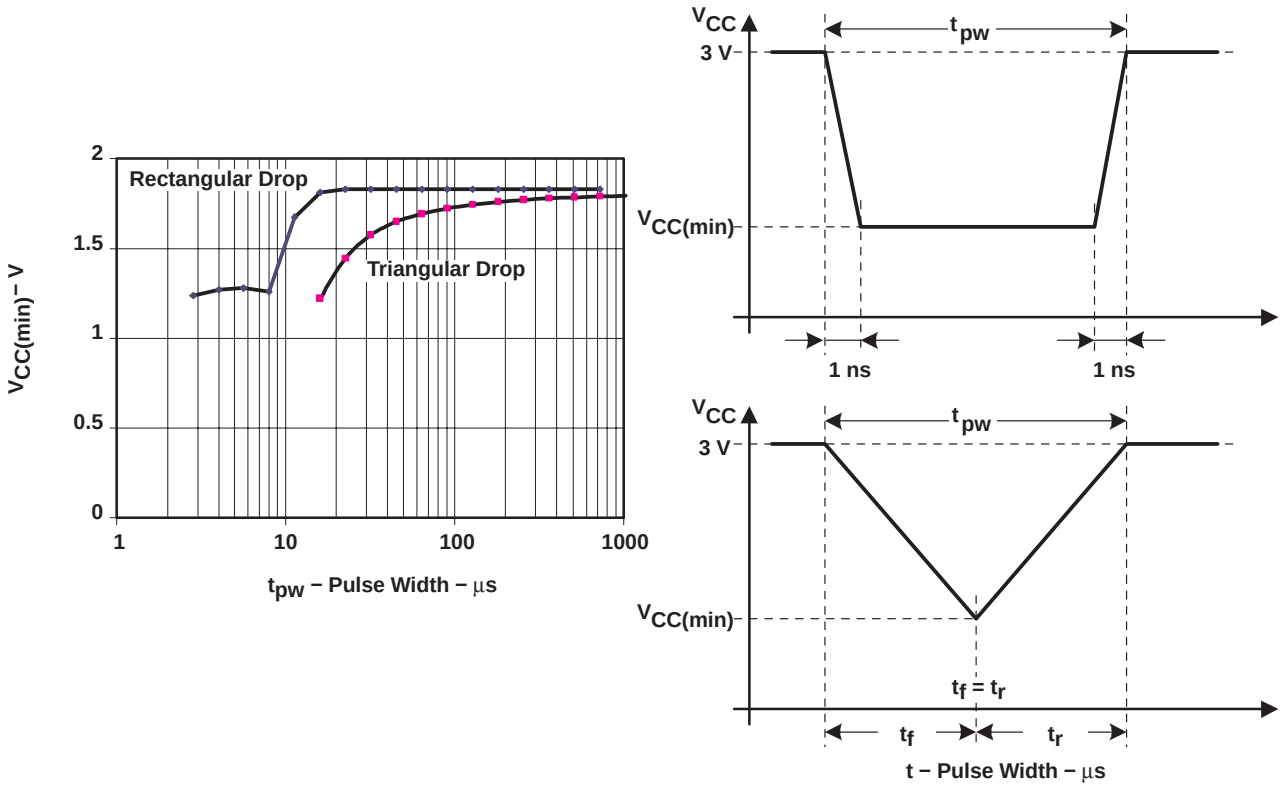


Figure 14. $V_{CC(min)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$=01E0h, FN_8=FN_4=FN_3=FN_2=0, D = 2; DCOPLUS= 0	V_{CC} = 2.2 V/3 V		1		MHz
$f_{(DCO2)}$	FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1	V_{CC} = 2.2 V	0.3	0.65	1.25	MHz
		V_{CC} = 3 V	0.3	0.7	1.3	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1, (see Note 1)	V_{CC} = 2.2 V	2.5	5.6	10.5	MHz
		V_{CC} = 3 V	2.7	6.1	11.3	
$f_{(DCO2)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1	V_{CC} = 2.2 V	0.7	1.3	2.3	MHz
		V_{CC} = 3 V	0.8	1.5	2.5	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1, (see Note 1)	V_{CC} = 2.2 V	5.7	10.8	18	MHz
		V_{CC} = 3 V	6.5	12.1	20	
$f_{(DCO2)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1	V_{CC} = 2.2 V	1.2	2	3	MHz
		V_{CC} = 3 V	1.3	2.2	3.5	
$f_{(DCO27)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1, (see Note 1)	V_{CC} = 2.2 V	9	15.5	25	MHz
		V_{CC} = 3 V	10.3	17.9	28.5	
$f_{(DCO2)}$	FN_8=0, FN_4= 1, FN_3= FN_2=x; DCOPLUS = 1	V_{CC} = 2.2 V	1.8	2.8	4.2	MHz
		V_{CC} = 3 V	2.1	3.4	5.2	
$f_{(DCO27)}$	FN_8=0, FN_4=1, FN_3= FN_2=x; DCOPLUS = 1, (see Note 1)	V_{CC} = 2.2 V	13.5	21.5	33	MHz
		V_{CC} = 3 V	16	26.6	41	
$f_{(DCO2)}$	FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1	V_{CC} = 2.2 V	2.8	4.2	6.2	MHz
		V_{CC} = 3 V	4.2	6.3	9.2	
$f_{(DCO27)}$	FN_8=1,FN_4=FN_3=FN_2=x; DCOPLUS = 1, (see Note 1)	V_{CC} = 2.2 V	21	32	46	MHz
		V_{CC} = 3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$, (see Figure 16 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0, (see Note 2)	V_{CC} = 2.2 V	–0.2	–0.3	–0.4	%/°C
		V_{CC} = 3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0, D= 2; DCOPLUS = 0 (see Note 2)	V_{CC} = 2.2 V/3 V	0	5	15	%/V

NOTES: 1. Do not exceed the maximum system frequency.
2. This parameter not production tested.

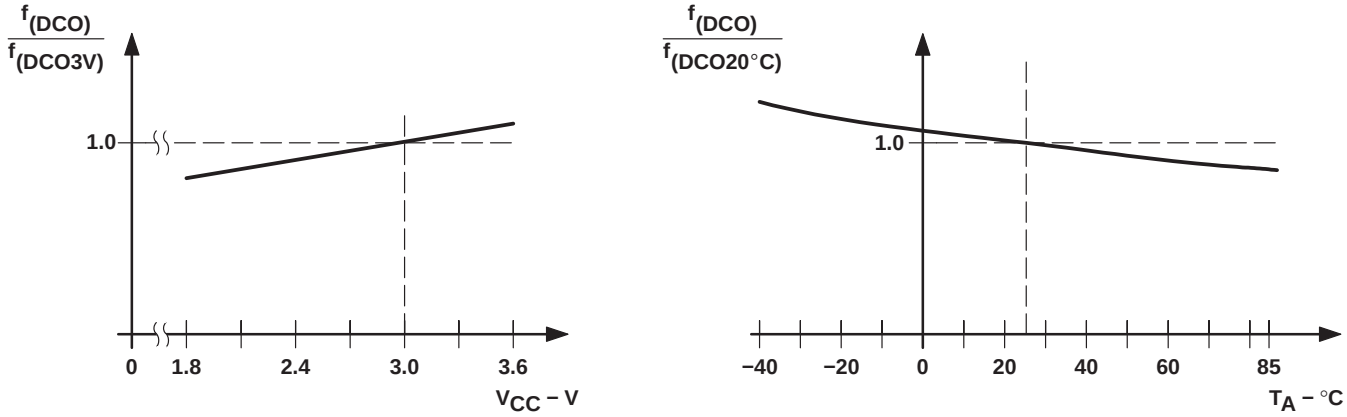


Figure 15. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

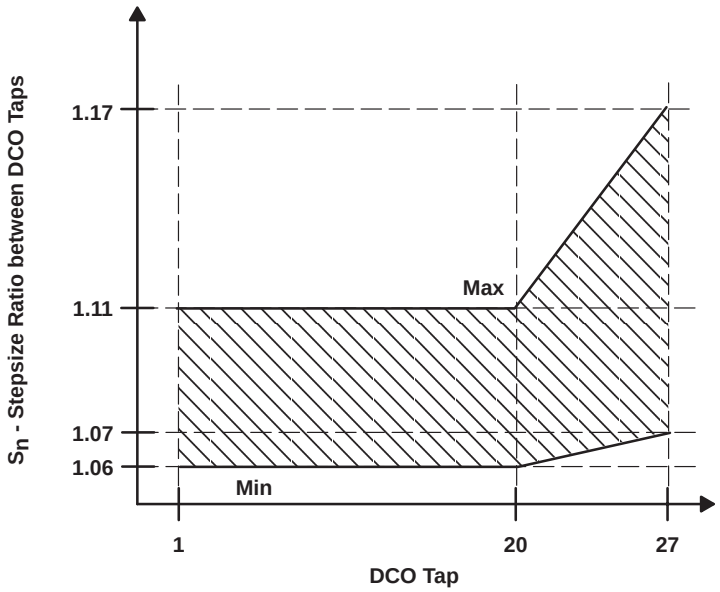


Figure 16. DCO Tap Step Size

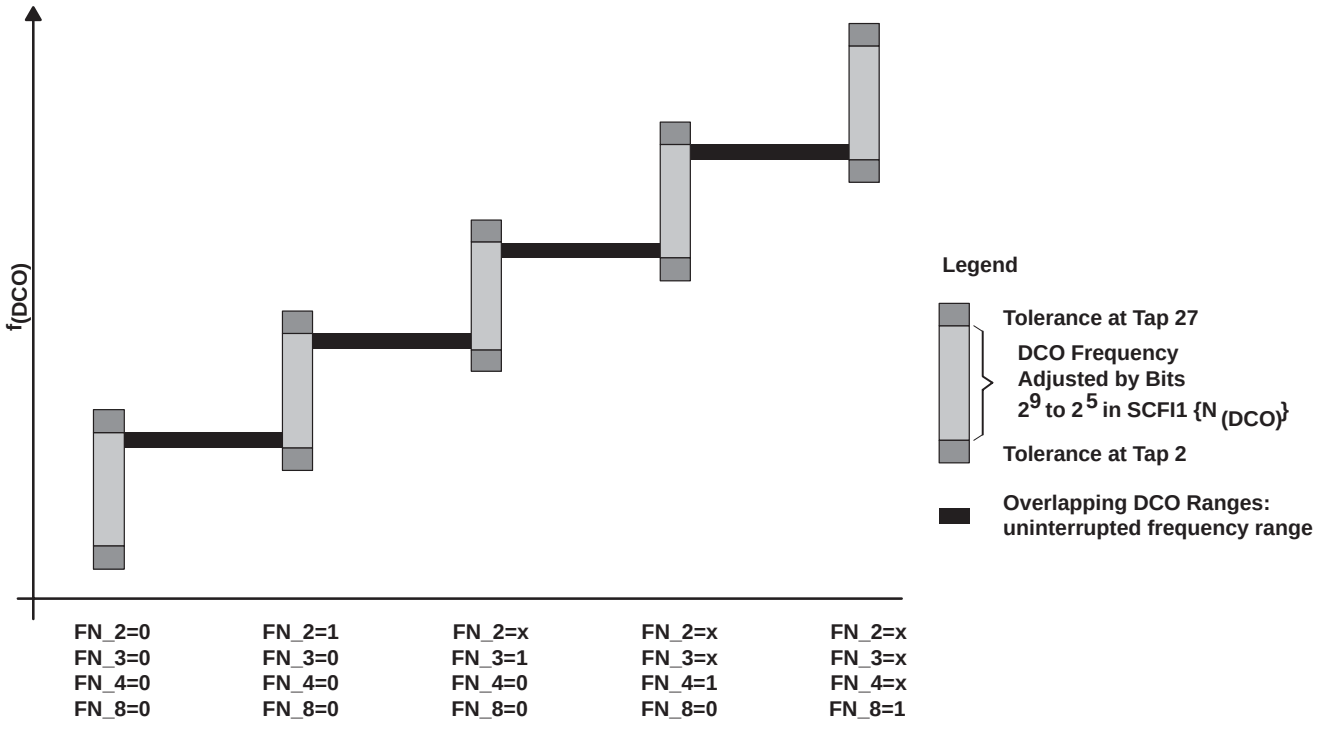


Figure 17. Five Overlapping DCO Ranges Controlled by FN_x Bits

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
C_{XOUT}	Integrated output capacitance	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V/3 V (see Note 3)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	V

NOTES: 1. The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is (C_{XIN} x C_{XOUT}) / (C_{XIN} + C_{XOUT}). This is independent of XTS_FLL.
2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
   - Keep as short of a trace as possible between the 'F43x/44x and the crystal.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications; OSCCAPx = 0h.

crystal oscillator, XT2 oscillator (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{XT2IN}	Integrated input capacitance	V_{CC} = 2.2 V/3 V		2		pF
C_{XT2OUT}	Integrated output capacitance	V_{CC} = 2.2 V/3 V		2		pF
V_{IL}	Input levels at XT2IN	V_{CC} = 2.2 V/3 V (see Note 2)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	V

NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

USART0, USART1 (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(\tau)}$	USART0/1: deglitch time	V_{CC} = 2.2 V	200	430	800	ns
		V_{CC} = 3 V	150	280	500	

NOTE 1: The signal applied to the USART0/1 receive signal/terminal (URXD0/1) should meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0/1 line.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range (see Note 2)	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $0 \le x \le 7$; $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal (see Note 3)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	2.2 V		0.65	1.3	mA
			3 V		0.8	1.6	
I_{REF+}	Operating supply current into AV_{CC} terminal (see Note 4)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V		0.5	0.8	mA
			3 V		0.5	0.8	
C_I †	Input capacitance	Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
R_I†	Input MUX ON resistance	$0V \le V_{Ax} \le V_{AVCC}$	3 V			2000	Ω

† Not production tested, limits verified by design

NOTES: 1. The leakage current is defined in the leakage current table with P6.x/Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC12}.
4. The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

12-bit ADC, external reference (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 2)		1.4		V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 3)		0		1.2	V
$(V_{eREF+} - V_{REF-}/V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 4)		1.4		V_{AVCC}	V
I_{VeREF+}	Static input current	$0V \le V_{eREF+} \le V_{AVCC}$	2.2 V/3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current	$0V \le V_{eREF-} \le V_{AVCC}$	2.2 V/3 V			±1	µA

NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, built-in reference

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V $I_{VREF+} \le I_{VREF+}max$	3 V	2.4	2.5	2.6	V
		REF2_5V = 0 for 1.5 V $I_{VREF+} \le I_{VREF+}max$	2.2 V/3 V	1.44	1.5	1.56	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built-in reference active	REF2_5V = 0, $I_{VREF+} \le$ 1mA		2.2			V
		REF2_5V = 1, $I_{VREF+} \le$ 0.5mA		V_{REF+} + 0.15			
		REF2_5V = 1, $I_{VREF+} \le$ 1mA		V_{REF+} + 0.15			
I_{VREF+}	Load current out of V_{REF+} terminal		2.2 V	0.01		−0.5	mA
			3 V			−1	
$I_{L(VREF)+}$ †	Load-current regulation V_{REF+} terminal	I_{VREF+} = 500 µA +/− 100 µA Analog input voltage ~0.75 V; REF2_5V = 0	2.2 V			±2	LSB
			3 V			±2	
		I_{VREF+} = 500 µA ± 100 µA Analog input voltage ~1.25 V; REF2_5V = 1	3 V			±2	LSB
$I_{DL(VREF)+}$ ‡	Load current regulation V_{REF+} terminal	I_{VREF+} =100 µA → 900 µA, C_{VREF+}=5 µF, Ax ~0.5 x V_{REF+} Error of conversion result ≤ 1 LSB	3 V			20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (see Note 1)	REFON =1, 0 mA ≤ $I_{VREF+} \le I_{VREF+}$max	2.2 V/3 V	5	10		µF
T_{REF+}†	Temperature coefficient of built-in reference	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA	2.2 V/3 V			±100	ppm/°C
t_{REFON}†	Settle time of internal reference voltage (see Figure 18 and Note 2)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10µF, V_{REF+} = 1.5 V	2.2 V			17	ms

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10 µF tantalum and 100 nF ceramic.
2. The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

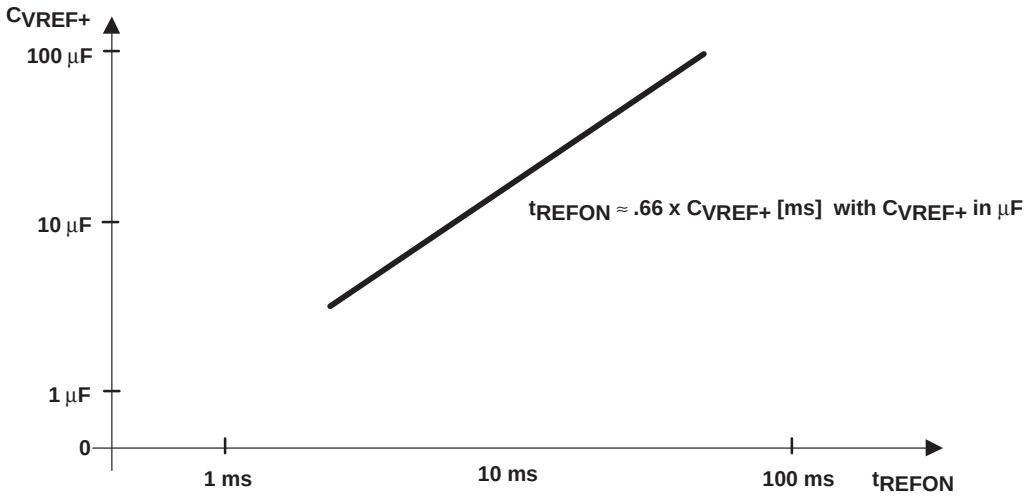


Figure 18. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

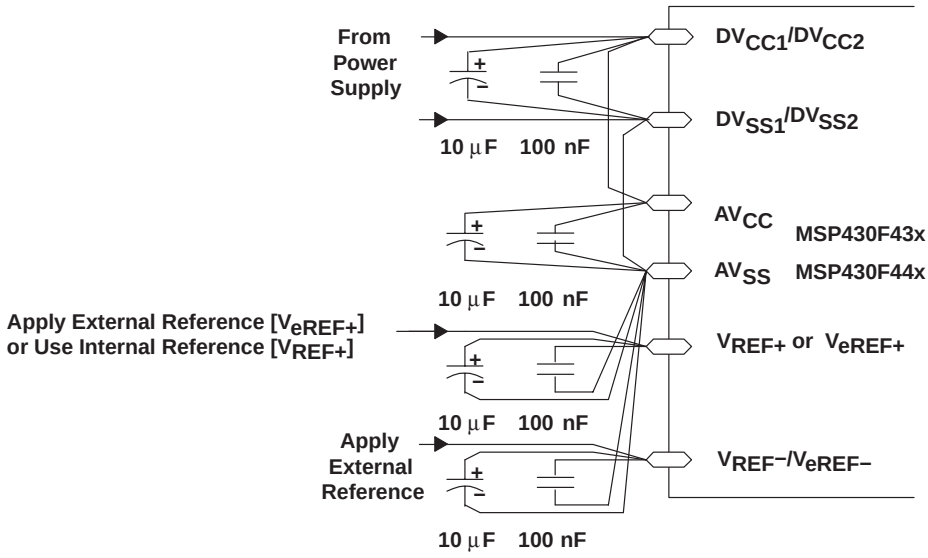


Figure 19. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

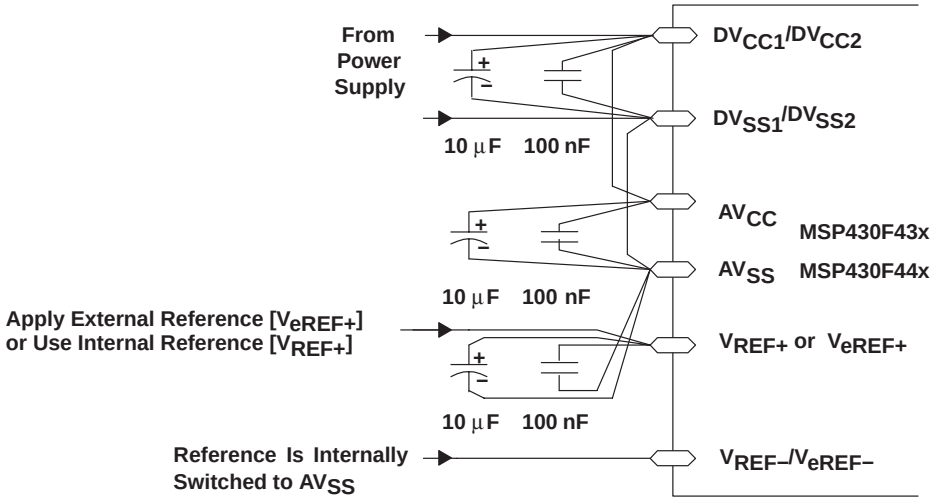


Figure 20. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} = AV_{SS}, Internally Connected

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, timing parameters

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	2.2V/ 3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV=0, $f_{ADC12CLK}=f_{ADC12OSC}$	2.2 V/ 3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	$C_{VREF+} \geq 5$ µF, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V/ 3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK: ADC12SSEL ≠ 0		13×ADC12DIV× $1/f_{ADC12CLK}$			µs
$t_{ADC12ON}$‡	Turn on settling time of the ADC	(see Note 1)				100	ns
t_{Sample}‡	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, τ = [R_S + R_I] x C_I;(see Note 2)	3 V	1220			ns
			2.2 V	1400			

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
2. Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns where n = ADC resolution = 12, R_S = external source resistance.

12-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ 1.6 V	2.2 V/3 V			±2	LSB
		1.6 V < (V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ [$V_{(AVCC)}$]				±1.7	
E_D	Differential linearity error	(V_{eREF+} − V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V			±1	LSB
E_O	Offset error	(V_{eREF+} − V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), Internal impedance of source R_S < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±4	LSB
E_G	Gain error	(V_{eREF+} − V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error	(V_{eREF+} − V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±5	LSB

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, temperature sensor and built-in V_{MID}

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (see Note 1)	REFON = 0, INCH = 0Ah, ADC12ON=NA, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}†		ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986	986±5%	mV
			3 V		986	986±5%	
TC_{SENSOR}†		ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55±3%	mV/°C
			3 V		3.55	3.55±3%	
$t_{SENSOR(sample)}$†	Sample time required if channel 10 is selected (see Note 2)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11	ADC12ON = 1, INCH = 0Bh, (see Note 3)	2.2 V			NA	µA
			3 V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 x V_{AVCC}	2.2 V		1.1	1.1±0.04	V
			3 V		1.5	1.50±0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (see Note 4)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

† Not production tested, limits characterized

NOTES: 1. The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON=1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high). Therefore it includes the constant current through the sensor and the reference.
2. The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
3. No additional current is needed. The V_{MID} is used during sampling.
4. The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Flash Memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.7		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.7 V/ 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.7 V/ 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.7 V/ 3.6 V			4	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.7 V/ 3.6 V	200			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

JTAG Interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

JTAG Fuse (see Note 1)

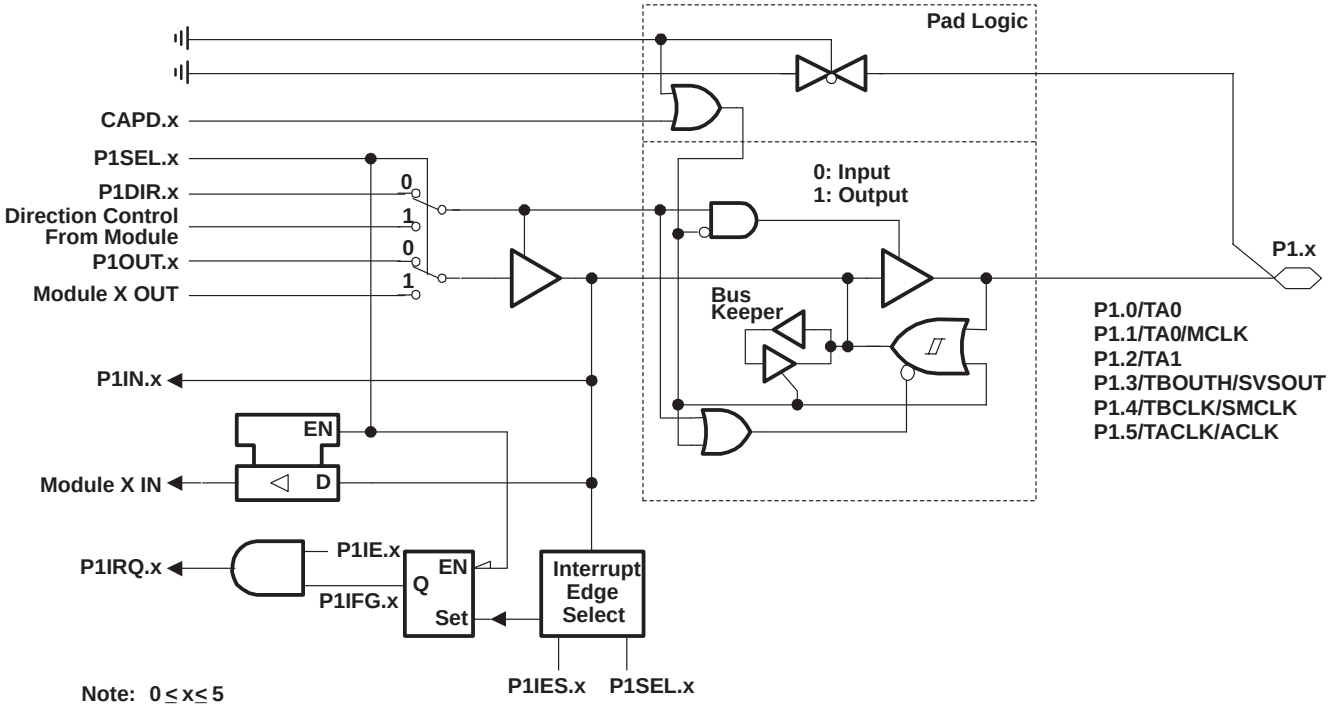
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6		7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.5, input/output with Schmitt-trigger



Note: 0 ≤ x ≤ 5
Note: Port function is active if CAPD.x = 0

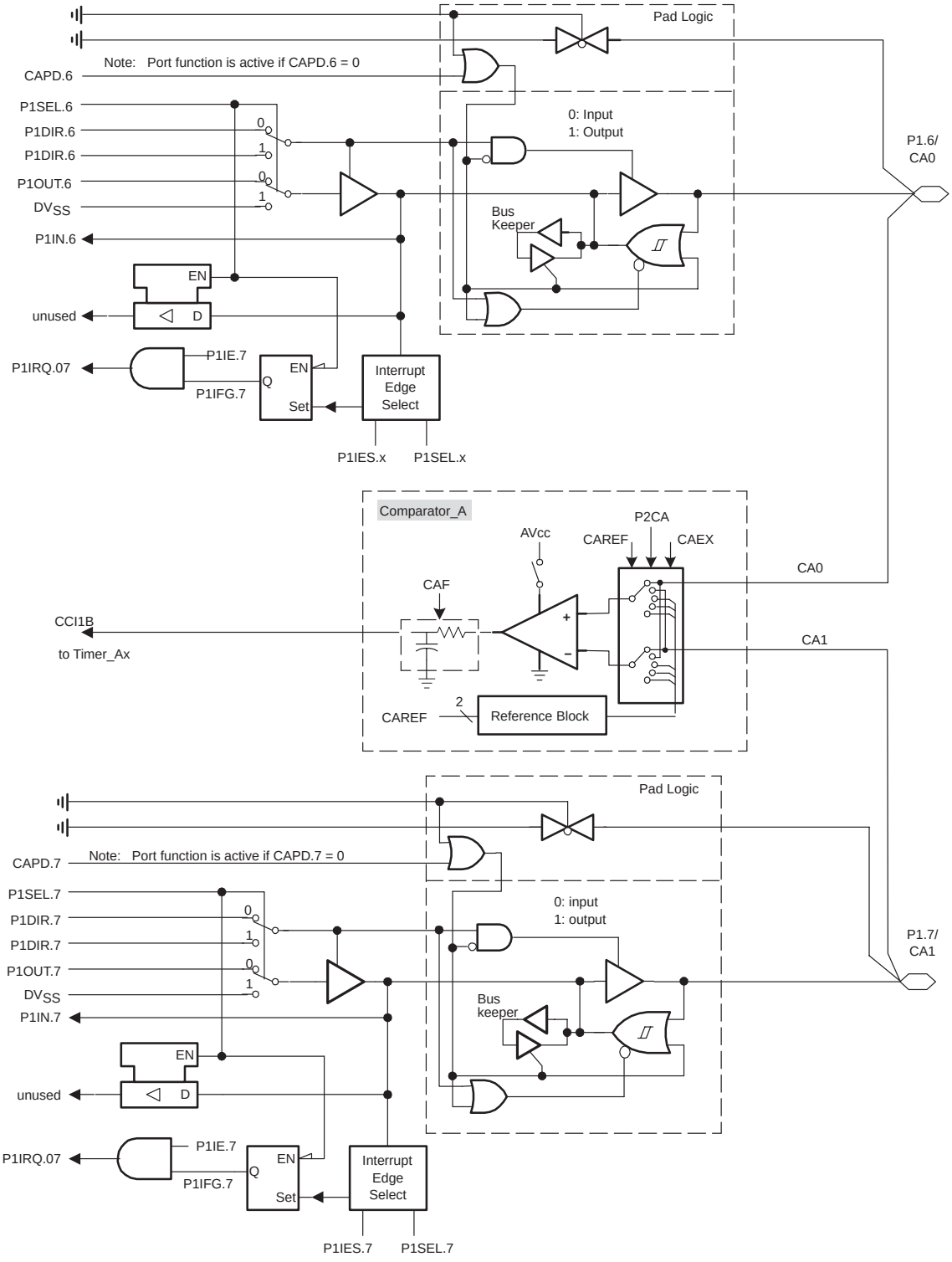
PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	Out0 sig. †	P1IN.0	CCI0A †	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	MCLK	P1IN.1	CCI0B †	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 sig. †	P1IN.2	CCI1A †	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	SVSOUT	P1IN.3	TBOUTH ‡	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	TBCLK ‡	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	ACLK	P1IN.5	TACLK †	P1IE.5	P1IFG.5	P1IES.5

† Timer_A
‡ Timer_B

APPLICATION INFORMATION

input/output schematic (continued)

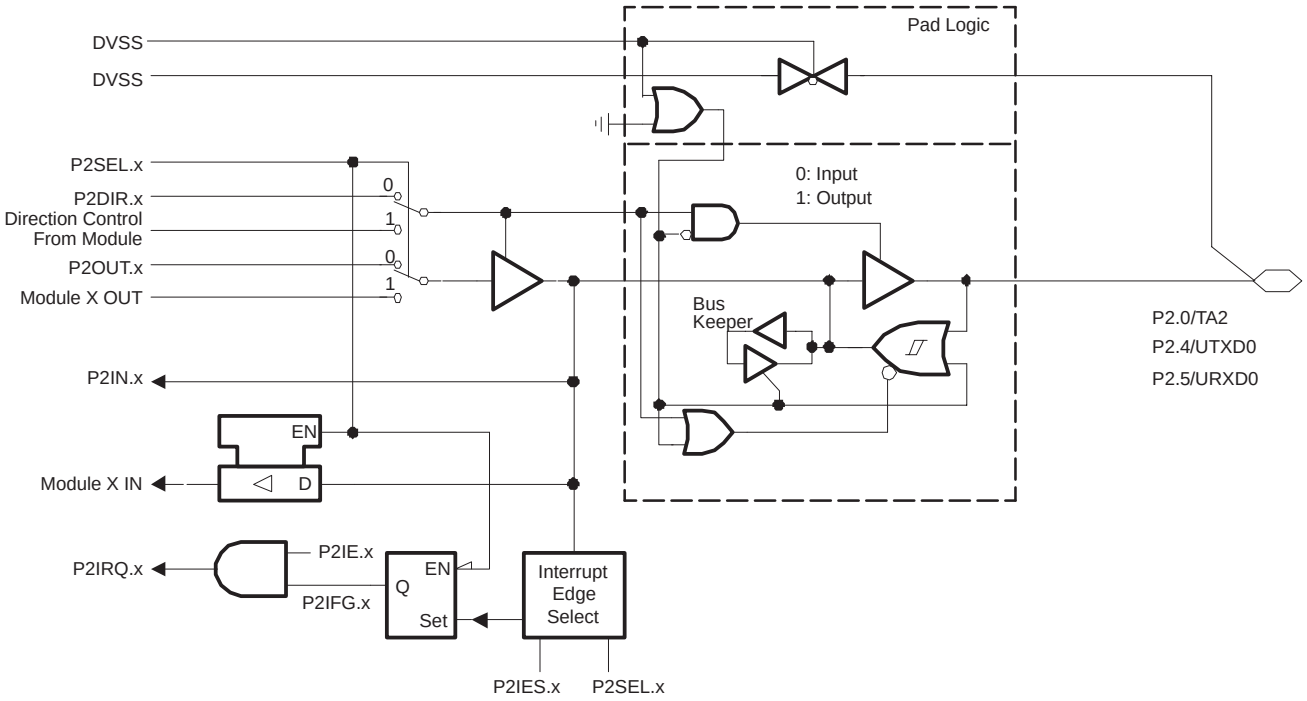
Port P1, P1.6, P1.7, input/output with Schmitt-trigger



APPLICATION INFORMATION

input/output schematic (continued)

port P2, P2.0, P2.4 to P2.5, input/output with Schmitt-trigger



Note: x {0,4,5}

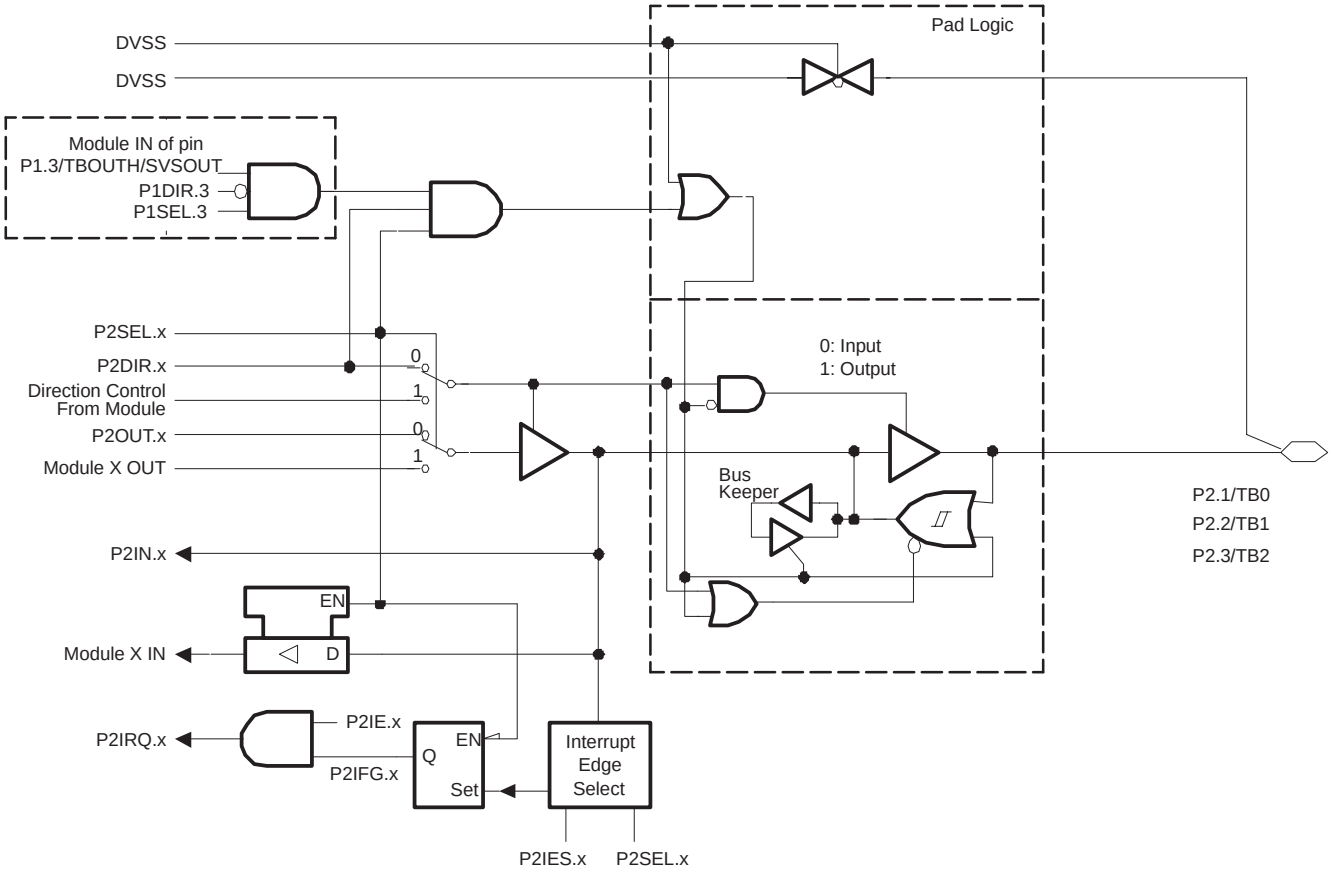
PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	Out2 sig. †	P2IN.0	CCI2A †	P2IE.0	P2IFG.0	P2IES.0
P2Sel.4	P2DIR.4	DV_{CC}	P2OUT.4	UTXD0 ‡	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4
P2Sel.5	P2DIR.5	DV_{SS}	P2OUT.5	DV_{SS}	P2IN.5	URXD0 ‡	P2IE.5	P2IFG.5	P2IES.5

†Timer_A
‡USART0

APPLICATION INFORMATION

input/output schematic (continued)

port P2, P2.1 to P2.3, input/output with Schmitt-trigger



Note: $1 \le x \le 3$

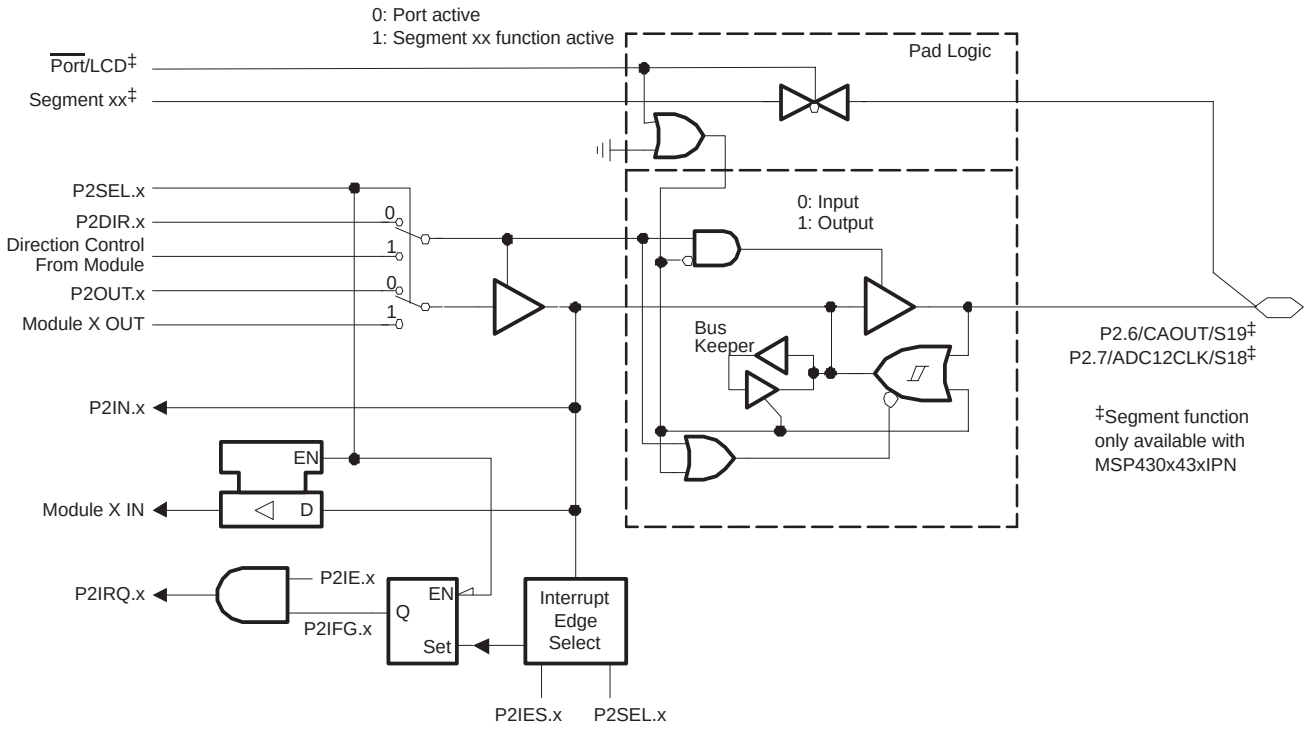
PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	Out0 sig. †	P2IN.1	CCI0A † CCI0B	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	Out1 sig. †	P2IN.2	CCI1A † CCI1B	P2IE.2	P2IFG.2	P2IES.2
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out2 sig. †	P2IN.3	CCI2A † CCI2B	P2IE.3	P2IFG.3	P2IES.3

†Timer_B

APPLICATION INFORMATION

input/output schematic (continued)

port P2, P2.6 to P2.7, input/output with Schmitt-trigger



Note: $6 \le x \le 7$

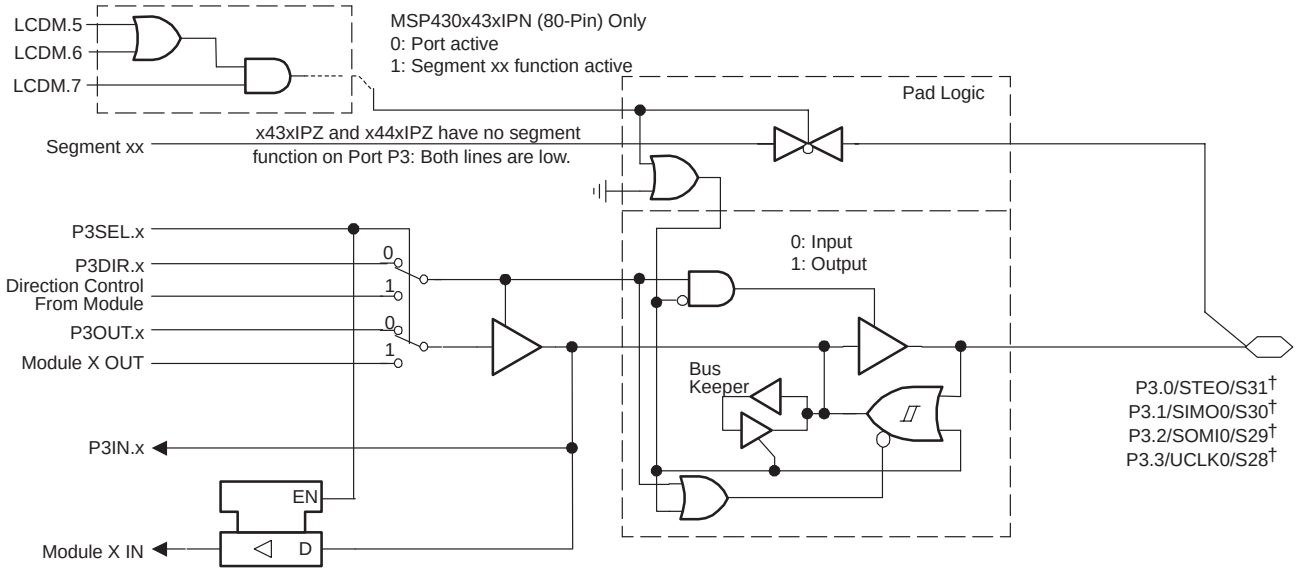
PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x	Port/LCD‡
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	CAOUT†	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6	0: LCDM<40h‡
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	ADC12CLK§	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7	0: LCDM<40h‡

† Comparator_A
‡Port/LCD signal is 1 only with MSP430xIPN and LCDM ≥40h.
§ ADC12

APPLICATION INFORMATION

input/output schematic (continued)

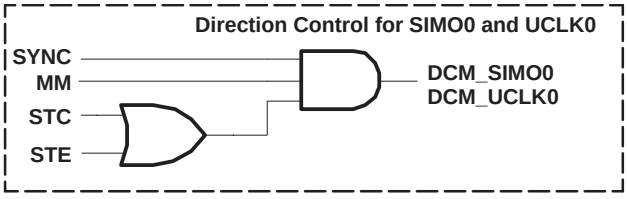
port P3, P3.0 to P3.3, input/output with Schmitt-trigger

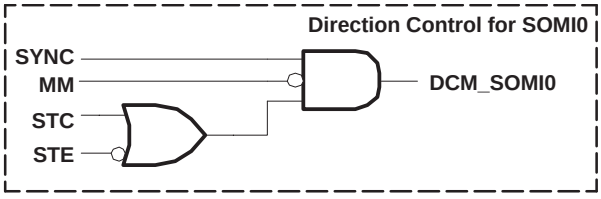


Note: $0 \le x \le 3$

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3Sel.0	P3DIR.0	DV_{SS}	P3OUT.0	DV_{SS}	P3IN.0	STE0(in)
P3Sel.1	P3DIR.1	DCM_SIMO0	P3OUT.1	SIMO0(out)	P3IN.1	SIMO0(in)
P3Sel.2	P3DIR.2	DCM_SOMI0	P3OUT.2	SOMIO(out)	P3IN.2	SOMI0(in)
P3Sel.3	P3DIR.3	DCM_UCLK0	P3OUT.3	UCLK0(out)	P3IN.3	UCLK0(in)

† S24 to S31 shared with port function only at MSP430x43xIPN (80-pin QFP)

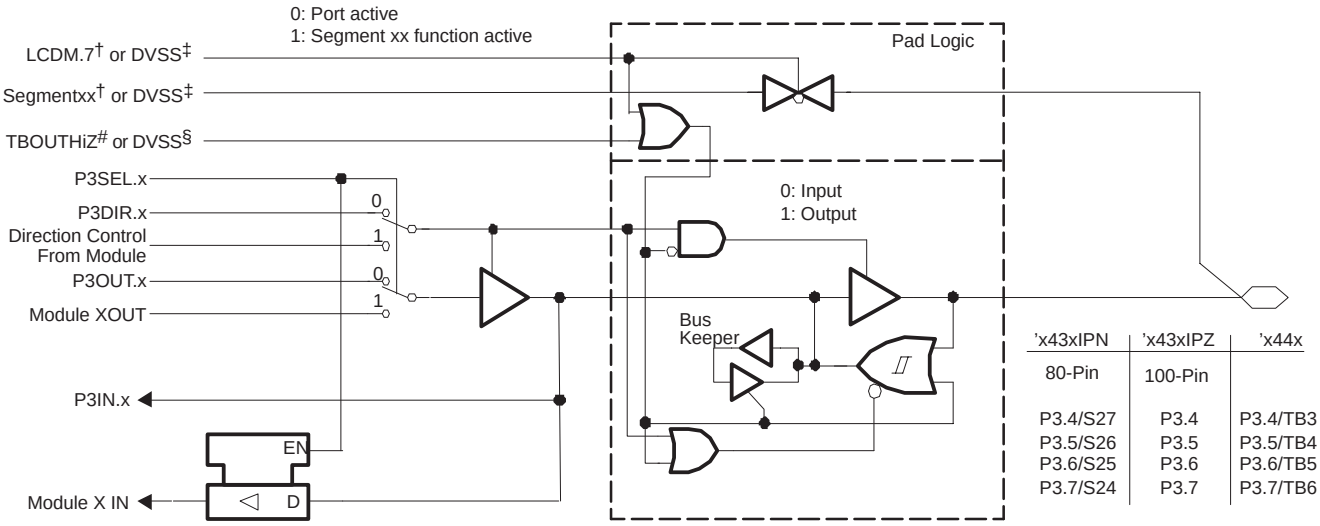




APPLICATION INFORMATION

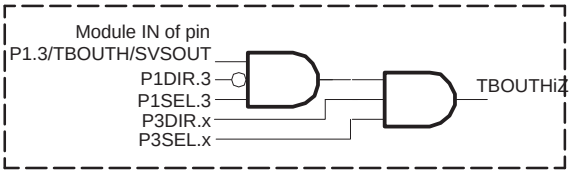
input/output schematic (continued)

port P3, P3.4 to P3.7, input/output with Schmitt-trigger



'x43xIPN	'x43xIPZ	'x44x
80-Pin	100-Pin	
P3.4/S27	P3.4	P3.4/TB3
P3.5/S26	P3.5	P3.5/TB4
P3.6/S25	P3.6	P3.6/TB5
P3.7/S24	P3.7	P3.7/TB6

Note: $4 \le x \le 7$



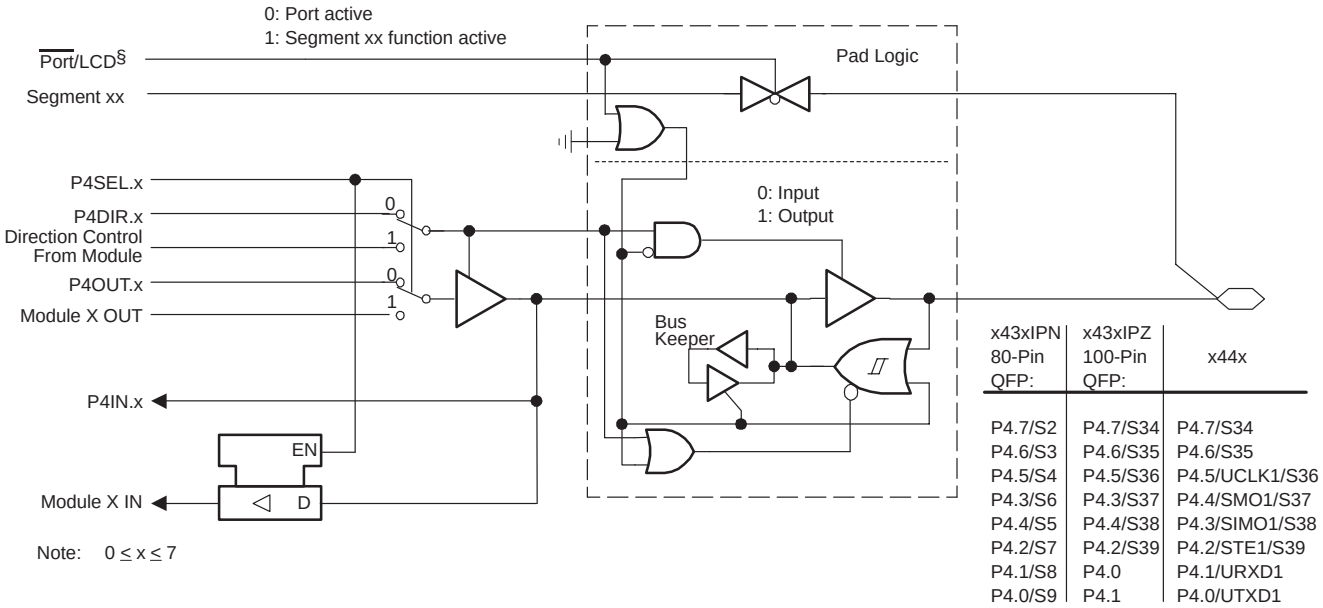
PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3Sel.4	P3DIR.4	P3DIR.4	P3OUT.4	DVSS § OUT3 #	P3IN.4	unused § CCI3A/B#
P3Sel.5	P3DIR.5	P3DIR.5	P3OUT.5	DVSS § OUT4 #	P3IN.5	unused § CCI4A/B#
P3Sel.6	P3DIR.6	P3DIR.6	P3OUT.6	DVSS § OUT5 #	P3IN.6	unused § CCI5A/B#
P3Sel.7	P3DIR.7	P3DIR.7	P3OUT.7	DVSS § OUT6 #	P3IN.7	unused § CCI6A #

† MSP430x43xIPN
‡ MSP430x43xIPZ, MSP430x44xIPZ
§ MSP430x43x
# MSP430x44x

APPLICATION INFORMATION

input/output schematic (continued)

port P4, P4.0 to P4.7, input/output with Schmitt-trigger



x43xIPN 80-Pin QFP:	x43xIPZ 100-Pin QFP:	x44x
P4.7/S2	P4.7/S34	P4.7/S34
P4.6/S3	P4.6/S35	P4.6/S35
P4.5/S4	P4.5/S36	P4.5/UCLK1/S36
P4.3/S6	P4.3/S37	P4.4/SMO1/S37
P4.4/S5	P4.4/S38	P4.3/SIMO1/S38
P4.2/S7	P4.2/S39	P4.2/STE1/S39
P4.1/S8	P4.0	P4.1/URXD1
P4.0/S9	P4.1	P4.0/UTXD1

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4Sel.0	P4DIR.0	P4DIR.0† DV_{CC}‡	P4OUT.0	DV_{SS}† UTXD1‡	P4IN.0	unused
P4Sel.1	P4DIR.1	P4DIR.1† DV_{SS}‡	P4OUT.1	DV_{SS}	P4IN.1	unused† URXD1‡
P4Sel.2	P4DIR.2	P4DIR.2† DV_{SS}‡	P4OUT.2	DV_{SS}	P4IN.2	unused† STE1(in)‡
P4Sel.3	P4DIR.3	P4DIR3.† DCM_SIMO1‡	P4OUT.3	DV_{SS}† SIMO1(out)‡	P4IN.3	unused† SIMO1(in)‡
P4Sel.4	P4DIR.4	P4DIR4.† DCM_SOMI1‡	P4OUT.4	DV_{SS}† SOMI1(out)‡	P4IN.4	unused SOMI1(in)‡
P4Sel.5	P4DIR.5	P4DIR5.† DCM_UCLK1‡	P4OUT.5	DV_{SS}† UCLK1(out)‡	P4IN.5	unused† UCLK1(in)‡
P4Sel.6	P4DIR.4	P4DIR.6	P4OUT.6	DV_{SS}	P4IN.6	unused
P4Sel.7	P4DIR.5	P4DIR.7	P4OUT.7	DV_{SS}	P4IN.7	unused

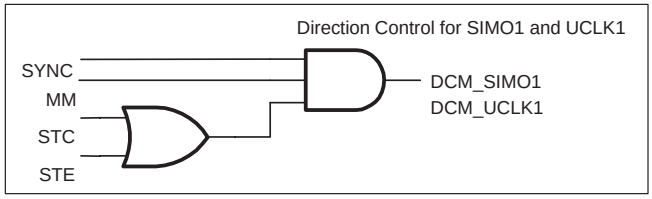
† Signal at MSP430x43x
‡ Signal at MSP430x44x
§

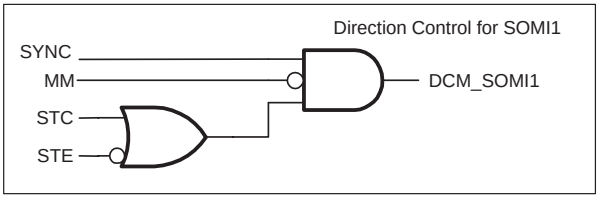
DEVICE	PORT BITS	PORT FUNCTION	LCD SEG. FUNCTION
x43xIPN 80-pin QFP	P4.0 . . .P4.7	LCDM < 020h	LCDM ≥ 020h
x43xIPZ 100-pin QFP	P4.2 . . .P4.5	LCDM < 0E0h	LCDM ≥ 0E0h
x44xIPZ 100-pin QFP	P4.6 . . .P4.7	LCDM < 0C0h	LCDM ≥ 0C0h

APPLICATION INFORMATION

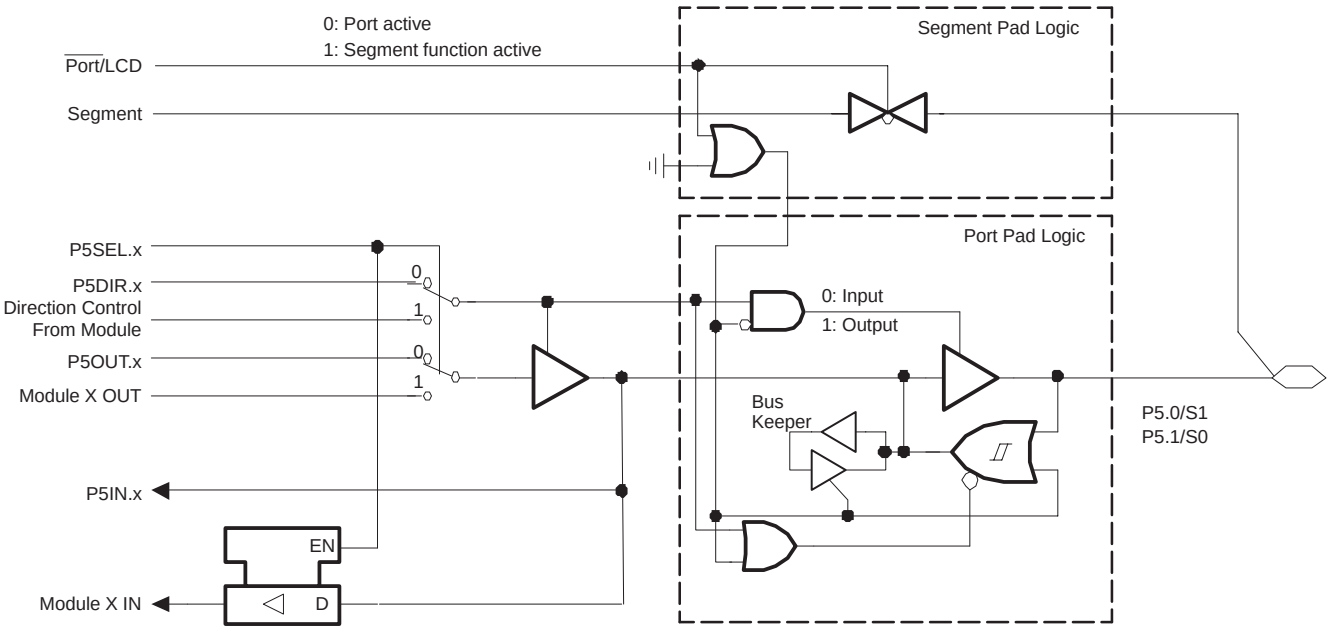
input/output schematic (continued)

port P4, P4.0 to P4.7, input/output with Schmitt-trigger (continued)





port P5, P5.0 to P5.1, input/output with Schmitt-trigger



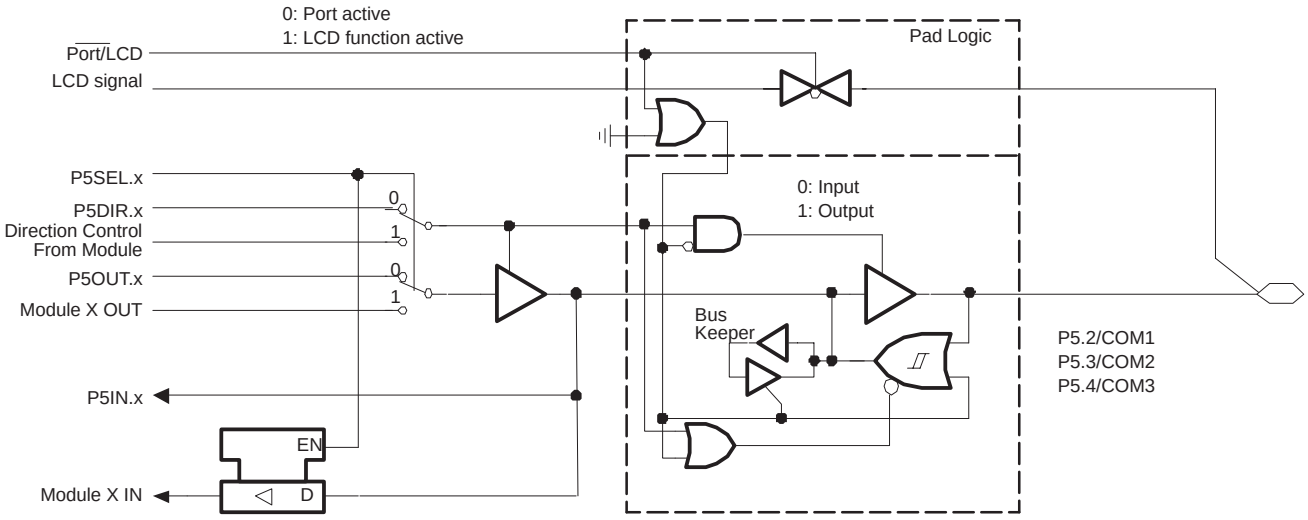
Note: $0 \le x \le 1$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	Segment	Port/LCD
P5Sel.0	P5DIR.0	P5DIR.0	P5OUT.0	DV_{SS}	P5IN.0	unused	S1	0: LCDM<20h
P5Sel.1	P5DIR.1	P5DIR.1	P5OUT.1	DV_{SS}	P5IN.1	unused	S0	0: LCDM<20h

APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.2 to P5.4, input/output with Schmitt-trigger



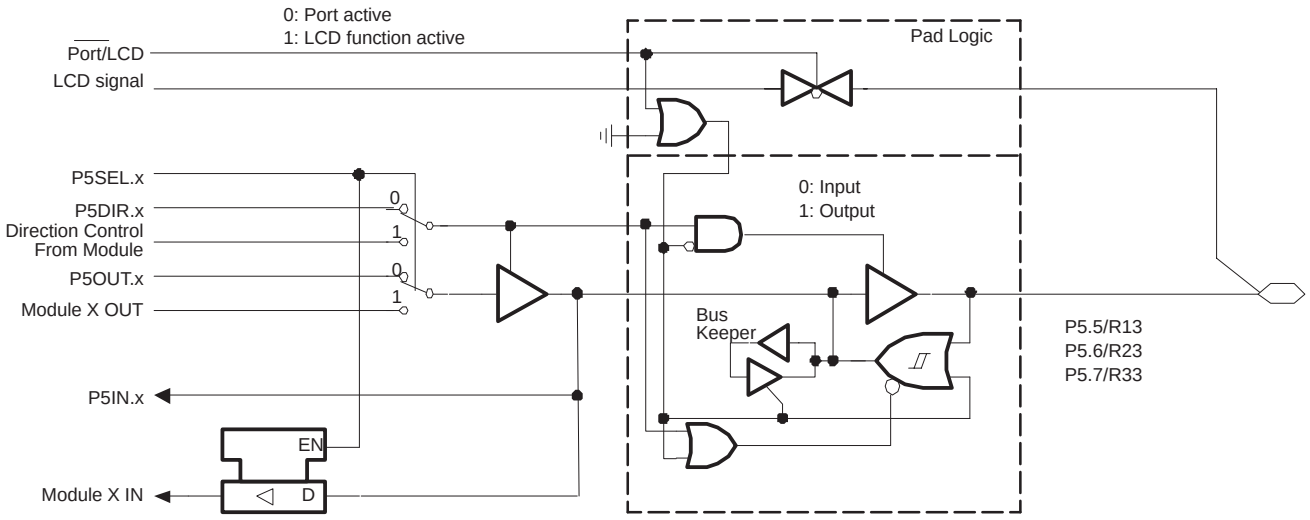
Note: $2 \le x \le 4$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	LCD signal	Port/LCD
P5Sel.2	P5DIR.2	P5DIR.2	P5OUT.2	DV_{SS}	P5IN.2	unused	COM1	P5SEL.2
P5Sel.3	P5DIR.3	P5DIR.3	P5OUT.3	DV_{SS}	P5IN.3	unused	COM2	P5SEL.3
P5Sel.4	P5DIR.4	P5DIR.4	P5OUT.4	DV_{SS}	P5IN.4	unused	COM3	P5SEL.4

APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.5 to P5.7, input/output with Schmitt-trigger



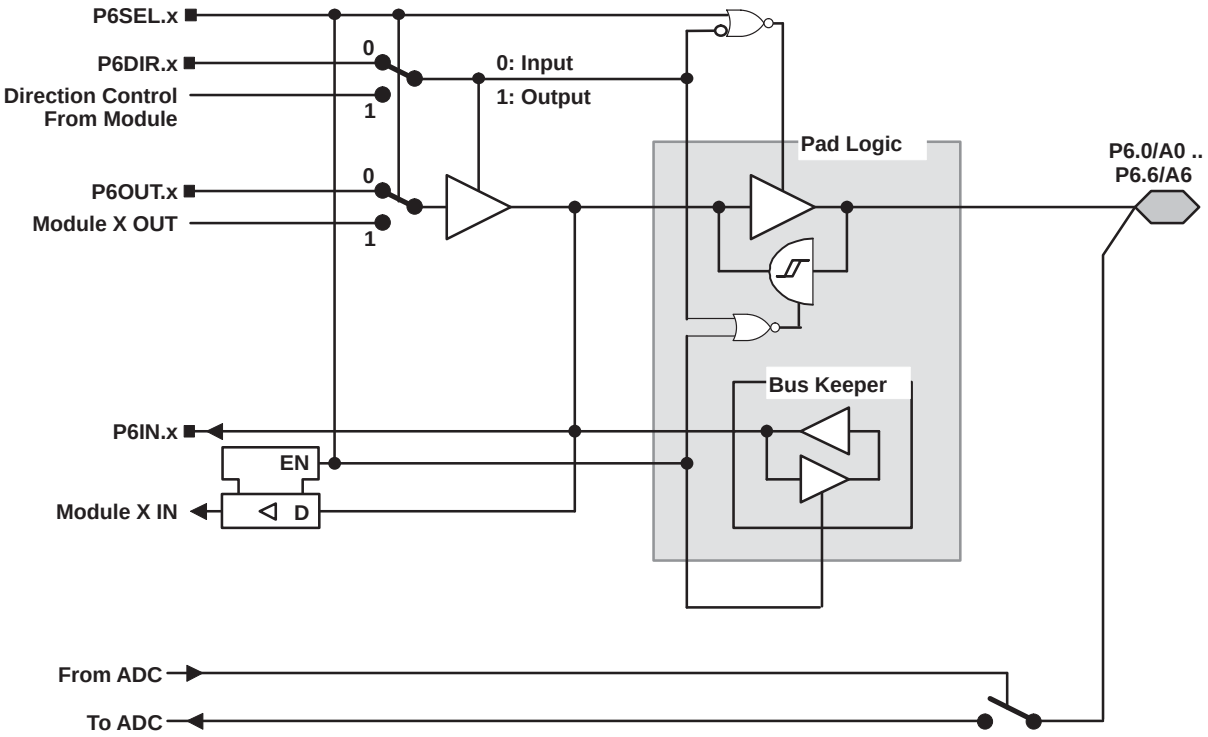
Note: $5 \le x \le 7$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	LCD signal	Port/LCD
P5Sel.5	P5DIR.5	P5DIR.5	P5OUT.5	DV_{SS}	P5IN.5	unused	R13	P5SEL.5
P5Sel.6	P5DIR.6	P5DIR.6	P5OUT.6	DV_{SS}	P5IN.6	unused	R23	P5SEL.6
P5Sel.7	P5DIR.7	P5DIR.7	P5OUT.7	DV_{SS}	P5IN.7	unused	R33	P5SEL.7

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.0 to P6.6, input/output with Schmitt-trigger



x: Bit Identifier, 0 to 6 for Port P6

NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 μA.
Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, even if the signal at the pin is not being used by the ADC12.

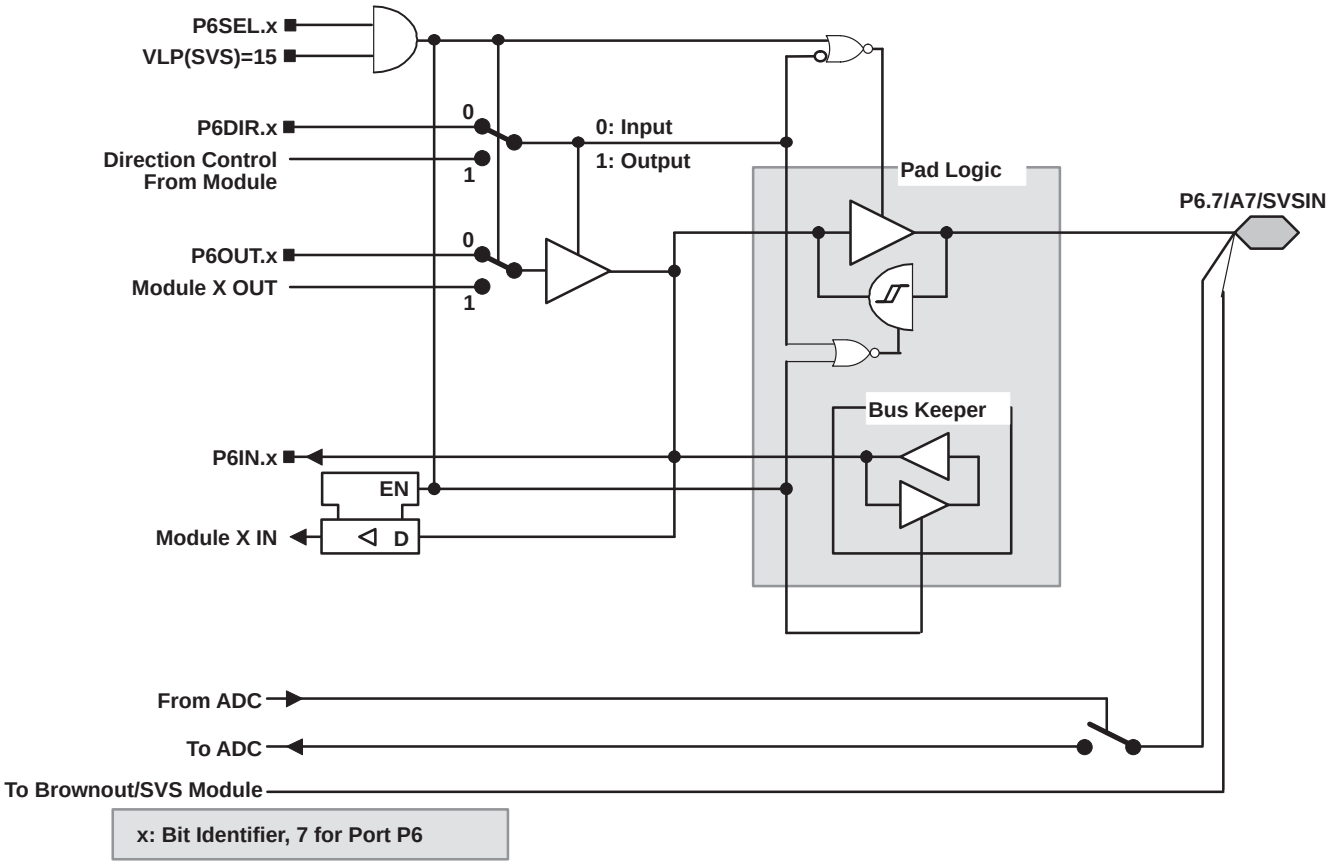
PnSel.x	PnDIR.x	Dir. Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV_{SS}	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused
P6Sel.6	P6DIR.6	P6DIR.6	P6OUT.6	DV_{SS}	P6IN.6	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.7, input/output with Schmitt-trigger



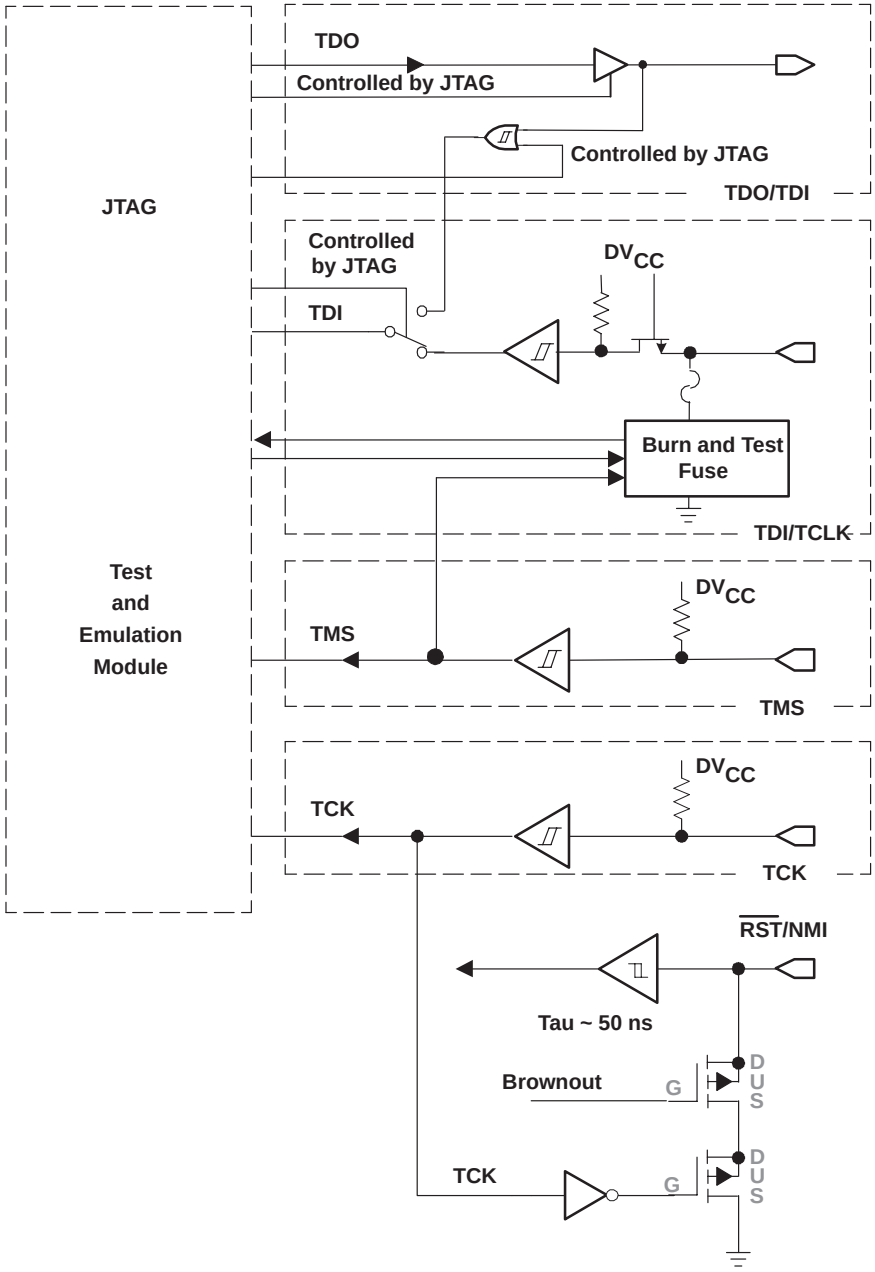
NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 μA.
Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, even if the signal at the pin is not being used by the ADC12.

PnSel.x	PnDIR.x	Dir. Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.7	P6DIR.7	P6DIR.7	P6OUT.7	DV_{SS}	P6IN.7	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.
The signal at pin P6.7/A7/SVSIN is also connected to the input multiplexer in the module brownout/supply voltage supervisor.

APPLICATION INFORMATION

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger or output



APPLICATION INFORMATION

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ($I_{(TF)}$) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 21). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

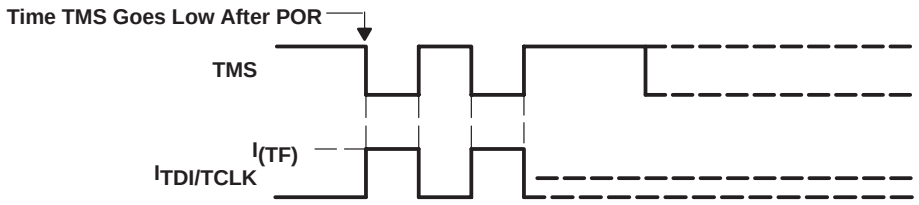
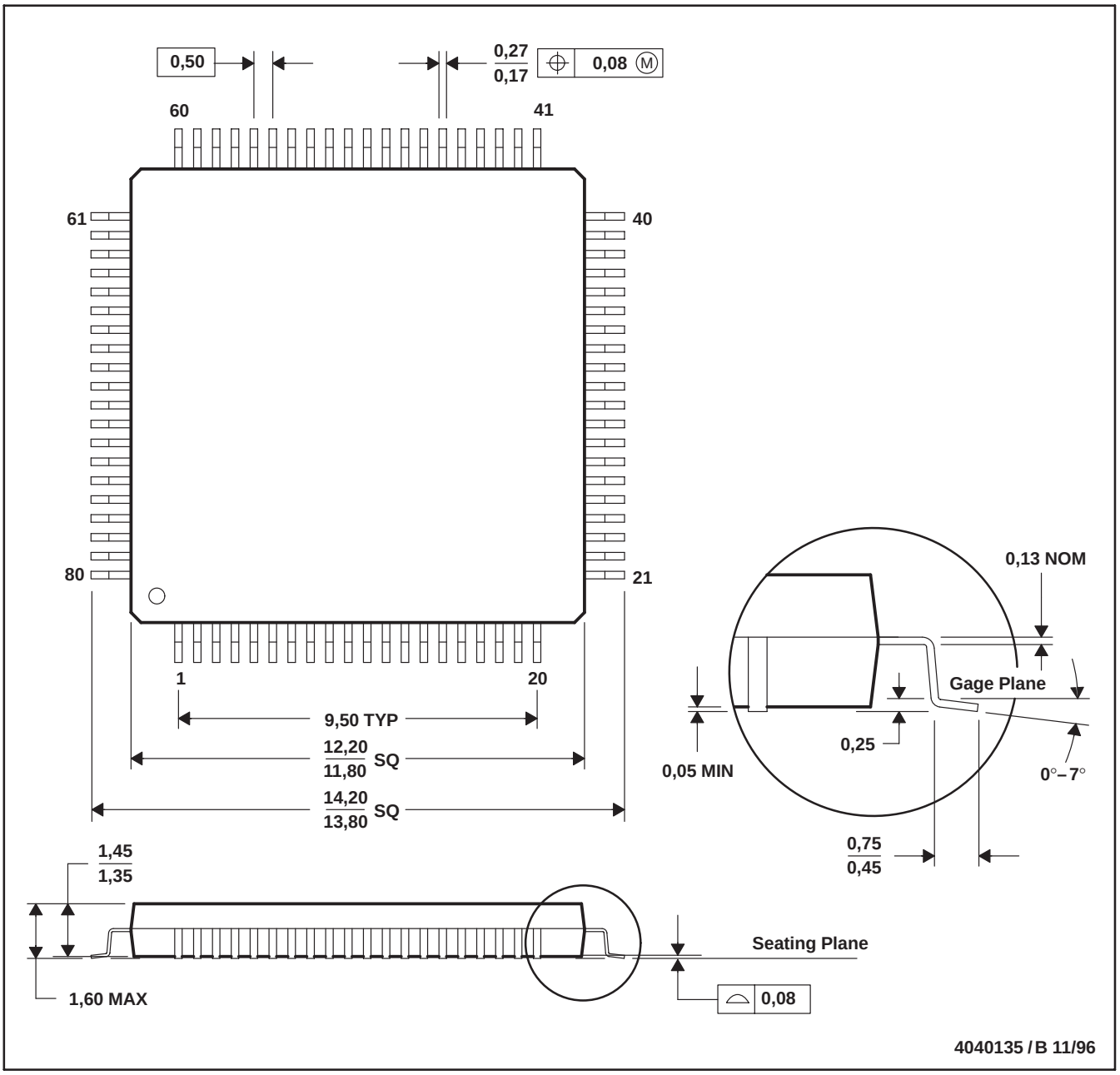


Figure 21. Fuse Check Mode Current MSP430x43x, MSP430x44x

MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

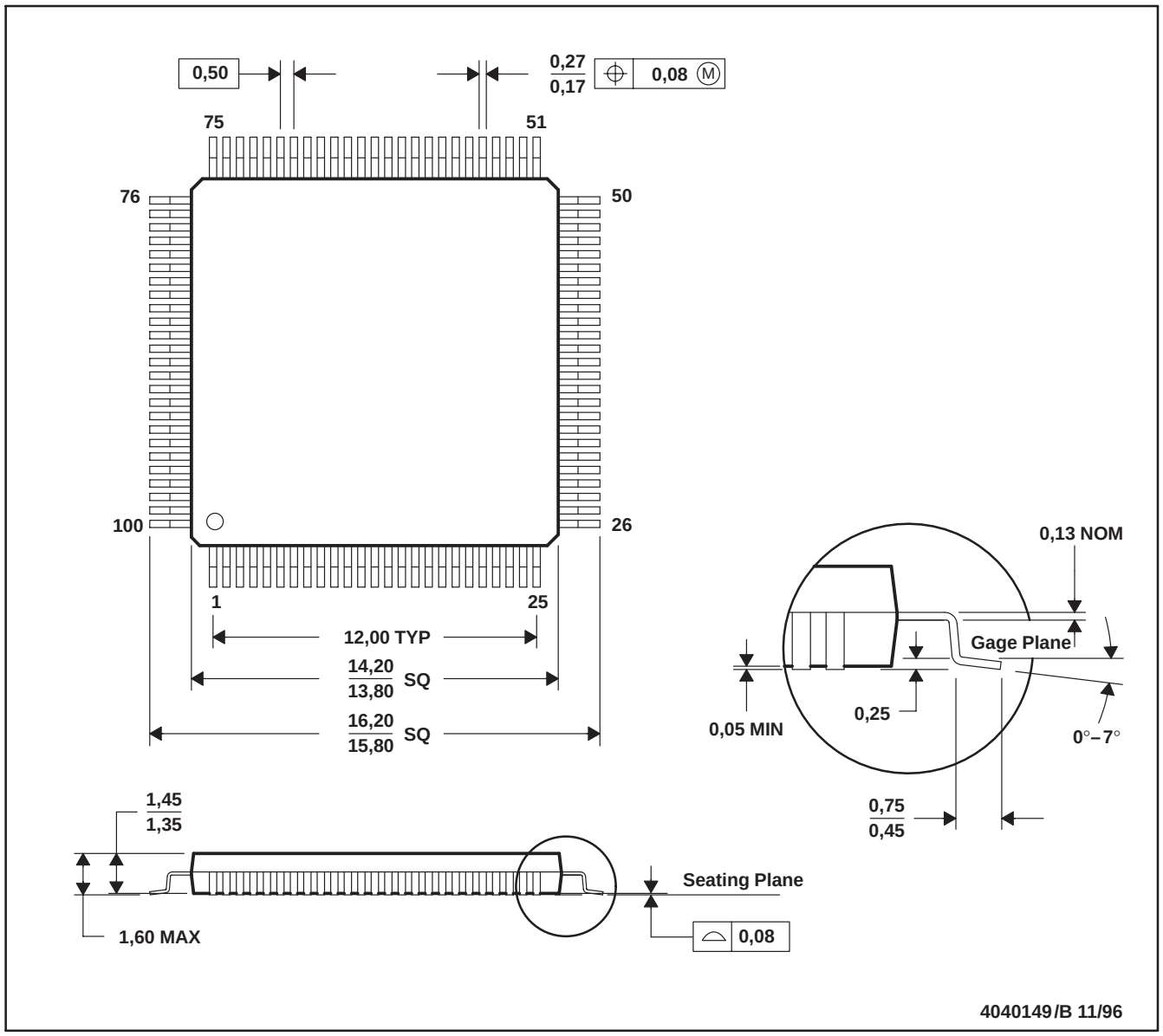
PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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