SY89112U

2.5V/3.3V Low-Jitter, Low-Skew 1:12 LVPECL Fanout Buffer with 2:1 MUX Input and Internal Termination

Features

- Selects Between 1 of 2 Inputs and Provides 12 Precision, Low-Skew LVPECL Output Copies
- Ensured AC Performance over Temperature and Voltage:
  - DC to >2 GHz Throughput
  - <550 ps Propagation Delay CLK-to-Q
  - <220 ps Rise/Fall Time
  - <25 ps Output-to-Output Skew
- Ultra-Low Jitter Design:
  - 50 fs_{RMS} Typical Phase Jitter
  - <0.7 ps_{RMS} Crosstalk-Induced Jitter
- Unique, Patent-Pending Input Termination and VT Pin Accepts DC-Coupled and AC-Coupled Differential Pins
- Unique, Patent-Pending 2:1 Input MUX Provides Superior Isolation to Minimize Channel-to-Channel Crosstalk
- 800 mV, 100K LVPECL Output Swing
- Power Supply: 2.5V ±5% or 3.3V ±10%
- Industrial Temperature Range: –40°C to +85°C
- Available in 44-Lead (7 mm x 7 mm) VQFN Package

Applications

- Multi-Processor Server
- SONET/SDH Clock/Data Distribution
- Fibre Channel Distribution
- Gigabit Ethernet Clock Distribution

General Description

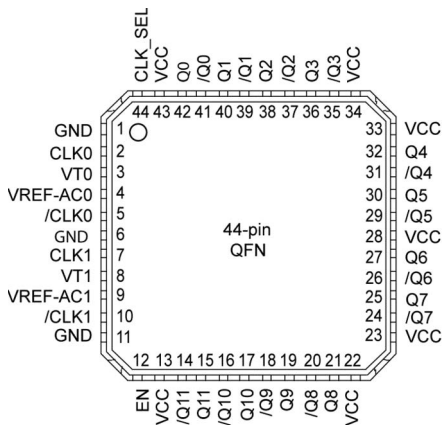
The SY89112U is a low-jitter, low-skew, high-speed LVPECL 1:12 differential fanout buffer optimized for precision telecom and enterprise server distribution applications. The input includes a 2:1 MUX for clock switchover applications. Unlike other multiplexers, this input includes a unique isolation design to minimize channel-to-channel crosstalk. The SY89112U distributes clock frequencies from DC to >2 GHz ensured over temperature and voltage. The SY89112U incorporates a synchronous output enable (EN) so that the outputs will only be enabled/disabled when they are already in the LOW state. This reduces the chance of generating “runt” clock pulses.

The SY89112U differential input includes Microchip’s unique, patent-pending 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100 mV (200 mV_{PP}) without any level shifting or termination resistor networks in the signal path. For AC-coupled input interface, an on-board output reference voltage (VREF-AC) is provided to bias the center-tap (VT) pin. The outputs are 800 mV, 100K compatible LVPECL with fast rise/fall times ensured to be less than 220 ps.

The SY89112U operates from a 2.5V ±5% or 3.3V ±10% supply and is ensured over the full industrial temperature range of –40°C to +85°C. The SY89112U is part of Microchip’s high-speed, Precision Edge® product line.

Package Type

SY89112U
44-Lead VQFN (M)
(Top View)



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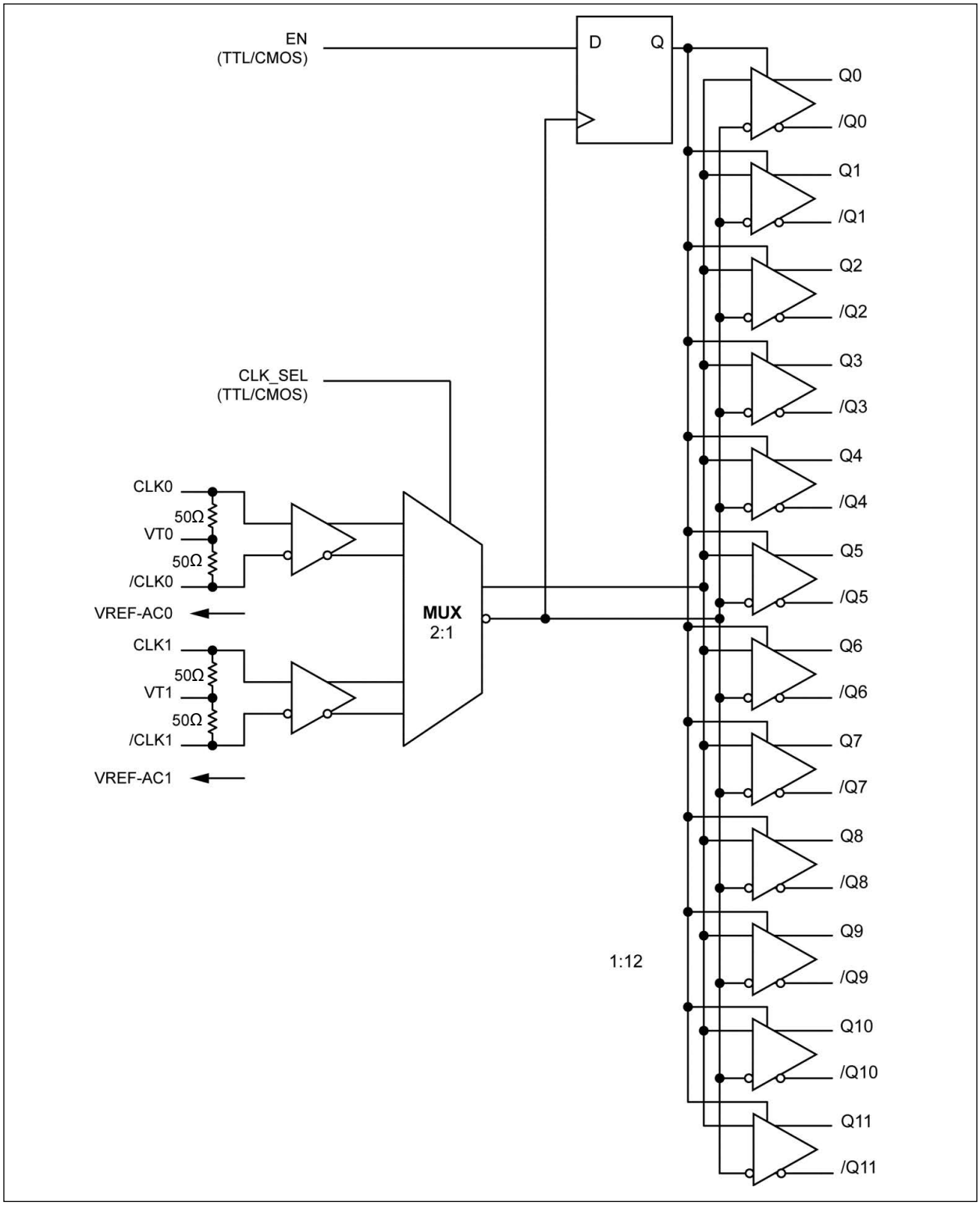
Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +4V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Continuous Output Current (I_{OUT}) ..... 50 mA
LVPECL Surge Output Current (I_{OUT}) ..... 100 mA
Source or Sink Current on VT Pin ..... ±100 mA
Source or Sink Current on CLK, /CLK ..... ±50 mA
Source or Sink Current on VREF-AC Pin ..... ±2 mA

Operating Ratings ‡

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
Supply Voltage (V_{CC}) ..... +3.0V to +3.6V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{CC}	2.375	—	2.625	V	—
		3.0	—	3.6		—
Power Supply Current	I_{CC}	—	95	130	mA	No load, V_{CC} = maximum
Input Resistance (CLK-to-VT)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (CLK-to-/CLK)	R_{DIFF_IN}	90	100	110	Ω	—
Input High Voltage (CLK-to-/CLK)	V_{IH}	1.2	—	V_{CC}	V	—
Input Low Voltage (CLK-to-/CLK)	V_{IL}	0	—	V_{IH} – 0.1	V	—
Input Voltage Swing (CLK-to-/CLK)	V_{IN}	0.1	—	1.7	V	See Figure 1-1
Differential Input Voltage Swing |CLK–/CLK|	V_{DIFF_IN}	0.2	—	—	V	See Figure 1-2
CLK-to-VT (/CLK-to-VT)	V_{T_IN}	—	—	1.28	V	—
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.3	V_{CC} – 1.2	V_{CC} – 1.1	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

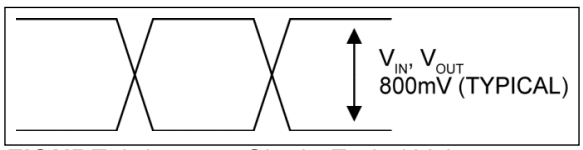

FIGURE 1-1: *Single-Ended Voltage Swing.*

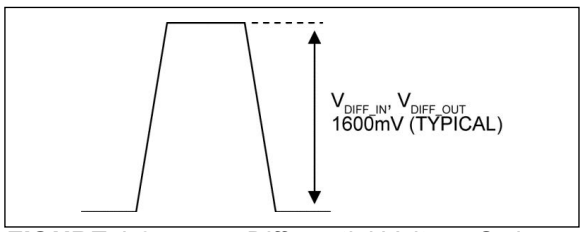

FIGURE 1-2: *Differential Voltage Swing.*

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LVPECL OUTPUTS DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC} − 2V; T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage (Q, /Q)	V_{OH}	V_{CC} – 1.145	—	V_{CC} – 0.895	V	—
Output Low Voltage (Q, /Q)	V_{OL}	V_{CC} – 1.945	—	V_{CC} – 1.695	V	—
Output Voltage Swing (Q, /Q)	V_{OUT}	550	800	—	mV	See Figure 1-1
Differential Output Voltage Swing (Q, /Q)	V_{DIFF_OUT}	1.1	1.6	—	V	See Figure 1-2

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input High Current	I_{IH}	–125	—	40	µA	—
Input Low Current	I_{IL}	–300	—	—	µA	—

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3 ±10%; R_L = 50Ω to V_{CC} − 2V; T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Operating Frequency	f_{MAX}	2	3	—	GHz	V_{OUT} ≥ 400 mV
Propagation Delay (CLK-to-Q)	t_{PD}	300	400	550	ps	V_{IN} ≥ 100 mV
Propagation Delay (CLK_SEL-to-Q)		200	350	600	ps	—
Differential Propagation Delay Temperature Coefficient	Δt_{PD}	—	150	—	fs/°C	—
Set-Up Time (EN-to-CLK)	t_S	0	—	—	ps	Note 2
Hold Time (CLK-to-EN)	t_H	500	—	—	ps	Note 2
Output-to-Output Skew	t_{SKEW}	—	—	25	ps	Note 3
Part-to-Part Skew		—	—	200	ps	Note 4
RMS Phase Jitter	t_{JITTER}	—	50	—	fs_{RMS}	Output = 622 MHz, Integration Range: 12 kHz to 20 MHz
Adjacent Channel Crosstalk-Induced Jitter		—	—	0.7	ps_{RMS}	Note 5
Output Rise/Fall Time (20% to 80%)	t_r,t_f	70	140	220	ps	At full output swing.

Note 1: High frequency AC parameters are ensured by design and characterization.

2: Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold do not apply.

3: Output-to-output skew is measured between two different outputs under identical transitions.

4: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

5: Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Package Thermal Resistances (Note 1)						
Thermal Resistance, VQFN 44-Ld	θ_{JA}	—	42	—	°C/W	Still-Air
	Ψ_{JB}	—	20	—	°C/W	Junction-to-Board

Note 1: Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} and θ_{JA} are shown for a 4-layer PCB in a still air environment, unless otherwise stated.

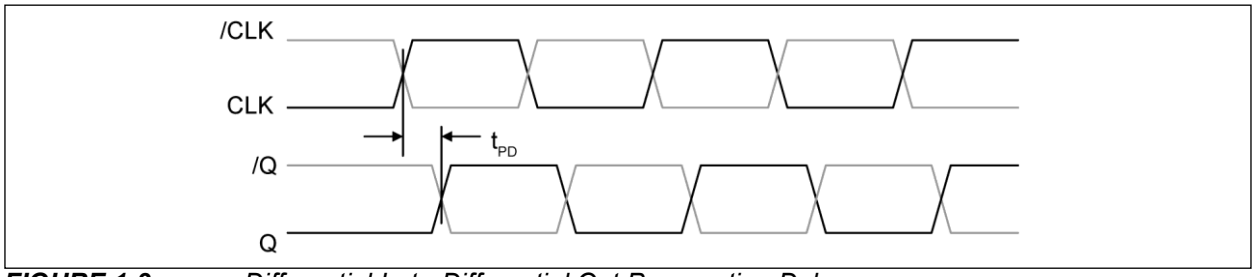

FIGURE 1-3: *Differential In-to-Differential Out Propagation Delay.*

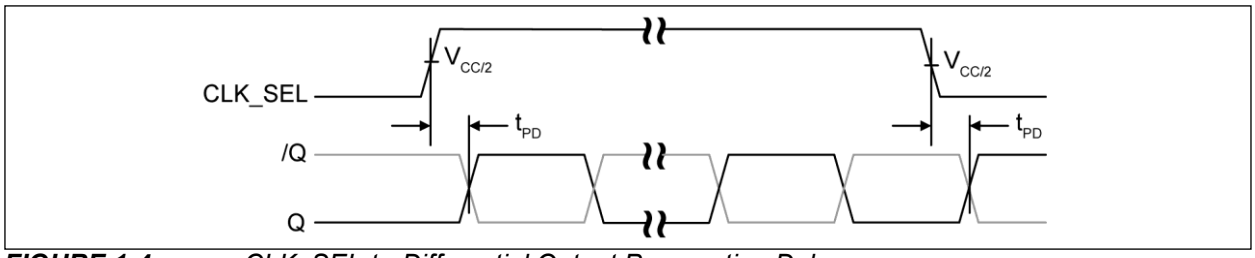

FIGURE 1-4: *CLK_SEL-to-Differential Output Propagation Delay.*

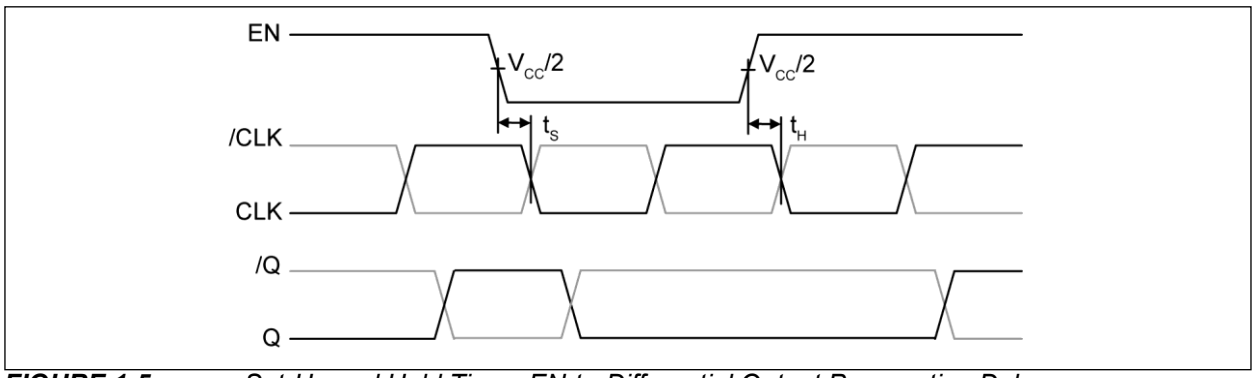

FIGURE 1-5: *Set-Up and Hold Times EN-to-Differential Output Propagation Delay.*

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 3.3V, GND = 0V, V_{IN} = 100 mV, R_L = 50Ω to V_{CC} – 2V, T_A = +25°C, unless otherwise stated.

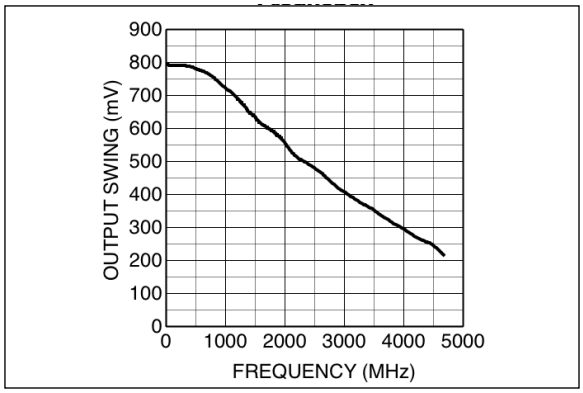

FIGURE 2-1: *Output Swing vs. Frequency.*

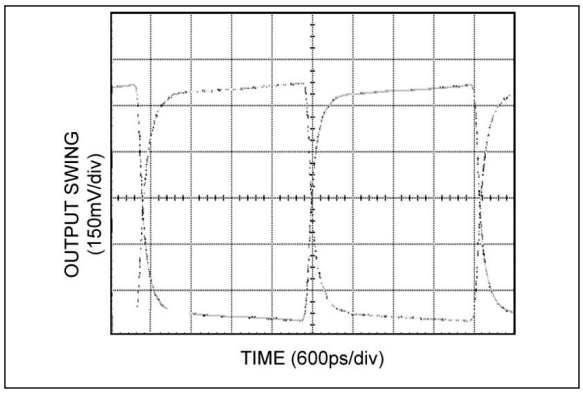

FIGURE 2-4: *200 MHz Output.*

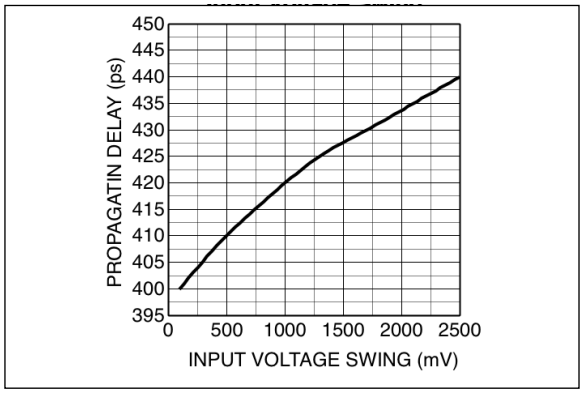

FIGURE 2-2: *Propagation Delay vs. Input Voltage Swing.*

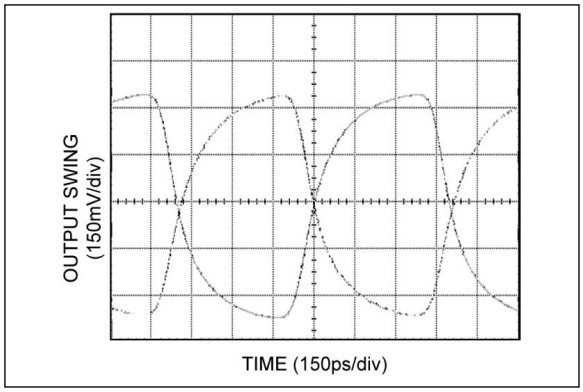

FIGURE 2-5: *1 GHz Output.*

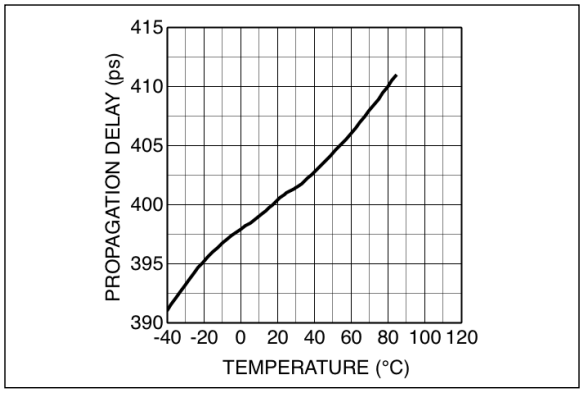

FIGURE 2-3: *Propagation Delay vs. Temperature.*

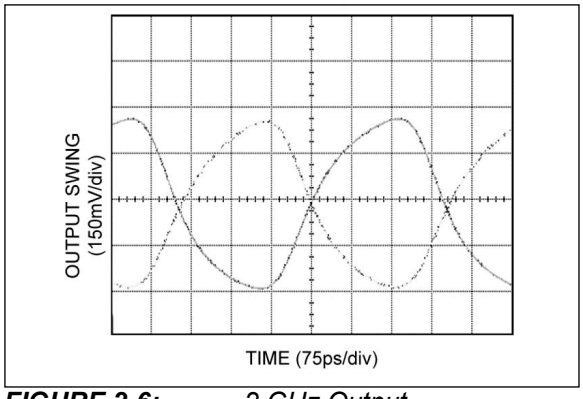

FIGURE 2-6: *2 GHz Output.*

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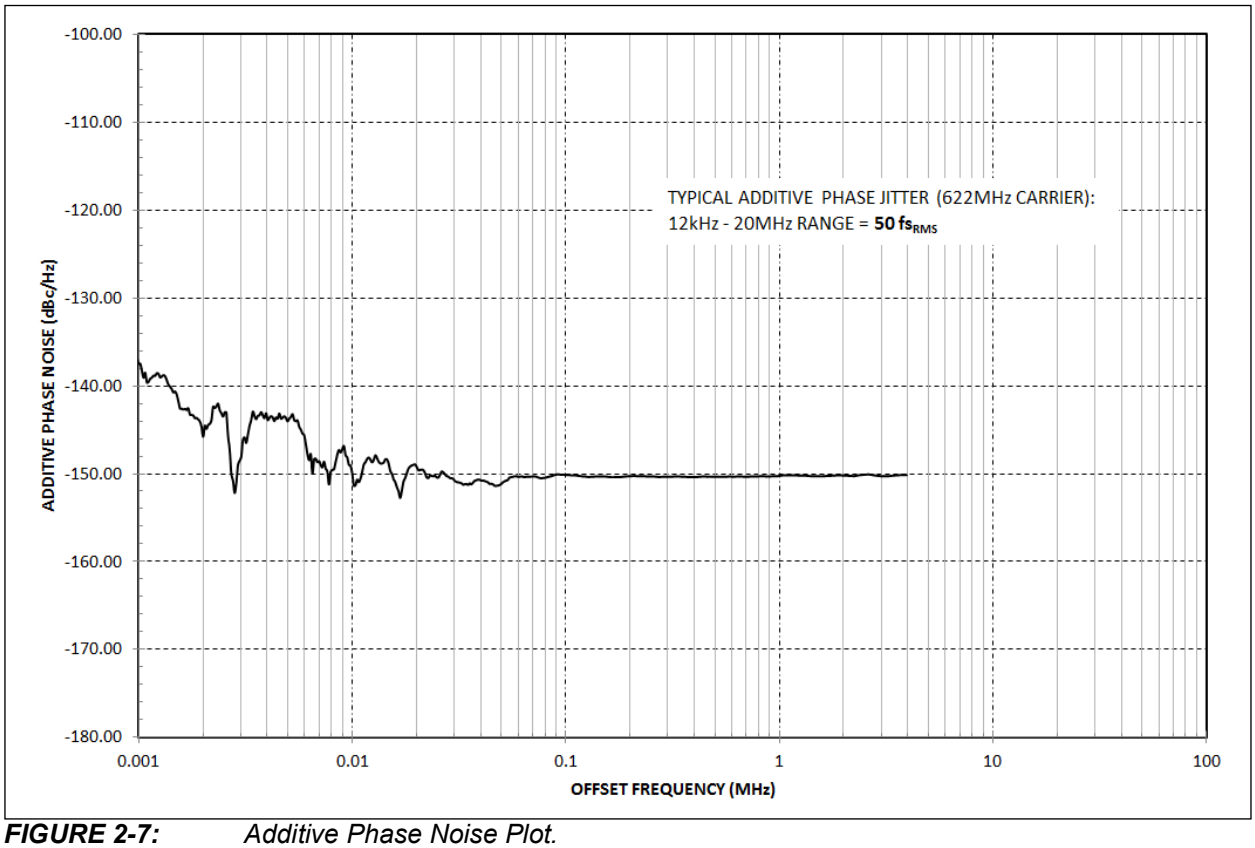

FIGURE 2-7: *Additive Phase Noise Plot.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
2, 5 7, 10	CLK0, /CLK0 CLK1, /CLK1	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled differential signals as small as 100 mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
3, 8	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
4, 9	VREF-AC0, VREF-AC1	Reference Voltage: These outputs bias to V_{CC} – 1.2V. They are used when AC-coupling the inputs (CLK, /CLK). For AC-coupled applications, connect VREF-AC to the VT pin and bypass with a 0.01 µF low ESR capacitor to VCC. See “Input Interface Applications” section for more details. Maximum sink/source current is ±1.5 mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
44	CLK_SEL	This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to a logic HIGH state if left open.
12	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
13, 22, 23, 28, 33, 34, 43	VCC	Positive power supply. Bypass with 0.1 µF//0.01 µF low-ESR capacitors and place as close to each VCC pin as possible.
42, 41 40, 39 38, 37 36, 35 32, 31 30, 29 27, 26 25, 24 21, 20 19, 18 17, 16 15, 14	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4 Q5, /Q5 Q6, /Q6 Q7, /Q7 Q8, /Q8 Q9, /Q9 Q10, /Q10 Q11, /Q11	Differential 100K LVPECL Outputs: These LVPECL outputs are the precision, low skew copies of the inputs. Please refer to the Truth Table below for details. Unused output pairs may be left open. Terminate with 50Ω to V_{CC} – 2V. See “LVPECL Output Interface Applications” section for more details.
1, 6, 11	GND, Exposed Pad	Ground. GND pins and exposed pad must both be connected to the most negative potential of chip the ground.

TABLE 3-2: TRUTH TABLE

EN	CLK_SEL	Q	/Q
H	L	CLK0	/CLK0
H	H	CLK1	/CLK1
L	X	L (Note 1)	H (Note 1)

Note 1: Transition occurs on the next negative transition of the non-inverted input.

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4.0 INPUT AND OUTPUT STAGES

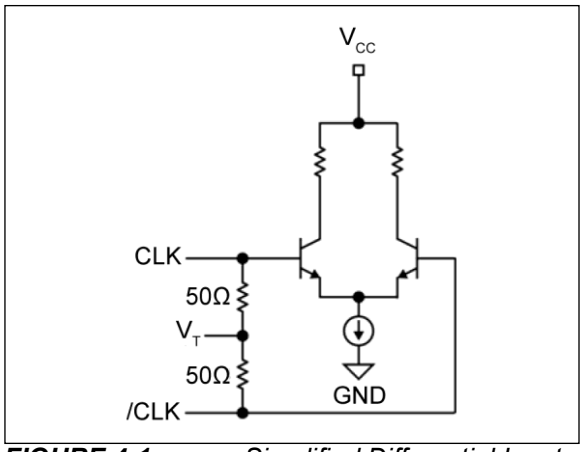

FIGURE 4-1: *Simplified Differential Input Stage.*

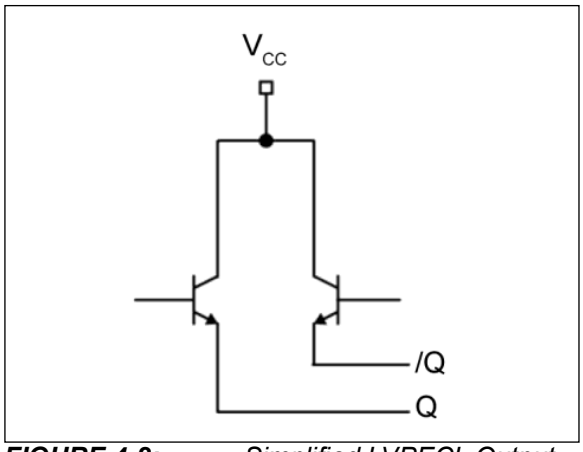

FIGURE 4-2: *Simplified LVPECL Output Stage.*

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5.0 INPUT INTERFACE APPLICATIONS

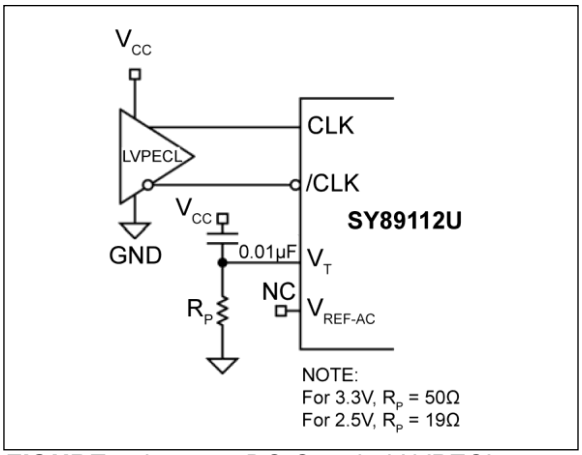

FIGURE 5-1: *DC-Coupled LVPECL Interface.*

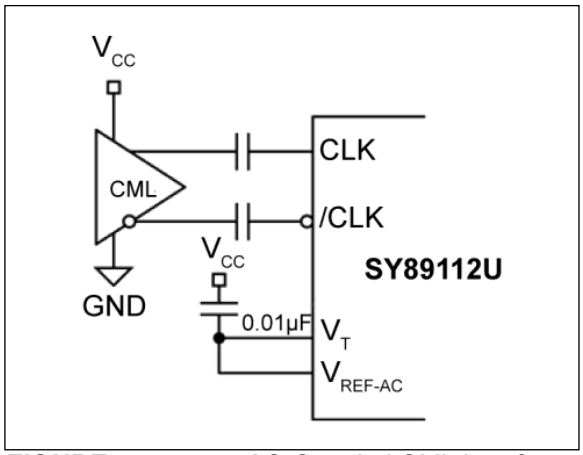

FIGURE 5-4: *AC-Coupled CML Interface.*

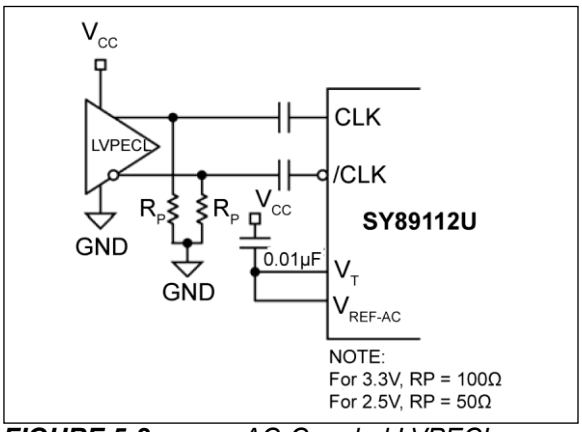

FIGURE 5-2: *AC-Coupled LVPECL Interface.*

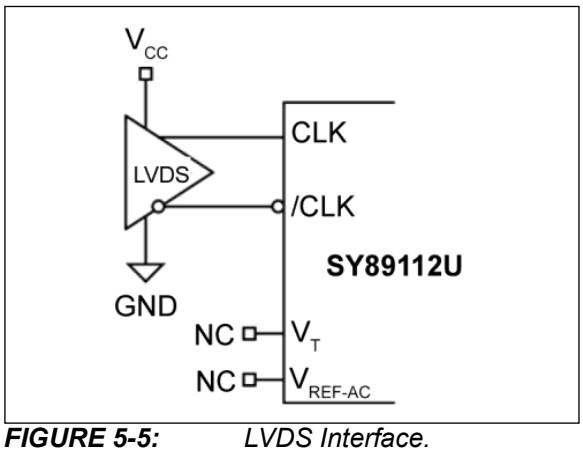

FIGURE 5-5: *LVDS Interface.*

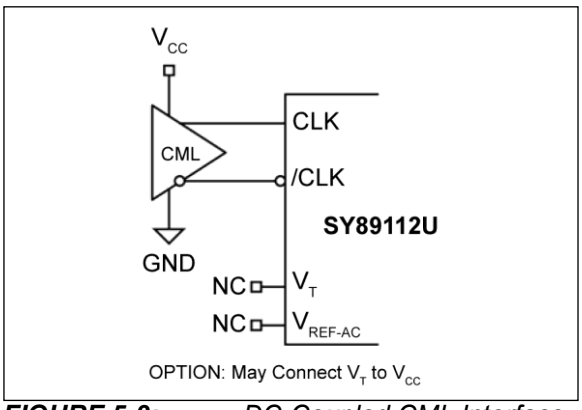

FIGURE 5-3: *DC-Coupled CML Interface.*

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6.0 LVPECL OUTPUT INTERFACE APPLICATIONS

LVPECL has high-input impedance, very-low output (open emitter) impedance, and small signal swing, which result in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques for terminating the LVPECL output: Parallel-Thevenin Equivalent, Parallel Termination (3-Resistor), and AC-Coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated or balanced.

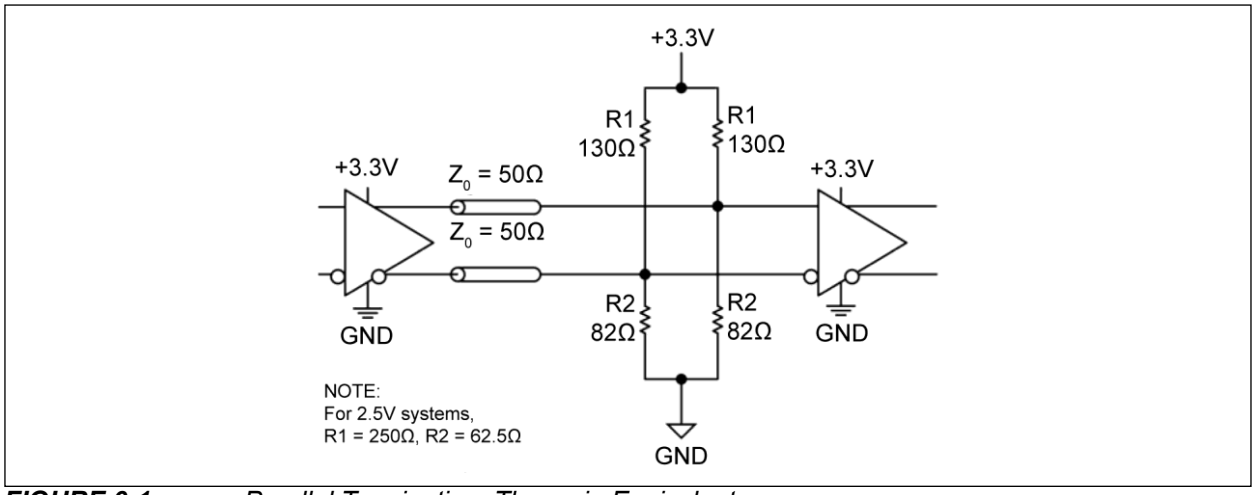

FIGURE 6-1: *Parallel Termination: Thevenin Equivalent.*

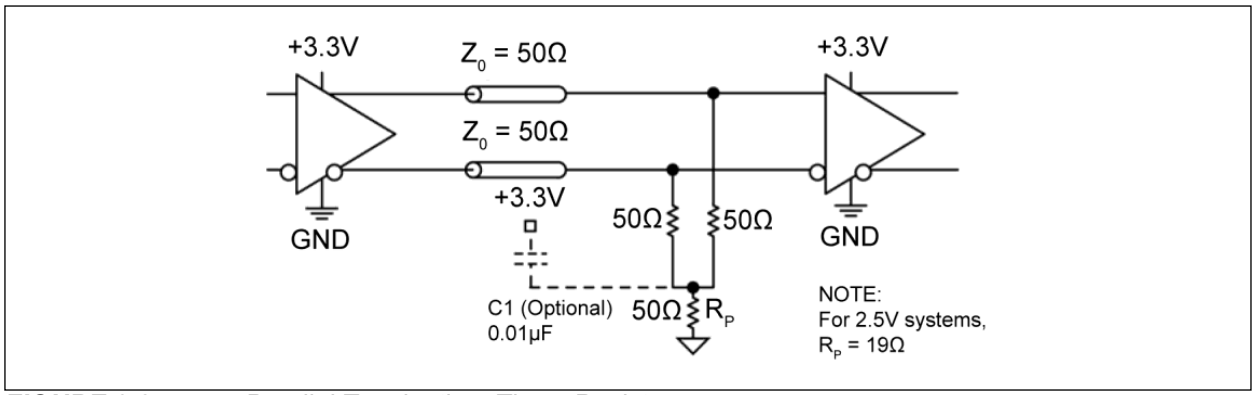

FIGURE 6-2: *Parallel Termination: Three-Resistor.*

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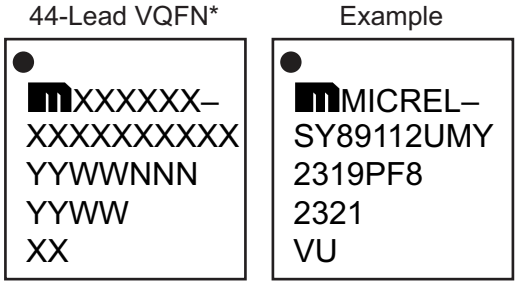
7.0 PACKAGING INFORMATION

7.1 Package Marking Information



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

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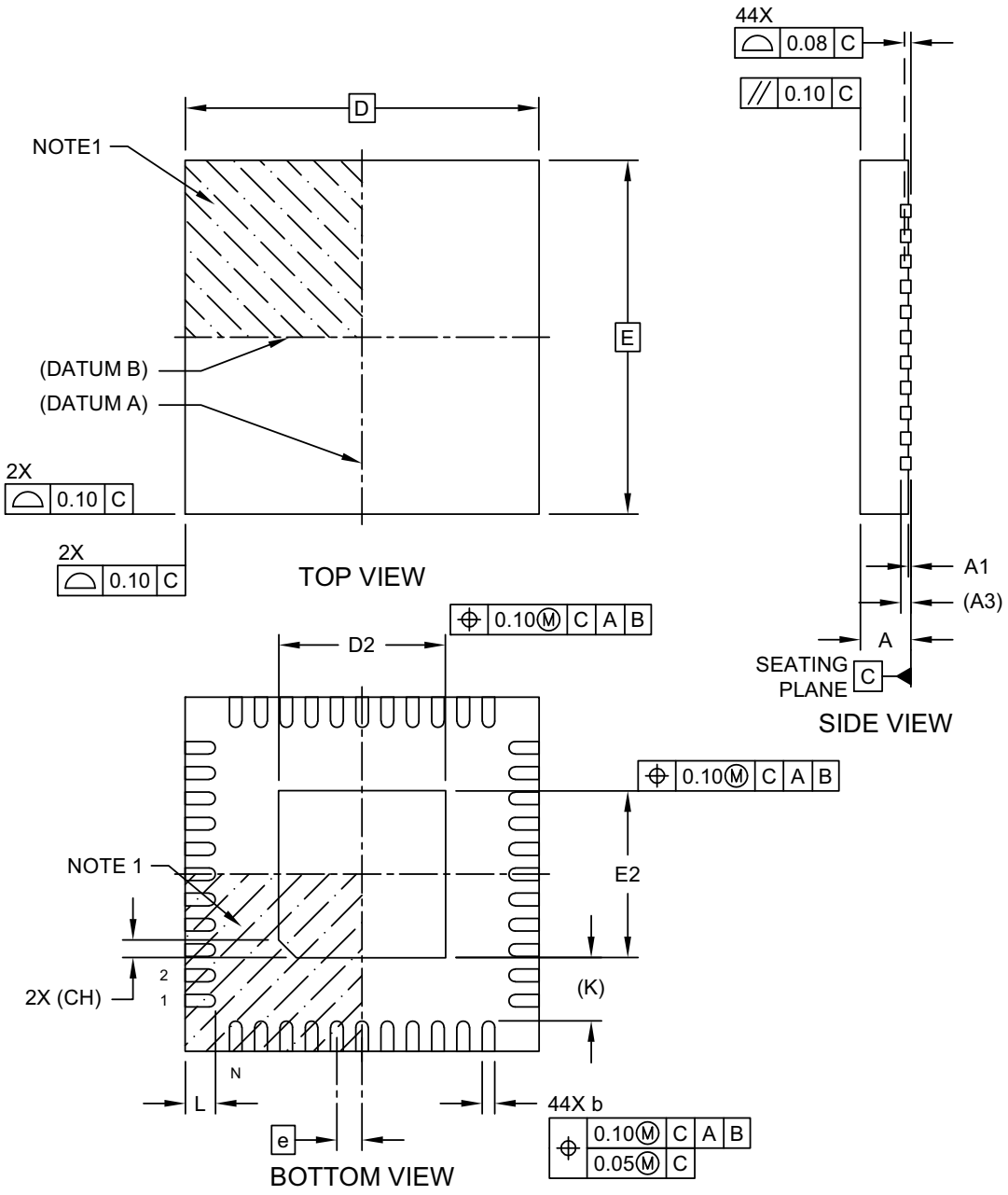
44-Lead Very Thin Quad Flat, No Lead Package (QPA) - 7x7x1.0 mm Body [VQFN]
With 3.3 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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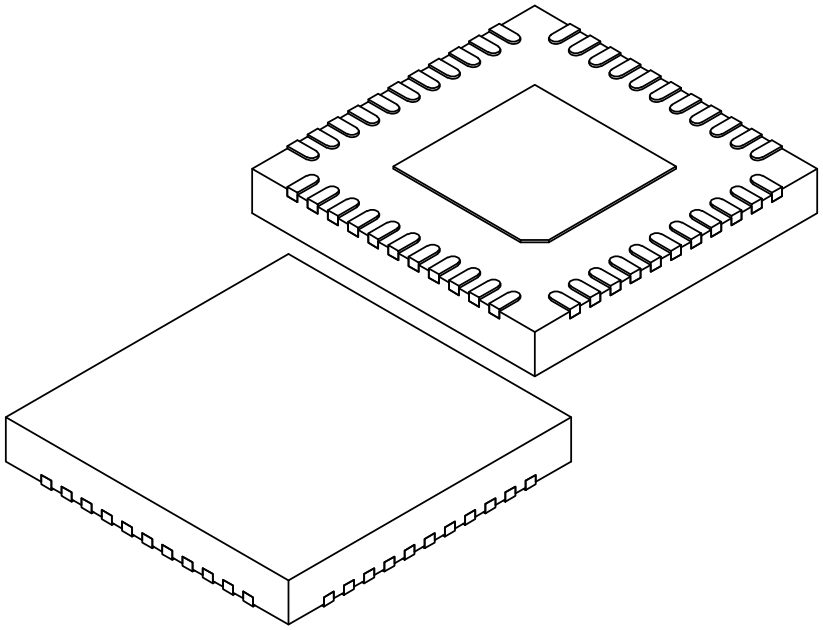
44-Lead Very Thin Quad Flat, No Lead Package (QPA) - 7x7x1.0 mm Body [VQFN] With 3.3 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		44	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	3.20	3.30	3.40
Overall Width	E		7.00 BSC	
Exposed Pad Width	E2	3.20	3.30	3.40
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K		0.20 REF	
Exposed Pad Corner Chamfer	CH		0.35 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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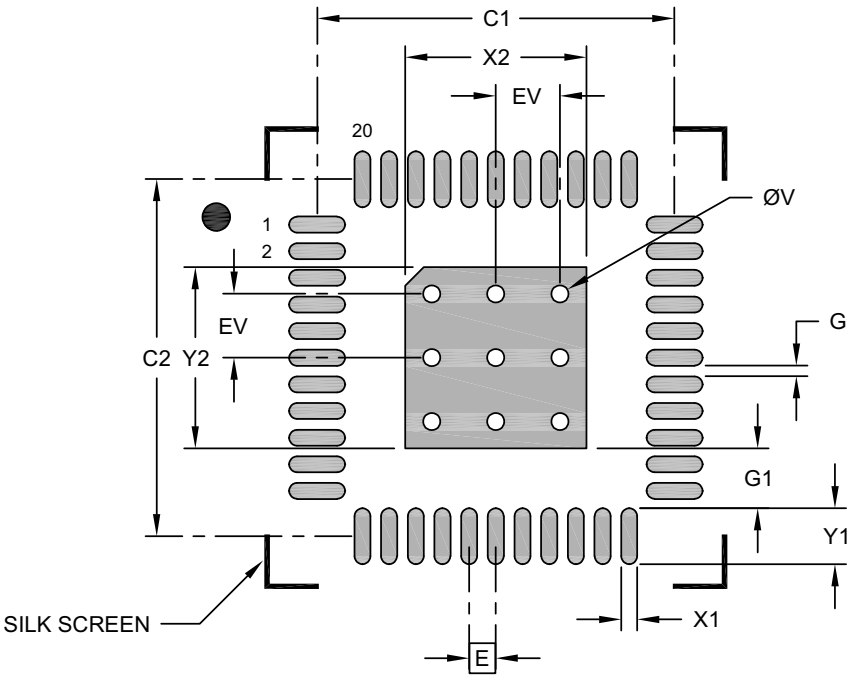
44-Lead Very Thin Quad Flat, No Lead Package (QPA) - 7x7x1.0 mm Body [VQFN] With 3.3 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			3.40
Center Pad Length	Y2			3.40
Contact Pad Spacing	C1		6.70	
Contact Pad Spacing	C2		6.70	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			1.05
Contact Pad to Center Pad (Xnn)	G1	1.13		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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APPENDIX A: REVISION HISTORY

Revision A (November 2023)

- Converted Micrel document SY89112U to Microchip data sheet template DS20006829A.
- Minor text changes throughout.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	X	[-XX]
Device	Supply Voltage	Package	Temperature Range	Media Type

Device:	SY89112:	2.5V/3.3V Low-Jitter, Low-Skew 1:12 LVPECL Fanout Buffer with 2:1 MUX Input and Internal Termination	
Supply Voltage:	U	=	2.5V/3.3V
Package:	M	=	44-Lead 7 mm x 7 mm VQFN
Temperature Range:	Y	=	–40°C to +85°C
Media Type:	<blank>	=	260/Tray
	TR	=	1,000/Reel

Examples:

a) SY89112UMY:

SY89112, 2.5V/3.3V Supply Voltage, 44-Lead VQFN, –40°C to +85°C Temperature Range, 260/Tray

b) SY89112UMY-TR:

SY89112, 2.5V/3.3V Supply Voltage, 44-Lead VQFN, –40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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