

256K SPI Bus Low-Power Serial SRAM

Device Selection Table

| Part Number | Vcc Range | Page Size | Temp. Ranges | Packages |
|-------------|-----------|-----------|--------------|-----------|
| 23K256 | 2.7-3.6V | 32 Byte | I, E | P, SN, ST |
| 23A256 | 1.5-1.95V | 32 Byte | I | P, SN, ST |

Features:

- Max. Clock 20 MHz
- Low-Power CMOS Technology:
 - Read Current: 3 mA at 1 MHz
 - Standby Current: 4 μ A Max. at +85°C
- 32,768 x 8-bit Organization
- 32-Byte Page
- $\overline{\text{HOLD}}$ pin
- Flexible Operating modes:
 - Byte read and write
 - Page mode (32 Byte Page)
 - Sequential mode
- Sequential Read/Write
- High Reliability
- Temperature Ranges Supported:
 - Industrial (I): -40°C to +85°C
 - Automotive (E): -40°C to +125°C
- Pb-Free and RoHS Compliant, Halogen Free

Pin Function Table

| Name | Function |
|--------------------------|--------------------|
| $\overline{\text{CS}}$ | Chip Select Input |
| SO | Serial Data Output |
| Vss | Ground |
| SI | Serial Data Input |
| SCK | Serial Clock Input |
| $\overline{\text{HOLD}}$ | Hold Input |
| Vcc | Supply Voltage |

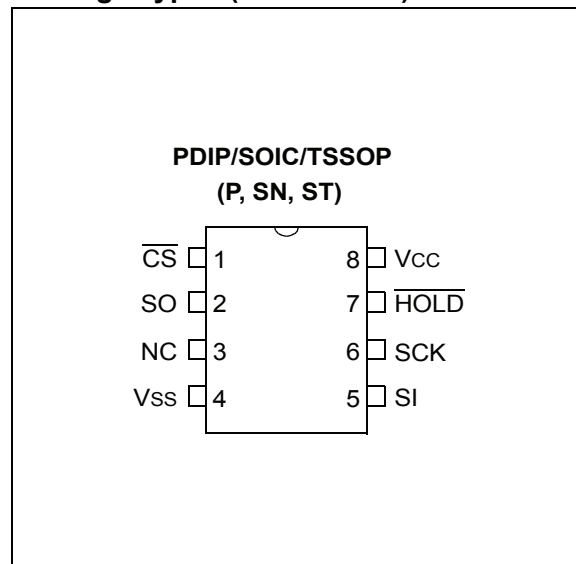
Description:

The Microchip Technology Inc. 23X256 are 256 Kbit Serial SRAM devices. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{\text{CS}}$) input.

Communication to the device can be paused via the hold pin ($\overline{\text{HOLD}}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 23X256 is available in standard packages including 8-lead PDIP and SOIC, and advanced packaging including 8-lead TSSOP.

Package Types (not to scale)



23A256/23K256

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

| | |
|---|--------------------------------|
| V _{CC} | 4.5V |
| All inputs and outputs w.r.t. V _{SS} | -0.3V to V _{CC} +0.3V |
| Storage temperature | -65°C to 150°C |
| Ambient temperature under bias | -40°C to 125°C |
| ESD protection on all pins | 2kV |

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

| DC CHARACTERISTICS | | | Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C | | | | |
|--------------------|----------------------|---|---|--------------------|---|----------------|---|
| Param. No. | Sym. | Characteristic | Min. | Typ ⁽¹⁾ | Max. | Units | Test Conditions |
| D001 | V _{CC} | Supply voltage | 1.5 | — | 1.95 | V | 23A256 (I-Temp) |
| D001 | V _{CC} | Supply voltage | 2.7 | — | 3.6 | V | 23K256 (I,E-Temp) |
| D002 | V _{IH} | High-level input voltage | .7 V _{CC} | — | V _{CC} +0.3 | V | |
| D003 | V _{IL} | Low-level input voltage | -0.3 | — | 0.2xV _{CC} 0.15xV _{CC} | V V | 23K256 (E-Temp) |
| D004 | V _{OL} | Low-level output voltage | — | — | 0.2 | V | I _{OL} = 1 mA |
| D005 | V _{OH} | High-level output voltage | V _{CC} -0.5 | — | — | V | I _{OH} = -400 μA |
| D006 | I _{LI} | Input leakage current | — | — | ±0.5 | μA | $\overline{CS} = V_{CC}, V_{IN} = V_{SS} \text{ OR } V_{CC}$ |
| D007 | I _{LO} | Output leakage current | — | — | ±0.5 | μA | $\overline{CS} = V_{CC}, V_{OUT} = V_{SS} \text{ OR } V_{CC}$ |
| D008 | I _{CC Read} | Operating current | — | — | 3 6 10 | mA mA mA | F _{CLK} = 1 MHz; SO = 0 F _{CLK} = 10 MHz; SO = 0 F _{CLK} = 20 MHz; SO = 0 |
| D009 | I _{CCS} | Standby current | — | 0.2 1 5 | 1 4 10 | μA μA μA | $\overline{CS} = V_{CC} = 1.8V$, Inputs tied to V _{CC} or V _{SS} $\overline{CS} = V_{CC} = 3.6V$, Inputs tied to V _{CC} or V _{SS} $\overline{CS} = V_{CC} = 3.6V$, Inputs tied to V _{CC} or V _{SS} @ 125°C |
| D010 | C _{INT} | Input capacitance | | | 7 | pF | V _{CC} = 0V, f = 1 MHz, T _a = 25°C (Note 1) |
| D011 | V _{DR} | RAM data retention voltage ⁽²⁾ | — | 1.2 | — | V | |

Note 1: This parameter is periodically sampled and not 100% tested. Typical measurements taken at room temperature (25°C).

2: This is the limit to which V_{DD} can be lowered without losing RAM data. This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

| AC CHARACTERISTICS | | | Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C | | | |
|--------------------|------|-----------------------------|---|------|-------|---------------------|
| Param. No. | Sym. | Characteristic | Min. | Max. | Units | Test Conditions |
| 1 | FCLK | Clock frequency | — | 10 | MHz | VCC = 1.5V (I-Temp) |
| | | | — | 16 | MHz | VCC = 1.8V (I-Temp) |
| | | | — | 16 | MHz | VCC = 3.0V (E-Temp) |
| | | | — | 20 | MHz | VCC = 3.0V (I-Temp) |
| 2 | Tcss | CS setup time | 50 | — | ns | VCC = 1.5V (I-Temp) |
| | | | 32 | — | ns | VCC = 1.8V (I-Temp) |
| | | | 32 | — | ns | VCC = 3.0V (E-Temp) |
| | | | 25 | — | ns | VCC = 3.0V (I-Temp) |
| 3 | Tcsh | CS hold time | 50 | — | ns | VCC = 1.5V (I-Temp) |
| | | | 50 | — | ns | VCC = 1.8V (I-Temp) |
| | | | 50 | — | ns | VCC = 3.0V (E-Temp) |
| | | | 50 | — | ns | VCC = 3.0V (I-Temp) |
| 4 | TcSD | CS disable time | 50 | — | ns | VCC = 1.5V (I-Temp) |
| | | | 32 | — | ns | VCC = 1.8V (I-Temp) |
| | | | 32 | — | ns | VCC = 3.0V (E-Temp) |
| | | | 25 | — | ns | VCC = 3.0V (I-Temp) |
| 5 | Tsu | Data setup time | 10 | — | ns | VCC = 1.5V (I-Temp) |
| | | | 10 | — | ns | VCC = 1.8V (I-Temp) |
| | | | 10 | — | ns | VCC = 3.0V (E-Temp) |
| | | | 10 | — | ns | VCC = 3.0V (I-Temp) |
| 6 | THD | Data hold time | 10 | — | ns | VCC = 1.5V (I-Temp) |
| | | | 10 | — | ns | VCC = 1.8V (I-Temp) |
| | | | 10 | — | ns | VCC = 3.0V (E-Temp) |
| | | | 10 | — | ns | VCC = 3.0V (I-Temp) |
| 7 | TR | CLK rise time | — | 2 | us | Note 1 |
| 8 | TF | CLK fall time | — | 2 | us | Note 1 |
| 9 | THI | Clock high time | 50 | — | ns | VCC = 1.5V (I-Temp) |
| | | | 32 | — | ns | VCC = 1.8V (I-Temp) |
| | | | 32 | — | ns | VCC = 3.0V (E-Temp) |
| | | | 25 | — | ns | VCC = 3.0V (I-Temp) |
| 10 | TLO | Clock low time | 50 | — | ns | VCC = 1.5V (I-Temp) |
| | | | 32 | — | ns | VCC = 1.8V (I-Temp) |
| | | | 32 | — | ns | VCC = 3.0V (E-Temp) |
| | | | 25 | — | ns | VCC = 3.0V (I-Temp) |
| 11 | TCLD | Clock delay time | 50 | — | ns | VCC = 1.5V (I-Temp) |
| | | | 32 | — | ns | VCC = 1.8V (I-Temp) |
| | | | 32 | — | ns | VCC = 3.0V (E-Temp) |
| | | | 25 | — | ns | VCC = 3.0V (I-Temp) |
| 12 | TV | Output valid from clock low | — | 50 | ns | VCC = 1.5V (I-Temp) |
| | | | — | 32 | ns | VCC = 1.8V (I-Temp) |
| | | | — | 32 | ns | VCC = 3.0V (E-Temp) |
| | | | — | 25 | ns | VCC = 3.0V (I-Temp) |
| 13 | THO | Output hold time | 0 | — | ns | Note 1 |

Note 1: This parameter is periodically sampled and not 100% tested.

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TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

| AC CHARACTERISTICS | | | Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C | | | |
|--------------------|------|---|---|------|-------|---------------------|
| Param. No. | Sym. | Characteristic | Min. | Max. | Units | Test Conditions |
| 14 | TDIS | Output disable time | — | 20 | ns | VCC = 1.5V (I-Temp) |
| | | | — | 20 | ns | VCC = 1.8V (I-Temp) |
| | | | — | 20 | ns | VCC = 3.0V (E-Temp) |
| | | | — | 20 | ns | VCC = 3.0V (I-Temp) |
| 15 | THS | $\overline{\text{HOLD}}$ setup time | 10 | — | ns | — |
| 16 | THH | $\overline{\text{HOLD}}$ hold time | 10 | — | ns | — |
| 17 | THZ | $\overline{\text{HOLD}}$ low to output High-Z | 10 | — | ns | — |
| 18 | THV | $\overline{\text{HOLD}}$ high to output valid | — | 50 | ns | — |

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC TEST CONDITIONS

| AC Waveform: | |
|-------------------------------------|--------------------|
| Input pulse level | 0.1 VCC to 0.9 VCC |
| Input rise/fall time | 5 ns |
| Operating temperature | -40°C to +125°C |
| CL = 100 pF | — |
| Timing Measurement Reference Level: | |
| Input | 0.5 VCC |
| Output | 0.5 VCC |

FIGURE 1-1: HOLD TIMING



FIGURE 1-2: SERIAL INPUT TIMING



FIGURE 1-3: SERIAL OUTPUT TIMING



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2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 23X256 is a 32,768-byte Serial SRAM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 23X256 contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{\text{CS}}$ pin must be low and the HOLD pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{\text{CS}}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input and place the 23X256 in 'HOLD' mode. After releasing the HOLD pin, operation will resume from the point when the HOLD was asserted.

2.2 Modes of Operation

The 23A256/23K256 has three modes of operation that are selected by setting bits 7 and 6 in the STATUS register. The modes of operation are Byte, Page and Burst.

Byte Operation – is selected when bits 7 and 6 in the STATUS register are set to 00. In this mode, the read/write operations are limited to only one byte. The Command followed by the 16-bit address is clocked into the device and the data to/from the device is transferred on the next 8 clocks (Figure 2-1, Figure 2-2).

Page Operation – is selected when bits 7 and 6 in the STATUS register are set to 10. The 23A256/23K256 has 1024 pages of 32 Bytes. In this mode, the read and write operations are limited to within the addressed page (the address is automatically incremented internally). If the data being read or written reaches the page boundary, then the internal address counter will increment to the start of the page (Figure 2-3, Figure 2-4).

Sequential Operation – is selected when bits 7 and 6 in the STATUS register are set to 01. Sequential operation allows the entire array to be written to and read from. The internal address counter is automatically incremented and page boundaries are ignored. When the internal address counter reaches the end of the array, the address counter will roll over to 0x0000 (Figure 2-5, Figure 2-6).

2.3 Read Sequence

The device is selected by pulling $\overline{\text{CS}}$ low. The 8-bit READ instruction is transmitted to the 23X256 followed by the 16-bit address, with the first MSB of the address being a "don't care" bit. After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin.

If operating in Page mode, after the first byte of data is shifted out, the next memory location on the page can be read out by continuing to provide clock pulses. This allows for 32 consecutive address reads. After the 32nd address read the internal address counter wraps back to the byte 0 address in that page.

If operating in Sequential mode, the data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (7FFFh), the address counter rolls over to address 0000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{\text{CS}}$ pin (Figure 2-1).

2.4 Write Sequence

Prior to any attempt to write data to the 23X256, the device must be selected by bringing $\overline{\text{CS}}$ low.

Once the device is selected, the Write command can be started by issuing a WRITE instruction, followed by the 16-bit address, with the first MSB of the address being a "don't care" bit, and then the data to be written. A write is terminated by the $\overline{\text{CS}}$ being brought high.

If operating in Page mode, after the initial data byte is shifted in, additional bytes can be shifted into the device. The Address Pointer is automatically incremented. This operation can continue for the entire page (32 Bytes) before data will start to be overwritten.

If operating in Sequential mode, after the initial data byte is shifted in, additional bytes can be clocked into the device. The internal Address Pointer is automatically incremented. When the Address Pointer reaches the highest address (7FFFh), the address counter rolls over to (0000h). This allows the operation to continue indefinitely, however, previous data will be overwritten.

TABLE 2-1: INSTRUCTION SET

| Instruction Name | Instruction Format | Description |
|------------------|--------------------|---|
| READ | 0000 0011 | Read data from memory array beginning at selected address |
| WRITE | 0000 0010 | Write data to memory array beginning at selected address |
| RDSR | 0000 0101 | Read STATUS register |
| WRSR | 0000 0001 | Write STATUS register |

FIGURE 2-1: BYTE READ SEQUENCE



FIGURE 2-2: BYTE WRITE SEQUENCE



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FIGURE 2-3: PAGE READ SEQUENCE

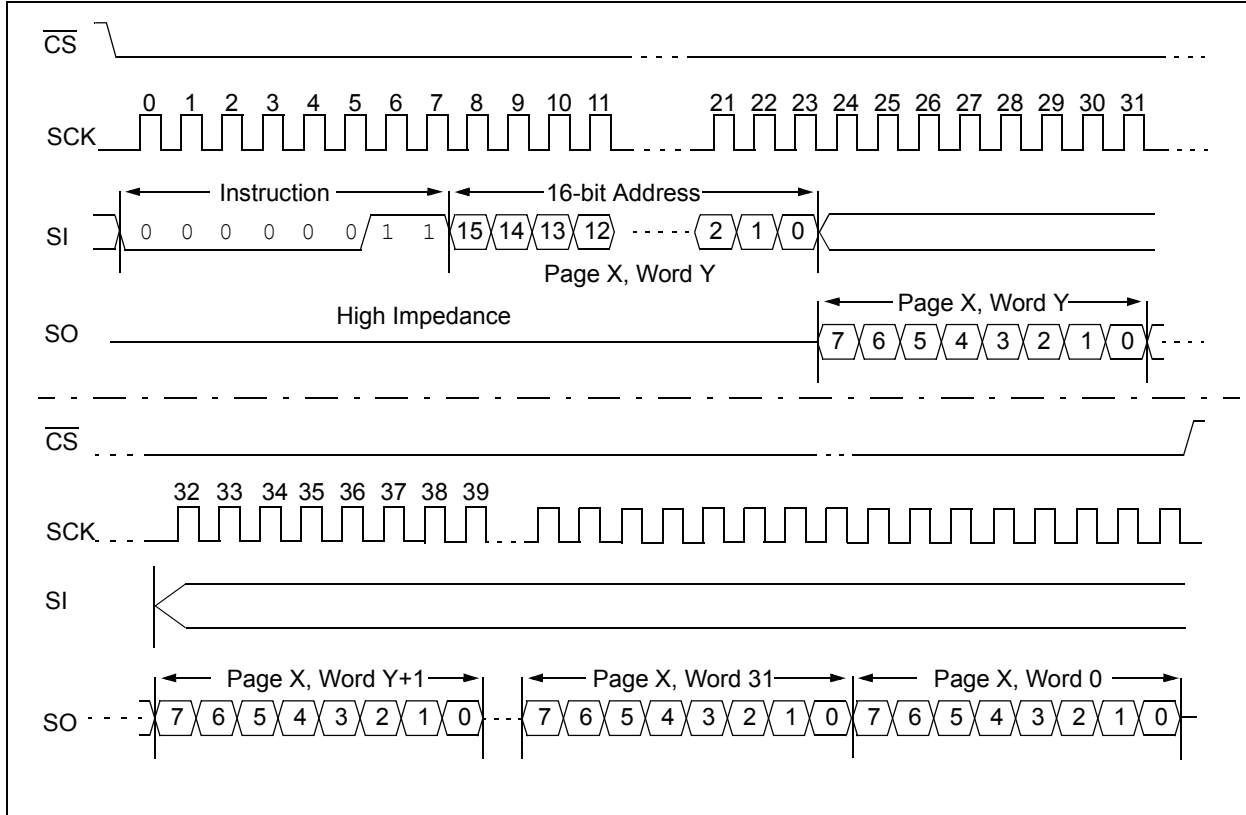


FIGURE 2-4: PAGE WRITE SEQUENCE

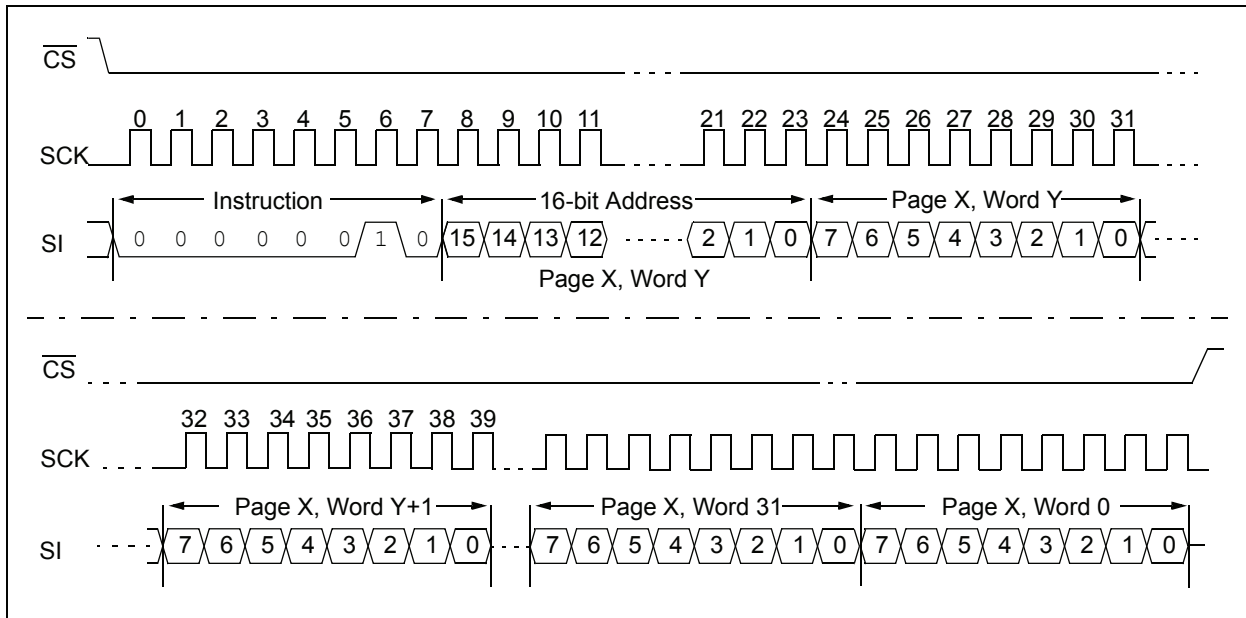


FIGURE 2-5: SEQUENTIAL READ SEQUENCE



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FIGURE 2-6: SEQUENTIAL WRITE SEQUENCE



2.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. The STATUS register may be read at any time. The STATUS register is formatted as follows:

TABLE 2-2: STATUS REGISTER

| | | | | | | | |
|------|------|---|---|---|---|---|------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| W/R | W/R | - | - | - | - | - | W/R |
| MODE | MODE | 0 | 0 | 0 | 0 | 0 | HOLD |

W/R = writable/readable.

The mode bits indicate the operating mode of the SRAM. The possible modes of operation are:

- 0 0 = Byte mode (default operation)
- 1 0 = Page mode
- 0 1 = Sequential mode
- 1 1 = Reserved

Write and read commands are shown in [Figure 2-7](#) and [Figure 2-8](#).

The HOLD bit enables the Hold pin functionality. It must be set to a '0' before HOLD pin is brought low for HOLD function to work properly. Setting HOLD to '1' disables feature.

Bits 1 through 5 are reserved and should always be set to '0'.

See [Figure 2-7](#) for the RDSR timing sequence.

FIGURE 2-7: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



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2.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the bits in the STATUS register as shown in Table 2-2. This allows for setting of the Device operating mode. Several of the bits in the STATUS register must be cleared to '0'. See Figure 2-8 for the WRSR timing sequence.

FIGURE 2-8: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



2.7 Power-On State

The 23X256 powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS} = 1$)
- A high-to-low-level transition on \overline{CS} is required to enter active state

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

| Name | PDIP/SOIC TSSOP | Function |
|--------------------------|--------------------|--------------------|
| $\overline{\text{CS}}$ | 1 | Chip Select Input |
| SO | 2 | Serial Data Output |
| Vss | 4 | Ground |
| SI | 5 | Serial Data Input |
| SCK | 6 | Serial Clock Input |
| $\overline{\text{HOLD}}$ | 7 | Hold Input |
| Vcc | 8 | Supply Voltage |

3.1 Chip Select ($\overline{\text{CS}}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. After power-up, a low level on $\overline{\text{CS}}$ is required, prior to any sequence being initiated.

3.2 Serial Output (SO)

The SO pin is used to transfer data out of the 23X256. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.3 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

3.4 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 23X256. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

3.5 Hold ($\overline{\text{HOLD}}$)

The $\overline{\text{HOLD}}$ pin is used to suspend transmission to the 23X256 while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{\text{HOLD}}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{\text{HOLD}}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 23X256 must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{\text{HOLD}}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

Hold functionality is disabled by the STATUS register bit.

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4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead PDIP



Example:



8-Lead SOIC (3.90 mm)



Example:




8-Lead TSSOP



Example:



| | | |
|----------------|---|--|
| Legend: | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| |  | Pb-free JEDEC designator for Matte Tin (Sn) |

Note: For very small packages with no room for the Pb-free JEDEC designator , the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | INCHES | | |
|----------------------------|-------|----------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

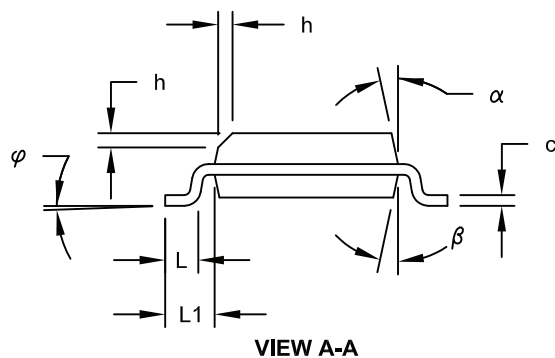
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

23A256/23K256

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 4.90 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|----------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | MILLIMETERS | | |
|--------------------------|--------|-------|-------------|------|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | | |
| Pitch | e | | 0.65 BSC | | |
| Overall Height | A | – | – | – | 1.20 |
| Molded Package Thickness | A2 | | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | | 0.05 | – | 0.15 |
| Overall Width | E | | 6.40 BSC | | |
| Molded Package Width | E1 | | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | | 2.90 | 3.00 | 3.10 |
| Foot Length | L | | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | | |
| Foot Angle | ϕ | | 0° | – | 8° |
| Lead Thickness | c | | 0.09 | – | 0.20 |
| Lead Width | b | | 0.19 | – | 0.30 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

23A256/23K256

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C1 | | 5.90 | |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.45 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension, Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

APPENDIX A: REVISION HISTORY

Revision A (11/2008)

Original Release.

Revision B (12/2008)

Updates; Table 1-1, add Param. D011.

Revision C (01/2009)

Revised Section 2.5: Added a paragraph.

Revision D (04/2009)

Removed Preliminary status; Revised Standby Current; Revised Table 1-1, Param. No. D009; Revised TSSOP Package marking; Revised Product ID.

Revision E (08/2010)

Revised Table 1-1, Param. No. D009; Revised Package Drawings.

Revision F (10/2011)

Revised Parameter D003 in Table 1-1: DC Characteristics.

23A256/23K256

NOTES:

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Device: 23X256

Literature Number: DS22100F

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| <u>PART NO.</u> | | <u>X</u> | - | <u>X</u> | <u>/XX</u> |
|---------------------------|-------------|--------------------------------------|---|----------|------------|
| Device | Tape & Reel | Temp Range | | Package | |
| Device: | 23A256 = | 256 Kbit, 1.8V, SPI Serial SRAM | | | |
| | 23K256 = | 256 Kbit, 3.6V, SPI Serial SRAM | | | |
| Tape & Reel: | Blank = | Standard packaging (tube) | | | |
| | T = | Tape & Reel | | | |
| Temperature Range: | I = | -40°C to+85°C | | | |
| | E = | -40°C to+125°C | | | |
| Package: | P = | Plastic PDIP (300 mil body), 8-lead | | | |
| | SN = | Plastic SOIC (3.90 mml body), 8-lead | | | |
| | ST = | TSSOP, 8-lead | | | |

Examples:

- a) 23K256-I/ST = 256 Kbit, 3.6V Serial SRAM, Industrial temp., TSSOP package
- b) 23A256T-I/SN = 256 Kbit, 1.8V Serial SRAM, Industrial temp., Tape & Reel, SOIC package
- c) 23K256-E/ST = 256 Kbit, 3.6V Serial SRAM, Automotive temp., TSSOP package

23A256/23K256

NOTES:

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