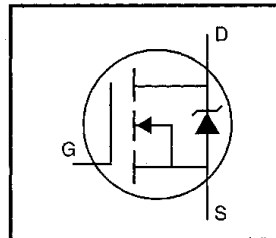


# IRF520PbF

## HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free



$$V_{DSS} = 100V$$

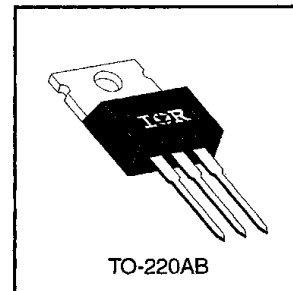
$$R_{DS(on)} = 0.27\Omega$$

$$I_D = 9.2A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	9.2	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	6.5	
$I_{DM}$	Pulsed Drain Current ①	37	
$P_D @ T_C = 25^\circ C$	Power Dissipation	60	W
	Linear Derating Factor	0.40	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	200	mJ
$I_{AR}$	Avalanche Current ①	9.2	A
$E_{AR}$	Repetitive Avalanche Energy ①	6.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to +175	°C
$T_{STG}$			
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

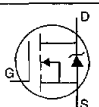
### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	2.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

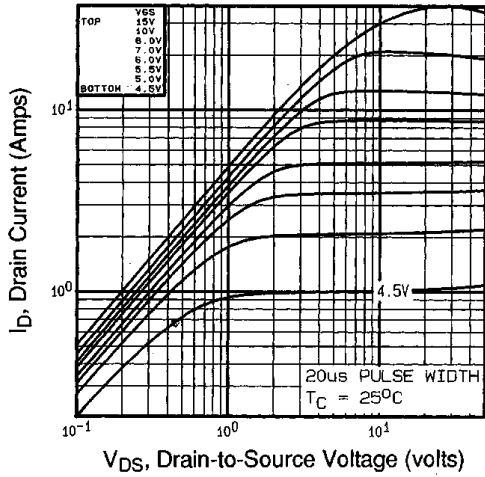
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.13	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.27	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =5.5A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	2.7	—	—	S	V <sub>DS</sub> =50V, I <sub>D</sub> =5.5A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V
		—	—	250		V <sub>DS</sub> =80V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> =20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> =-20V
Q <sub>g</sub>	Total Gate Charge	—	—	16	nC	I <sub>D</sub> =9.2A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	4.4		V <sub>DS</sub> =80V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	7.7		V <sub>GS</sub> =10V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	8.8	—	ns	V <sub>DD</sub> =50V
t <sub>r</sub>	Rise Time	—	30	—		I <sub>D</sub> =9.2A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	19	—		R <sub>G</sub> =18Ω
t <sub>f</sub>	Fall Time	—	20	—		R <sub>D</sub> =5.2Ω See Figure 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	360	—	pF	V <sub>GS</sub> =0V
C <sub>oss</sub>	Output Capacitance	—	150	—		V <sub>DS</sub> =25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	34	—		f=1.0MHz See Figure 5

## Source-Drain Ratings and Characteristics

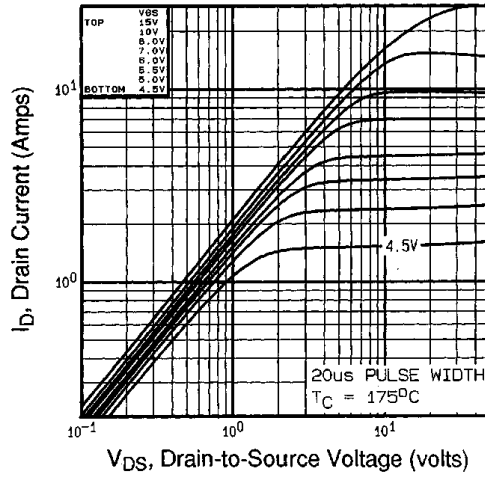
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	9.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	37		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.8	V	T <sub>J</sub> =25°C, I <sub>S</sub> =9.2A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	110	260	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =9.2A
Q <sub>rr</sub>	Reverse Recovery Charge	—	0.53	1.3	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

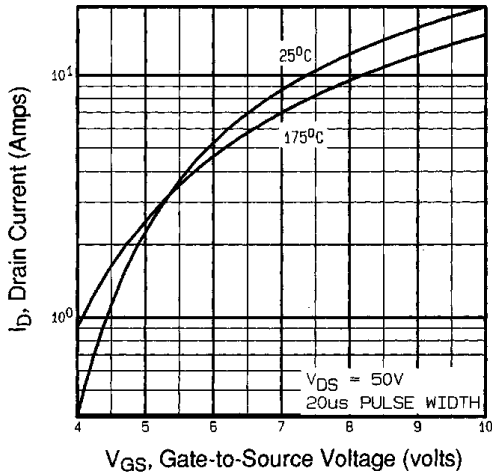
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=25V, starting T<sub>J</sub>=25°C, L=3.5mH, R<sub>G</sub>=25Ω, I<sub>AS</sub>=9.2A (See Figure 12)
- ③ I<sub>SD</sub>≤9.2A, di/dt≤110A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤175°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.



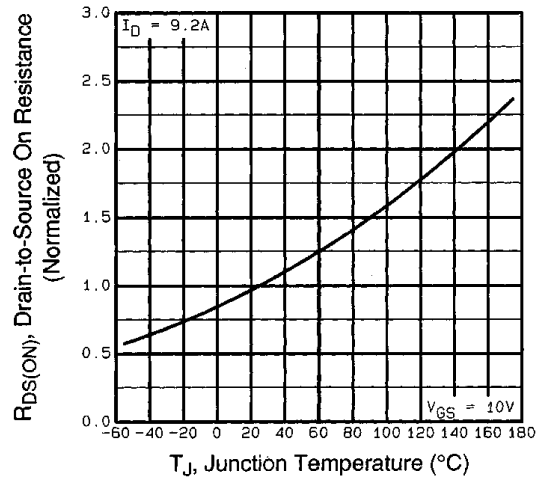
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



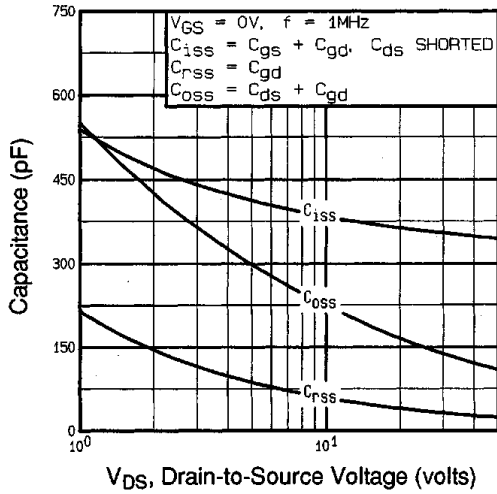
**Fig 2.** Typical Output Characteristics,  
 $T_C=175^\circ\text{C}$



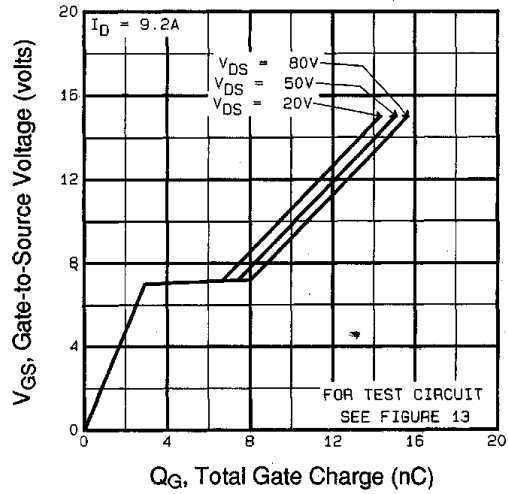
**Fig 3.** Typical Transfer Characteristics



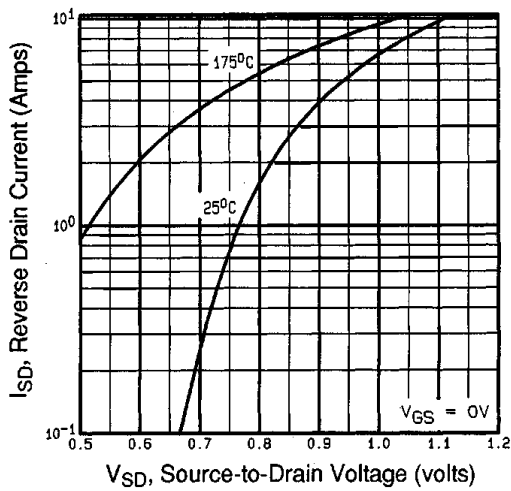
**Fig 4.** Normalized On-Resistance  
 Vs. Temperature



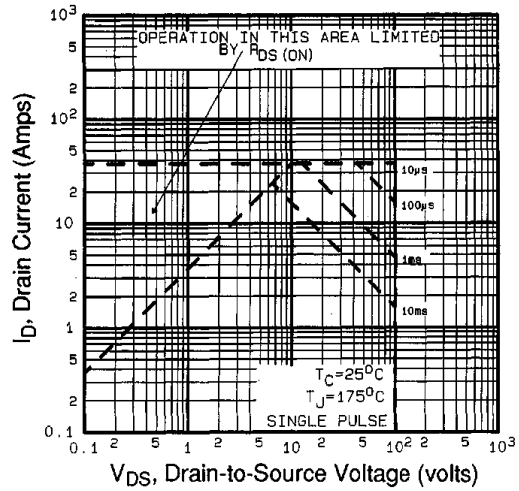
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



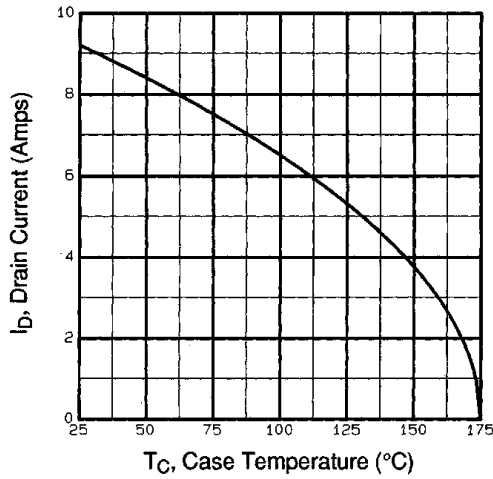
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



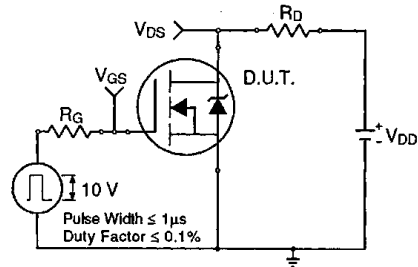
**Fig 7.** Typical Source-Drain Diode Forward Voltage



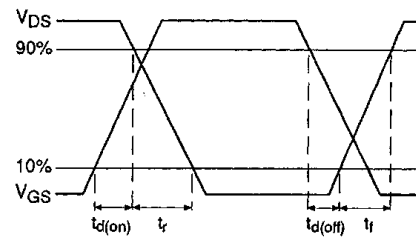
**Fig 8.** Maximum Safe Operating Area



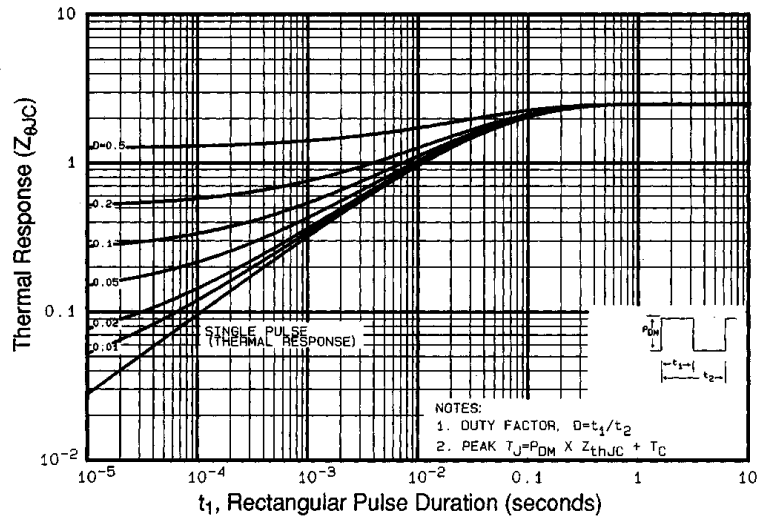
**Fig 9.** Maximum Drain Current Vs. Case Temperature



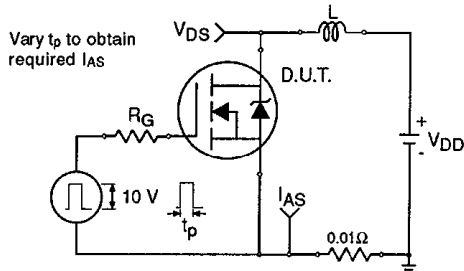
**Fig 10a.** Switching Time Test Circuit



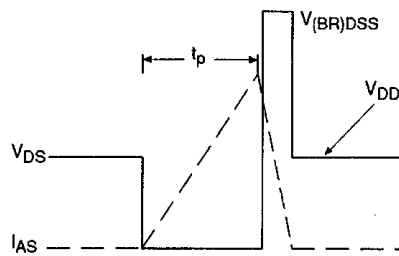
**Fig 10b.** Switching Time Waveforms



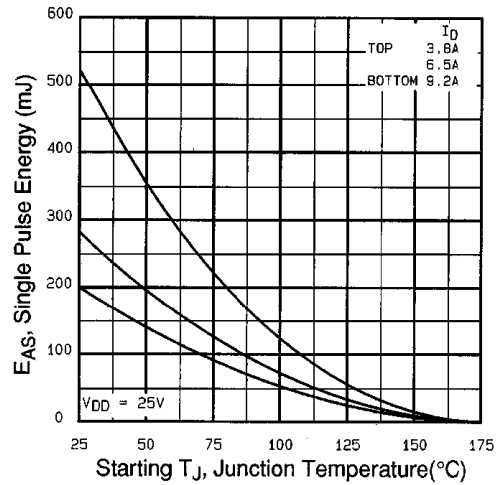
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



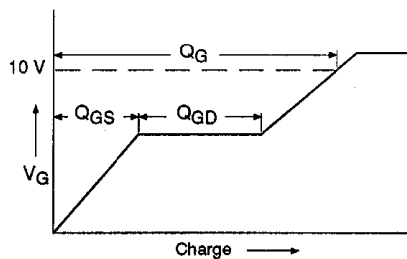
**Fig 12a.** Unclamped Inductive Test Circuit



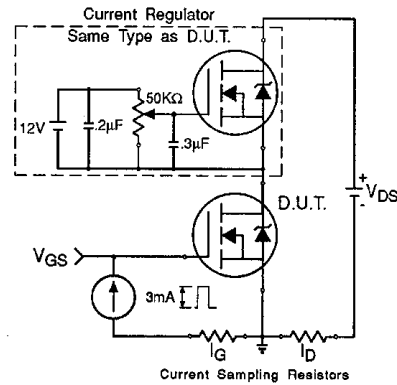
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

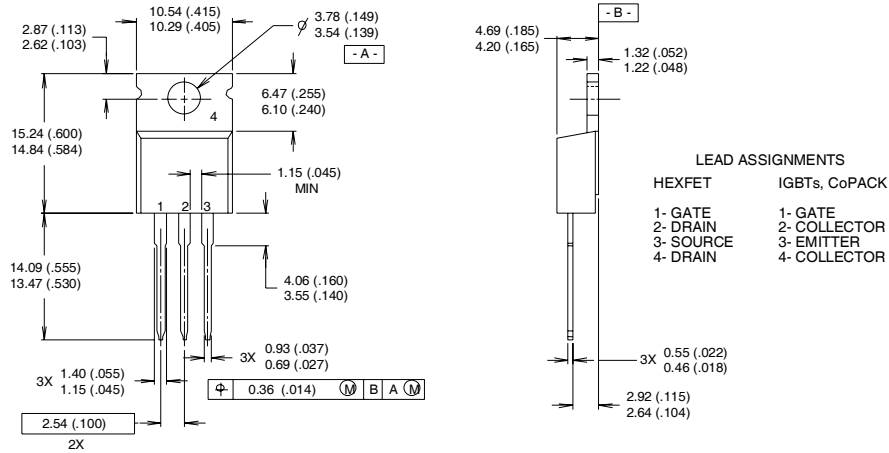
**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1509

**Appendix E:** Optional Leadforms – See page 1525

## TO-220AB Package Outline

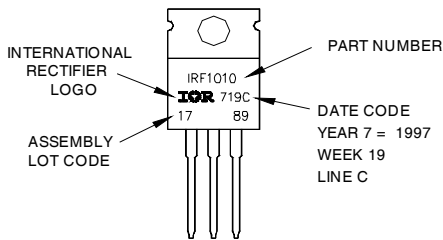
Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
  - 2 CONTROLLING DIMENSION : INCH
  - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
  - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

International  
**IR** Rectifier

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 TAC Fax: (310) 252-7903

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>