LPC804

32-bit Arm® Cortex®-M0+ microcontroller; up to 32 KB flash and 4 KB SRAM; 12-bit ADC; Comparator; 10-bit DAC; Capacitive Touch Interface; Programmable Logic Unit

Rev. 1.8 — 18 March 2021 Product data sheet

1. General description

The LPC804 are an Arm Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 15 MHz. The LPC804 supports 32 KB of flash memory and 4 KB of SRAM.

The peripheral complement of the LPC804 includes a CRC engine, two I^2C-bus interfaces, up to two USARTs, one SPI interface, Capacitive Touch Interface (Cap Touch), one multi-rate timer, self-wake-up timer, one general purpose 32-bit counter/timer, one 12-bit ADC, one 10-bit DAC, one analog comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine, Programmable Logic Unit (PLU), and up to 30 general-purpose I/O pins.

For additional documentation related to the LPC804 parts, see Section 19.

2. Features and benefits

- System:
  - Arm Cortex-M0+ processor (revision r0p1), running at frequencies of up to 15 MHz with single-cycle multiplier and fast single-cycle I/O port.
  - Arm Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - System tick timer.
  - AHB multilayer matrix.
  - Serial Wire Debug (SWD) with four break points and two watch points. JTAG boundary scan (BSDL) supported.
- Memory:
  - Up to 32 KB on-chip EEPROM based flash programming memory.
  - Code Read Protection (CRP).
  - 4 KB SRAM.
- Dual I/O power (LPC804M111JDH24):
  - Independent supplies on each package side permitting level-shifting signals from one off-chip voltage domain to another and/or interfacing directly to off-chip peripherals operating at different supply levels.
  - The switch matrix provides level shifter functionality to allow up to two selected signals to be routed from user-selected pins in one voltage domain to selected pins in the alternate domain. This feature can also be used on a single supply device if voltage level shifting is not required.
- ROM API support:
  - Boot loader.

- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART.
- On-chip ROM APIs for integer divide.
- Free Running Oscillator (FRO) API.

- Digital peripherals:
  - High-speed GPIO interface connected to the Arm Cortex-M0+ I/O bus with up to 30 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, and input inverter. GPIO direction control supports independent set/clear/toggle of individual bits.
  - High-current source output driver (20 mA) on five pins.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight GPIO inputs.
  - Switch matrix for flexible configuration of each I/O pin function.
  - CRC engine.
  - Capacitive Touch Interface.
  - Programmable Logic Unit (PLU) to create small combinatorial and/or sequential logic networks including simple state machines.
- Timers:
  - One 32-bit general purpose counter/timer, with four match outputs and three capture inputs. Supports PWM mode, and external count
  - Four channel Multi-Rate Timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Self-Wake-up Timer (WKT) clocked from either Free Running Oscillator (FRO), a low-power, low-frequency internal oscillator, or an external clock input.
  - Windowed Watchdog timer (WWDT).
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 480 Ksamples/s. The ADC supports two independent conversion sequences.
  - Comparator with five input pins and external or internal reference voltage.
  - One 10-bit DAC.
- Serial peripherals:
  - Two USART interfaces with pin functions assigned through the switch matrix and one fractional baud rate generators.
  - One SPI controllers with pin functions assigned through the switch matrix.
  - Two I^2C-bus interface. It supports data rates up to 400 kbit/s on standard digital pins.
- Clock generation:
  - Free Running Oscillator (FRO). This oscillator provides a selectable 9 MHz, 12 MHz and 15 MHz outputs that can be used as a system clock. The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
  - 1 MHz low power oscillator can be used as a clock source.
  - Clock output function with divider that can reflect all internal clock sources.
- Power control:
  - Reduced power modes: sleep mode, deep-sleep mode, power-down mode, and deep power-down mode.

- Wake-up from deep-sleep and power-down modes on activity on USART, SPI, and I^2C peripherals.
- Wake-up from deep power-down mode on multiple pins.
- Timer-controlled self wake-up from sleep, deep-sleep, and power-down modes.
- Power-On Reset (POR).
- Brownout detect (BOD).

- Unique device serial number for identification.
- Single power supply (1.71 V to 3.6 V).
- Operating temperature range -40 °C to +105 °C.
- Available in WLCSP20, TSSOP20, TSSOP24, and HVQFN33 packages.

3. Applications

- Sensor gateways
- Industrial
- Gaming controllers
- 8/16-bit applications
- Consumer
- Climate control
- Simple motor control
- Portables and wearables
- Lighting
- Motor control
- Fire and security applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC804M101JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC804M101JDH24	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
LPC804M111JDH24	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
LPC804M101JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11
LPC804UK	WLCSP20	wafer level chip-size package; 20 (5 × 4) bumps; 2.50 ×1.84 × 0.5 mm	SOT1397-8

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/KB	SRAM/KB	USART	I^2C	SPI	DAC	Capacitive Touch	PLU	GPIO	Dual I/O power supply	Package
LPC804M101JDH20	32	4	2	2	1	-	yes	yes	17	-	TSSOP20
LPC804M101JDH24	32	4	2	2	1	1	yes	yes	21	-	TSSOP24
LPC804M111JDH24	32	4	2	2	1	1	yes	yes	20	yes	TSSOP24
LPC804M101JHI33	32	4	2	2	1	1	yes	yes	30	-	HVQFN33
LPC804UK	32	4	2	2	1	-	yes	yes	17	-	WLCSP20

5. Marking

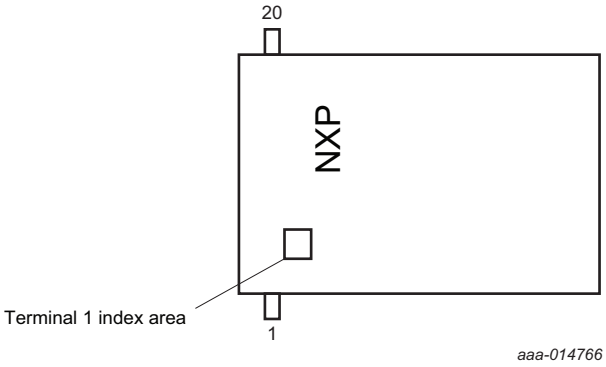


Fig 1. TSSOP20 and TSSOP24 package markings

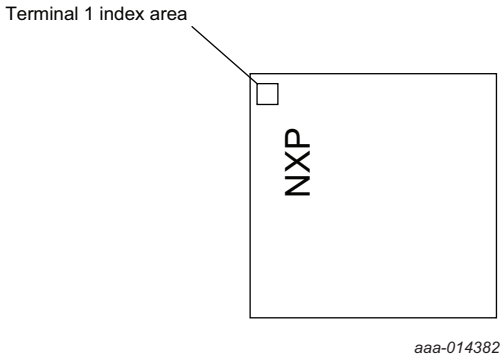


Fig 2. HVQFN33 package marking

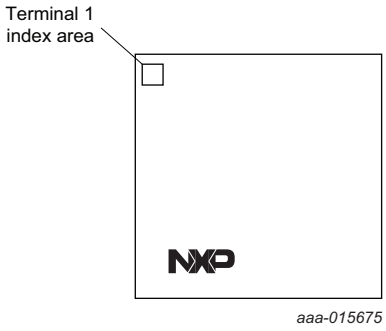


Fig 3. WLCSP20 package marking

The LPC804 HVQFN33 packages have the following top-side marking::

- First line: LPC804M1
- Second line: xxxx
- Third line: yywwx[R]
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

The LPC804 TSSOP20 packages typically have the following top-side marking:

- First line: LPC804
- Second line: M101
- Third line: xxxx
- Fourth line: xxywwx[R]
  - yww: Date code with y = year and ww = week.
  - xR = Boot code version and device revision.

The LPC804 TSSOP24 packages have the following top-side marking:

- First line: LPC804
- Second line: xxxx
- Third line: ywwx[R]
  - yww: Date code with y = year and ww = week.
  - xR = Boot code version and device revision.
- Fourth line: M1y1J
  - y: 0 or 1

The LPC804 WLCSP20 packages have the following top-side marking:

- First line: LPC804
- Second line: xxxxx
- Third line: xyywwx[R]
  - yyww: Date code with ww = week and yy = year.
  - xR = Boot code version and device revision.
- Fourth line: xxx - yyy

Table 3. Device revision table

Revision identifier (R)	Revision description
1A	Initial device revision with Boot ROM version 13.1
1B	Initial device revision with Boot ROM version 13.1
1C	Initial device revision with Boot ROM version 13.1

6. Block diagram

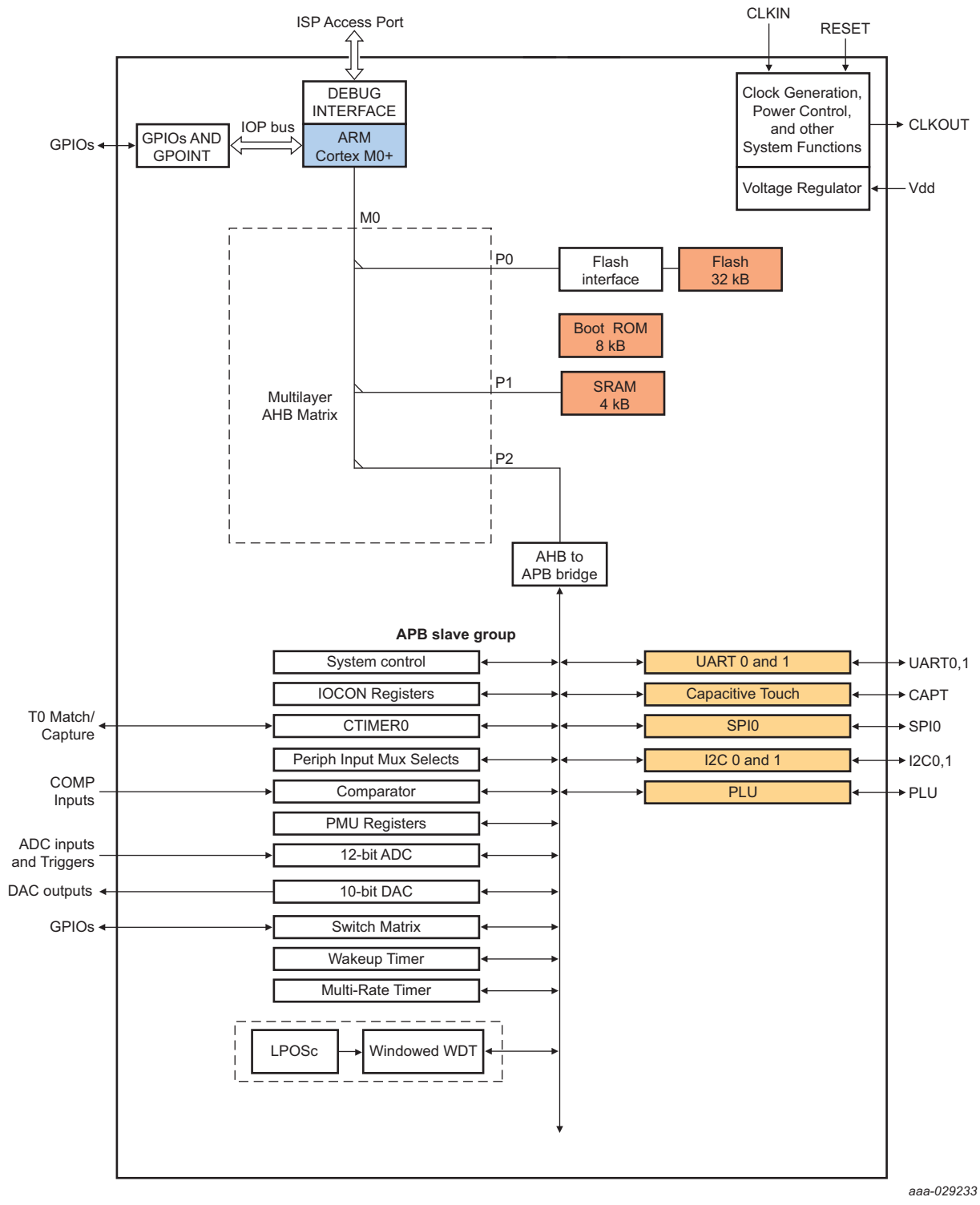


Fig 4. LPC804 block diagram

7. Pinning information

7.1 Pinning

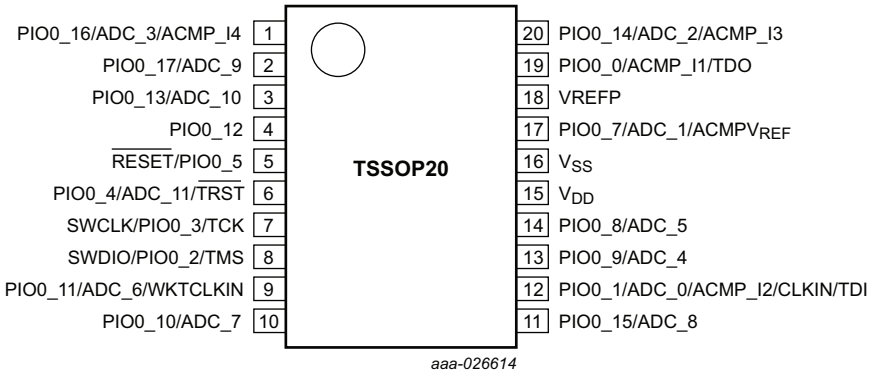


Fig 5. Pin configuration TSSOP20 package

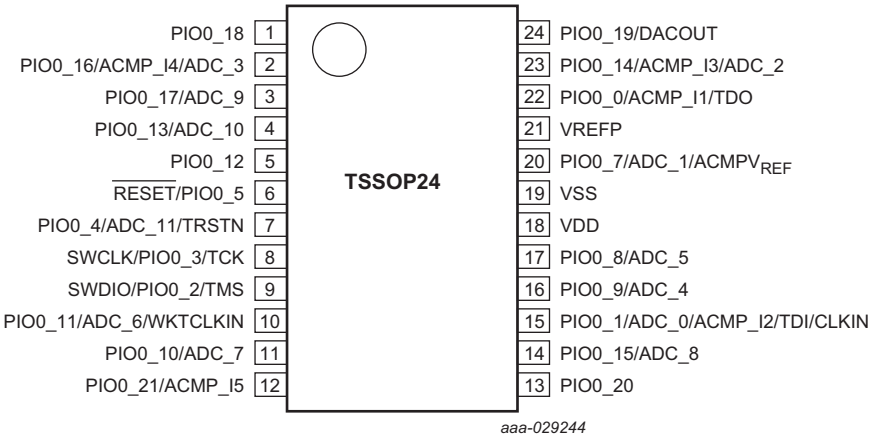


Fig 6. Pin configuration TSSOP24 - 1 package (LPC804M101JDH24 - single supply device)

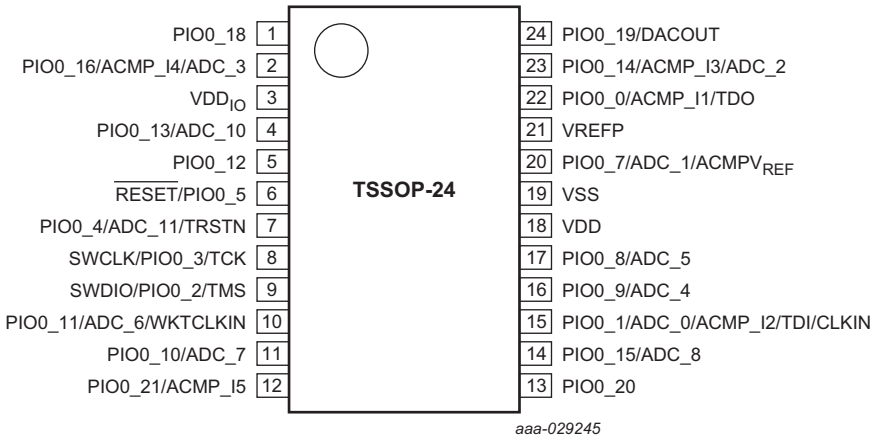
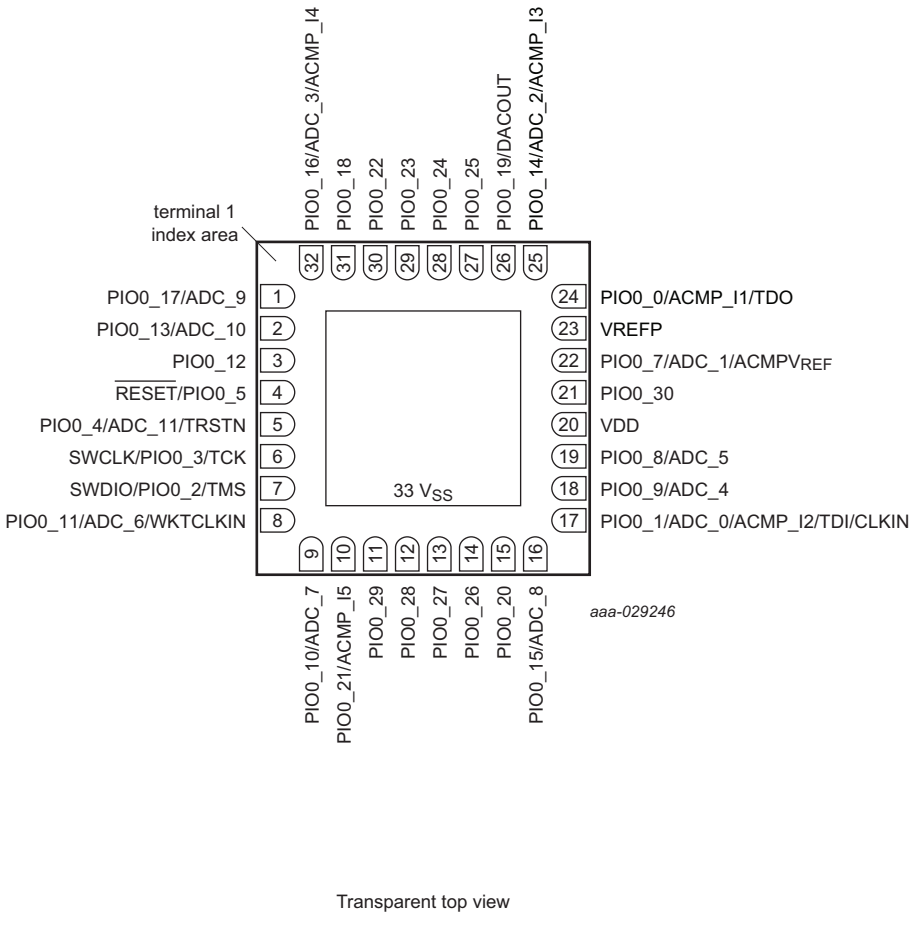


Fig 7. Pin configuration TSSOP24 - 2 package with VDDIO (LPC804M111JDH20 - dual supply device)



Transparent top view

Fig 8. Pin configuration HVQFN33 package

7.2 Pin description

Table 4 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, and $\overline{\text{RESET}}$ pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable functions for the I2C, USART, SPI, CTimer pins, Capacitive Touch, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, an output and/or one or more inputs can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Eight GPIO pins trigger a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via an external pin, do not assign any movable function to this pin. The GPIO pins should be pulled HIGH externally before entering deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit deep power-down mode and wakes up the part.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

PIO0_2, PIO0_3, PIO0_12, PIO0_18, and PIO0_20 are the high drive output pins. PIO0_4, PIO0_8, PIO0_9, PIO0_10, PIO0_11, PIO0_13, PIO0_15, and PIO0_17 are the $\overline{\text{WAKEUP}}$ pins.

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
PIO0_0/ACMP_I1/TDO	22	22	19	24	D3	[2]	I; PU	IO	**PIO0_0 —** General-purpose port 0 input/output 0. In ISP mode, this is the U0_RXD pin (for single supply devices). In boundary scan mode: TDO (Test Data Out).
								A	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ADC_0/ACMP_I2/ TDI/CLKIN	15	15	12	17	A4	[2]	I; PU	IO	**PIO0_1 —** General-purpose port 0 input/output 1. In boundary scan mode: TDI (Test Data In).
								A	**ACMP_I2 —** Analog comparator input 2.
								I	**CLKIN —** External clock input.
SWDIO/PIO0_2/ TMS	9	9	8	7	B2	[3]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
								I/O	**PIO0_2 —** General-purpose port 0 input/output 2.
SWCLK/PIO0_3/ TCK	8	8	7	6	B1	[3]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
								IO	**PIO0_3 —** General-purpose port 0 input/output 3.
PIO0_4/ADC_11/ TRSTN	7	7	6	5	C2	[2]	I; PU	IO	**PIO0_4 —** General-purpose port 0 input/output 4. In ISP mode, this pin is the U0_TXD pin (for single supply devices). In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset).
								A	**ADC_11 —** ADC input 11.
$\overline{\text{RESET}}$/PIO0_5	6	6	5	4	C1	[5]	I; PU	IO	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{RESET}}$ function is not needed.
								I	**PIO0_5 —** General-purpose port 0 input/output 5.

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
PIO0_7/ADC_1/ $ACMPV_{REF}$	20	20	17	22	D4	[2]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7.
								A	**ADC_1 —** ADC input 1.
									$ACMPV_{REF}$ — Alternate reference voltage for the analog comparator.
PIO0_8/ADC_5	17	17	14	19	C3	[2]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8. In ISP mode, this is the U0_RXD pin (for dual supply devices).
								A	**ADC_5 —** ADC input 5.
PIO0_9/ADC_4	16	16	13	18	B3	[2]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9. In ISP mode, this is the U0_TXD pin (for dual supply devices).
								A	**ADC_4 —** ADC input 4.
PIO0_10/ADC_7	11	11	10	9	A2	[2]	I; PU	I; F	**PIO0_10 —** General-purpose port 0 input/output 10.
									ADC_7 — ADC input 7.
PIO0_11/ADC_6/ WKTCLKIN	10	10	9	8	A1	[2]	I; PU	I; F	**PIO0_11 —** General-purpose port 0 input/output 11.
									ADC_6 — ADC input 6.
									WKTCKLKIN — This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in sleep, deep-sleep, and power-down modes.
PIO0_12	5	5	4	3	D1	[3]	I; PU	IO	**PIO0_12 —** General-purpose port 0 input/output 12. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler.
PIO0_13/ADC_10	4	4	3	2	D2	[2]	I; PU	IO	**PIO0_13 —** General-purpose port 0 input/output 13.
								A	**ADC_10 —** ADC input 10.
PIO0_14/ACMP_3/ ADC_2	23	23	20	25	E3	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
								A	**ACMP_I3 —** Analog comparator common input 3.
								A	**ADC_2 —** ADC input 2.
PIO0_15/ADC_8	14	14	11	16	A3	[4]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
									ADC_8 — ADC input 8.

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
PIO0_16/ACMP_I4/ ADC_3	2	2	1	32	E2	[3]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
									ACMP_I4 — Analog comparator common input 4.
									ADC_3 — ADC input 3.
PIO0_17/ADC_9	3	-	2	1	E1	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
								A	**ADC_9 —** ADC input 9.
PIO0_18	1	1	-	31	-	[3]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
PIO0_19/DACOUT	24	24	-	26	-	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
								A	**DACOUT —** DAC output.
PIO0_20	13	13	-	15	-	[3]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
PIO0_21/ACMP_I5	12	12	-	10	-	[3]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
									ACMP_15 — Analog comparator common input 5.
PIO0_22	-	-	-	30	-	[3]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
PIO0_23	-	-	-	29	-	[3]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
PIO0_24	-	-	-	28	-	[3]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24.
PIO0_25	-	-	-	27	-	[3]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25.
PIO0_26	-	-	-	14	-	[3]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	-	-	-	13	-	[3]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28	-	-	-	12	-	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28.
PIO0_29	-	-	-	11	-	[3]	I; PU	IO	**PIO0_29 —** General-purpose port 0 input/output 29.
PIO0_30	-	-	-	21	-	[3]	I; PU	IO	**PIO0_30 —** General-purpose port 0 input/output 30.
VREFP	21	21	18	23	E4			A	**VREFP —** ADC positive reference voltage. Must be equal or lower than V_{DD}.

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
V_{DD}	18	18	15	20	B4		-	-	If VDDIO is present, VDD is the supply voltage for the I/Os on the right side of the package and the core voltage regulator. If VDDIO is not present, VDD also supplies voltage to the I/Os on the left side of the package.
VDD_{IO}	-	3	-	-	-		-	-	If present, it is the supply voltage for the I/Os on the left side of the package.
V_{SS}	19		16	33[8]	C4		-	-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled; F = floating. For pin states in the different power modes, see Section 15.5 “Pin states in different power modes”. For termination on unused pins, see Section 15.4 “Termination of unused pins”.

[2] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[5] See Figure 16 for the reset pad configuration. This pin includes a 20 ns glitch filter (active in all power modes). $\overline{\text{RESET}}$ functionality is not available in deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from deep power-down mode.

[6] The WKTCLKIN function is enabled in the PINENABLE0 register in the PMU. See the LPC804 user manual.

[7] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

[8] Thermal pad for HVQFN33.

8. Movable functions

Movable functions for the I2C, USART, SPI, CTimer pins, Capacitive Touch, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the fixed functions of the pin.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_5, PIO0_7 to PIO0_30 through switch matrix)

Function name	Type	Description
Ux_TXD	O	Transmitter output for USART0 to USART1.
Ux_RXD	I	Receiver input for USART0 to USART1.
$\overline{\text{Ux\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{Ux\_CTS}}$	I	Clear To Send input for USART0.
Ux_SCLK	I/O	Serial clock input/output for USART0 to USART1 in synchronous mode.
SPIx_SCK	I/O	Serial clock for SPI0.
SPIx_MOSI	I/O	Master Out Slave In for SPI0.
SPIx_MISO	I/O	Master In Slave Out for SPI0.
SPIx_SSEL0	I/O	Slave select 0 for SPI0.
SPIx_SSEL1	I/O	Slave select 1 for SPI0.
I2Cx_SDA	I/O	I^2C0 and I^2C1 bus data input/output.
I2Cx_SCL	I/O	I^2C0 and I^2C1 bus clock input/output.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.
T0_MAT0	O	Timer Match channel 0.
T0_MAT1	O	Timer Match channel 1.
T0_MAT2	O	Timer Match channel 2.
T0_MAT3	O	Timer Match channel 3.
T0_CAP0	I	Timer Capture channel 0.
T0_CAP1	I	Timer Capture channel 1.
T0_CAP2	I	Timer Capture channel 2.
CAPT_X0	O	CAPT_X0 function.
CAPT_X1	O	CAPT_X1 function.
CAPT_X2	O	CAPT_X2 function.
CAPT_X3	O	CAPT_X3 function.
CAPT_X4	O	CAPT_X4 function.
CAPT_YL	O	CAPT_YL function.
CAPT_YH	O	CAPT_YH function.
LVLSHFT_IN0	I	Level shift input 0.
LVLSHFT_IN1	I	Level shift input 1.
LVLSHFT_OUT0	O	Level shift output 0.
LVLSHFT_OUT1	O	Level shift output 1.

9. Functional description

9.1 Arm Cortex-M0+ core

The Arm Cortex-M0+ core runs at an operating frequency of up to 15 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The Arm Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

9.2 On-chip flash program memory

The LPC804 contain up to 32 KB of on-chip EEPROM based flash program memory.

9.3 On-chip SRAM

The LPC804 contain a total of 4 KB on-chip static RAM data memory.

9.4 On-chip ROM

The on-chip ROM contains the bootloader:

- Boot loader.
- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART.
- On-chip ROM APIs for integer divide.
- Free Running Oscillator (FRO) API.

9.5 Memory map

The LPC804 incorporates several distinct memory regions. Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The Arm private peripheral bus includes the Arm core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

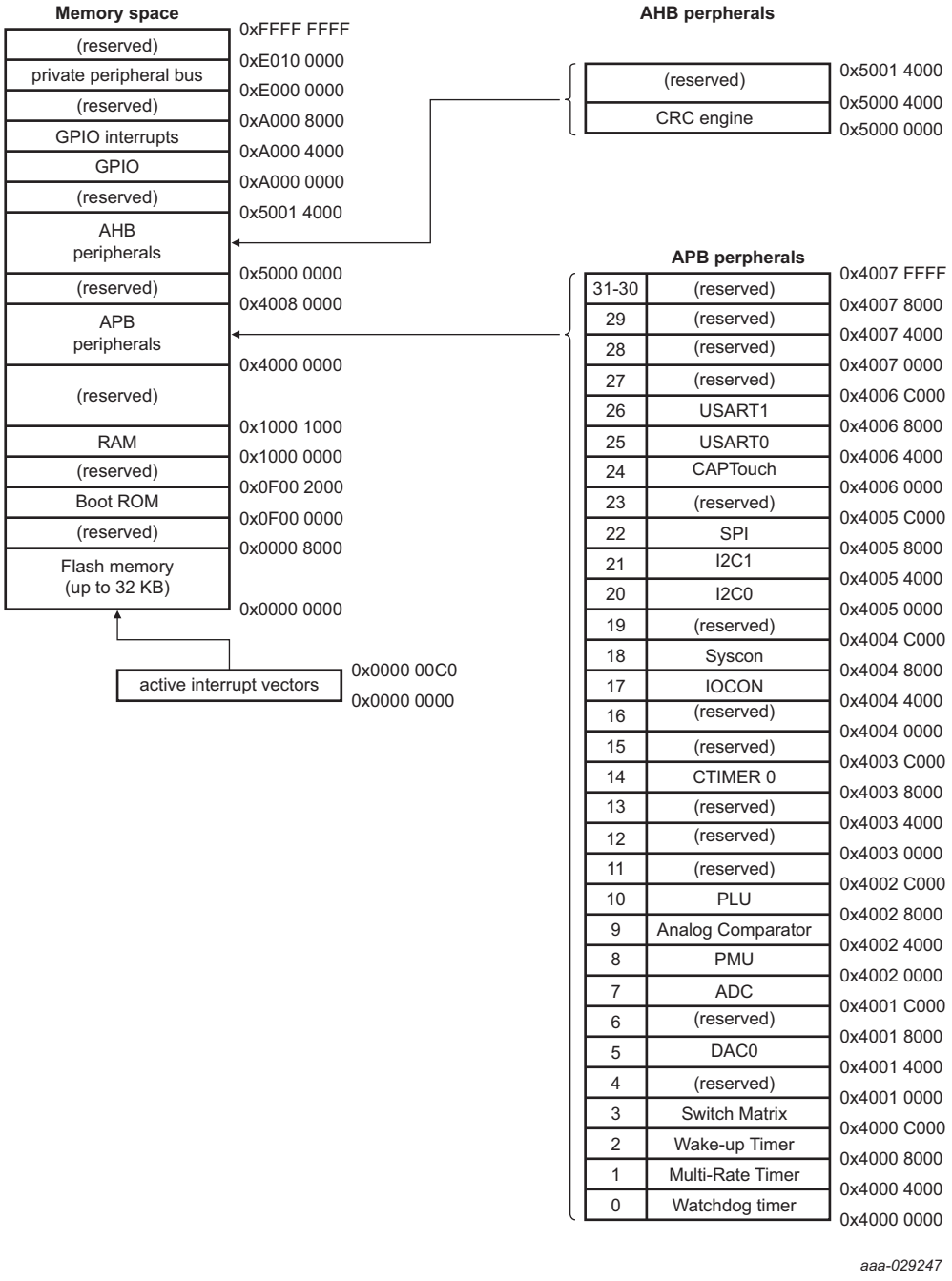


Fig 9. LPC804 Memory mapping

9.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

9.6.1 Features

- Nested Vectored Interrupt Controller is a part of the Arm Cortex-M0+.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC804, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the Arm exceptions SVCall and PendSV.
- Supports NMI.

9.6.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

9.7 System tick timer

The Arm Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

9.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 12 “LPC804 clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.
- The LPC804 uses a dual voltage I/O feature. The pins on one side of the package are supplied by VDDIO and the pins on the other side are supplied by VDD. Each of these two supplies can be connected to different voltages within the allowed Vdd range. This feature allows the device to level-shift signals from one off-chip voltage domain to another.

- The switch matrix provides level shifter functionality to allow up to two selected signals to be routed from user-selected pins in one voltage domain to selected pins in the alternate domain. This feature can also be used on a single supply device if voltage level shifting is not required.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 9.9 for details.

9.8.1 Standard I/O pad configuration

Figure 10 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

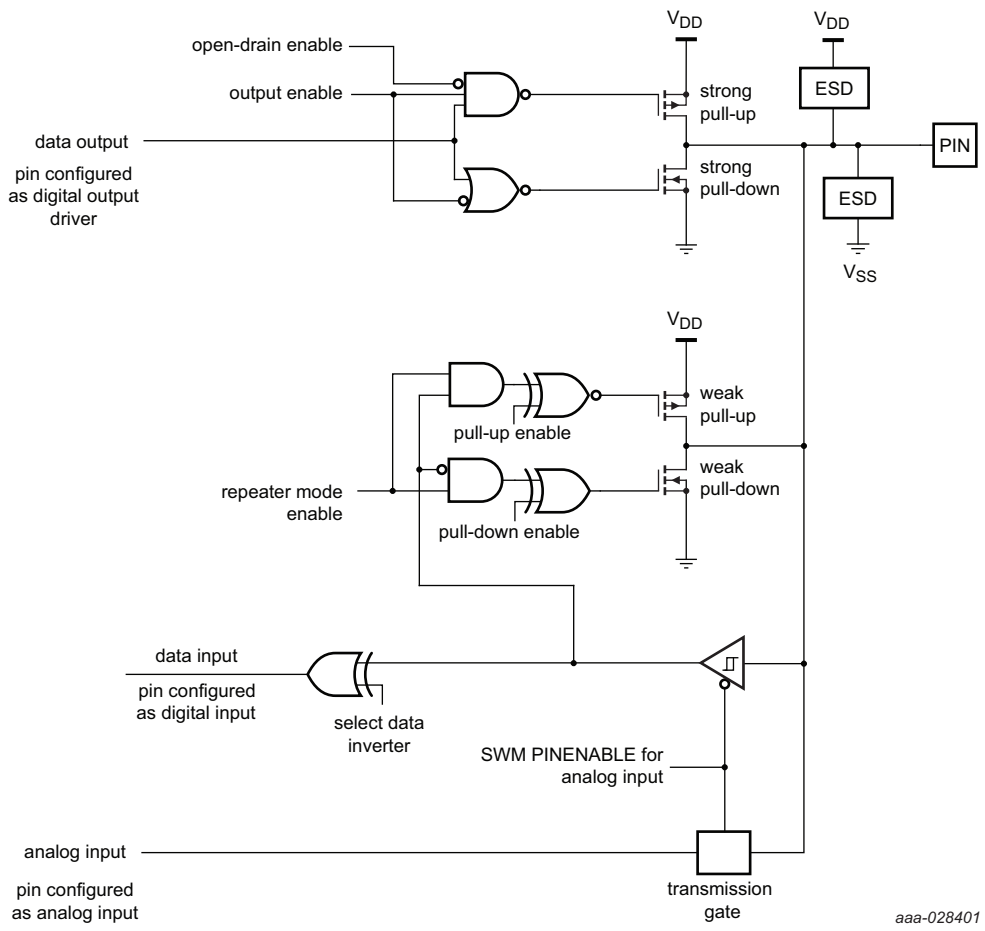


Fig 10. Standard I/O pad configuration

9.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, CTimer, Capacitive Touch, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Section 7.2 “Pin description”. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

9.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC804 use accelerated GPIO functions:

- GPIO registers are on the Arm Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 7 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and $\overline{\text{RESET}}$/PIO0_5, the switch matrix enables the GPIO port pin function by default.

9.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to GPIO inputs with internal pull-up resistors enabled after reset.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 10).
- Direction (input/output) can be set and cleared individually.
- Pin direction bits can be toggled.

9.11 Pin interrupt

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt. The registers that control the pin interrupt are on the IO+ bus for fast single-cycle access.

9.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC804 from sleep mode, deep-sleep mode, and power-down mode.

9.12 USART0/1

All USART functions are movable functions and are assigned to pins through the switch matrix.

9.12.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Baud rate clock can also be output in asynchronous mode.

9.13 SPI0

All SPI functions are movable functions and are assigned to pins through the switch matrix.

9.13.1 Features

- Maximum data rates of up to 15 Mbit/s in master mode and up to 20 Mbit/s in slave mode for SPI functions connected to all digital pins.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data, which can be useful while setting up an SPI memory.
- Control information can optionally be written along with data, which allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

9.14 I^2C-bus interface (I^2C0 and I^2C1)

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master.

9.14.1 Features

- I^2C0 and I^2C1 support standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.

9.15 Capacitive Touch Interface

The Capacitive Touch interface is designed to handle up to five capacitive buttons in different sensor configurations, such as slider, and button matrix. It operates in sleep, deep sleep, and power-down modes, allowing very low power performance.

The Capacitive Touch module measures the change in capacitance of an electrode plate when an earth-ground connected object (for example, finger) is brought within close proximity.

9.16 CTimer

9.16.1 General-purpose 32-bit timers/external event counter

The LPC804 has one general-purpose 32-bit timer/counter.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The timer/counter also includes three capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

9.16.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to three 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins can vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Shadow registers are added for glitch-free PWM output.
- For each timer, up to 4 external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins can vary by device):
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to 4 match registers can be configured for PWM operation, allowing up to 3 single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins can vary by device.)

9.17 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with two channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

9.17.1 Features

- 31-bit interrupt timer
- Two channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

9.18 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

9.18.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) is generated by the dedicated watchdog oscillator (WDOSC).

9.19 Self-Wake-up Timer (WKT)

The self-wake-up timer is a 32-bit, loadable down counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur prior to entering a reduced power mode.

9.19.1 Features

- 32-bit loadable down counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT supports three clock sources: an external clock on the WKTCLKIN pin, the low-power oscillator, and the FRO. The low-power oscillator can be used as the clock source in sleep, deep-sleep, and power-down modes.
- The WKT can be used for waking up the part from any reduced power mode or for general-purpose timing.

9.20 Programmable Logic Unit (PLU)

The PLU is comprised of 26 5-input LUT elements. Each LUT element contains a 32-bit truth table (look-up table) register and a 32:1 multiplexer. During operation, the five LUT inputs control the select lines of the multiplexer. This structure allows any desired logical combination of the five LUT inputs.

9.20.1 Features

- The PLU is used to create small combinatorial and/or sequential logic networks including simple state machines.
- The PLU is comprised of an array of 26 inter-connectable, 5-input Look-up Table (LUT) elements, and four flip-flops.
- Eight primary outputs can be selected using a multiplexer from among all of the LUT outputs and the four flip-flops.
- An external clock to drive the four flip-flops must be applied to the PLU_CLKIN pin if a sequential network is implemented.
- Programmable logic can be used to drive on-chip inputs/triggers through external pin-to-pin connections.
- A tool suite is provided to facilitate programming of the PLU to implement the logic network described in a Verilog RTL design.

Remark: PLU cannot be used to wake-up from sleep, deep-sleep, power-down, and deep power-down modes.

9.21 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 27.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled through the switch matrix.

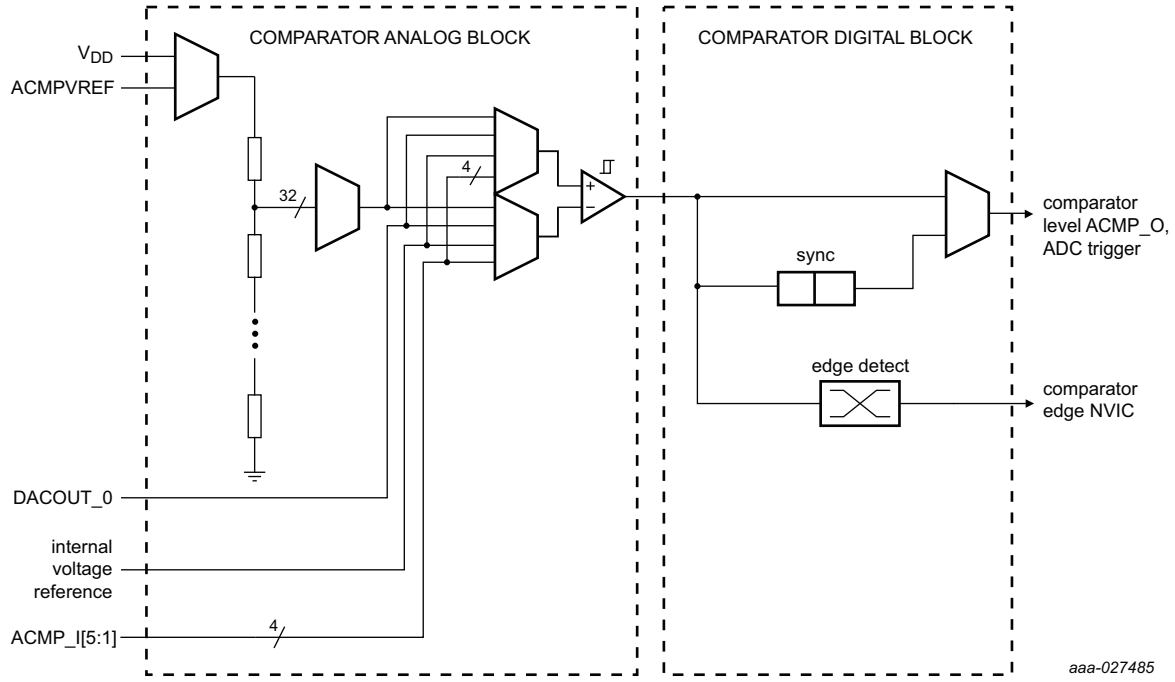


Fig 11. Comparator block diagram

9.21.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or $ACMPV_{REF}$); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- One comparator output is internally collected to the ADC trigger input multiplexer.

9.22 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 480 KSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the pin triggers, the analog comparator output, and the Arm TXEV.

The ADC includes a hardware threshold compare function with zero-crossing detection.

Remark: For best performance, select VREFP and VREFN at the same voltage levels as V_{DD} and V_{SS}. When selecting VREFP and VREFN different from VDD and VSS, ensure that the voltage midpoints are the same:

(VREFP-VREFN)/2 + VREFN = V_{DD}/2

9.22.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of up to 480 KSamples/s.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (not to exceed V_{DD} voltage level).
- Burst conversion mode for single or multiple inputs.

9.23 Digital-to-Analog Converter (DAC)

The DAC supports a resolution of 10 bits. Conversions can be triggered by an external pin input or an internal timer. The DAC includes an optional automatic hardware shut-off feature, which forces the DAC output voltage to zero while a HIGH level on the external DAC_SHUTOFF pin is detected.

9.23.1 Features

- 10-bit digital-to-analog converter.
- Internal timer or pin external trigger for staged, jitter-free DAC conversion sequencing.
- Automatic hardware shut-off triggered by an external pin.

9.24 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

9.24.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1’s complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

9.25 Clocking and power control

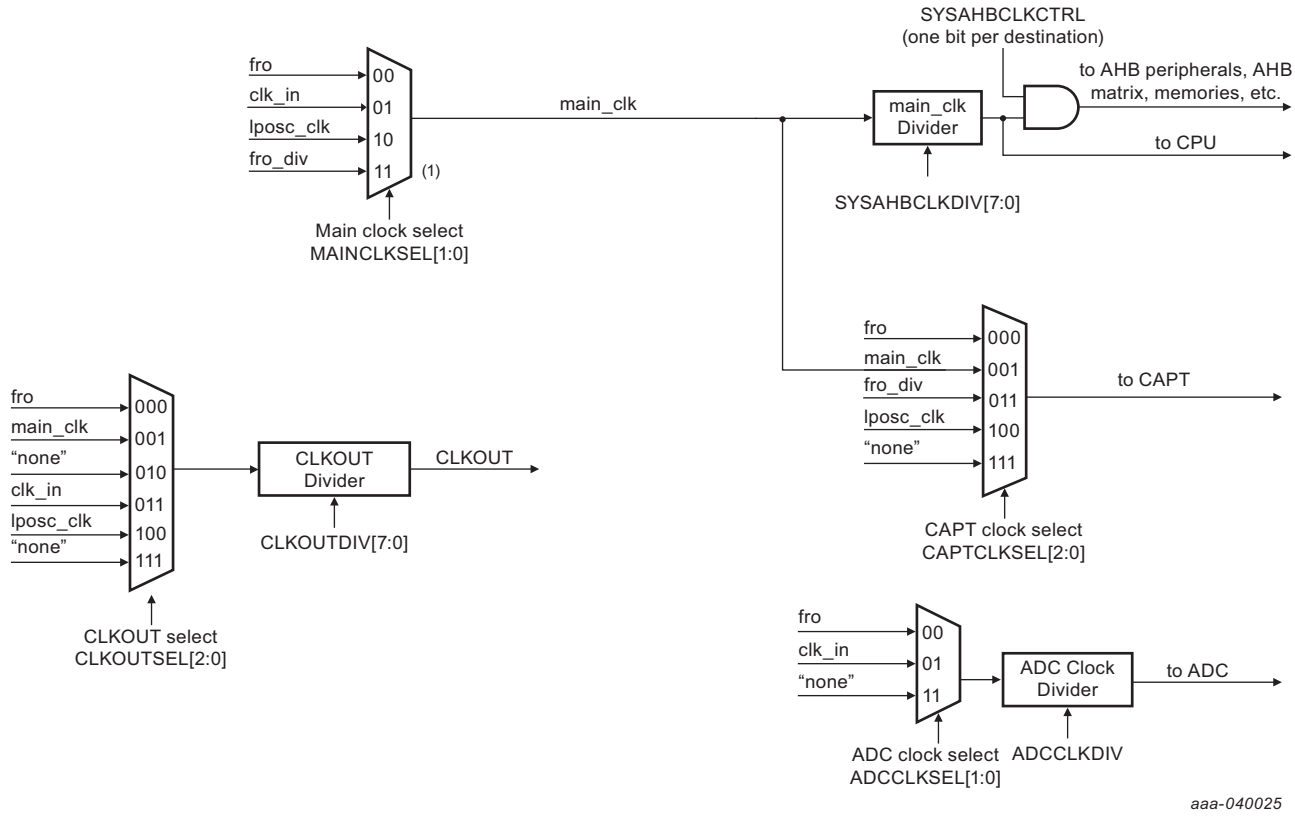


Fig 12. LPC804 clock generation

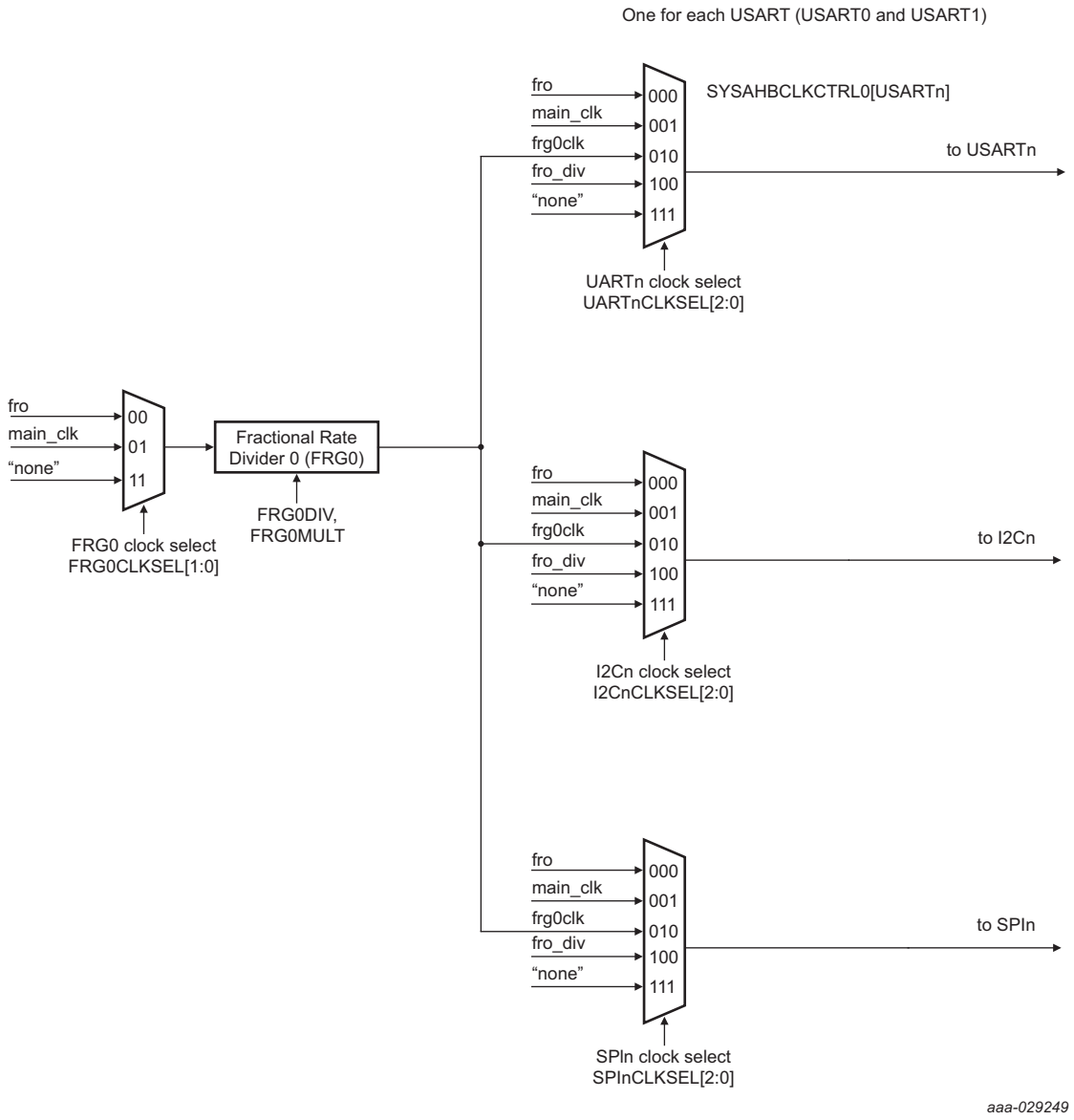


Fig 13. LPC804 clock generation (continued)

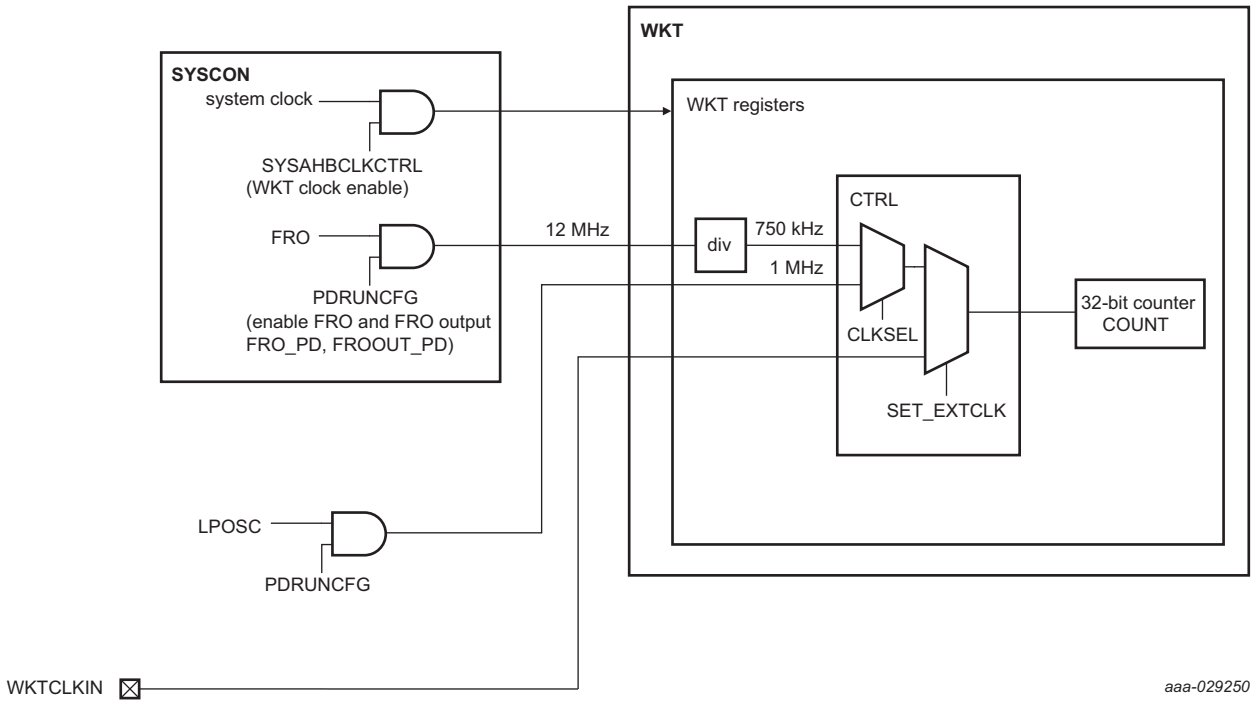


Fig 14. LPC804 WKT clocking

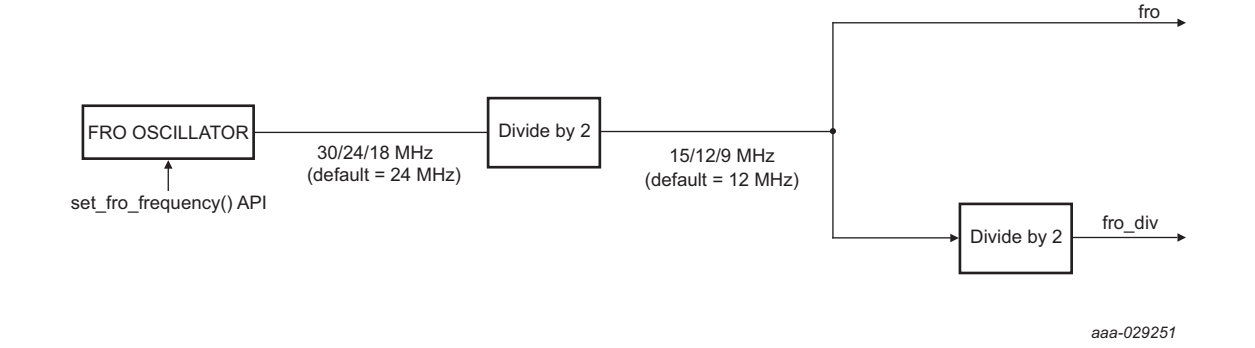


Fig 15. LPC804 FRO subsystem

Table 6. Clocking diagram signal name descriptions

Name	Description
clk_in	The internal clock that comes from the main CLK_IN pin function. That function must be connected to the pin by selecting it in the SWM block.
frg_clk	The output of the Fractional Rate Generator. The FRG and its source selection are shown in Figure 13.
fro_div	Divided output of the currently selected on-chip FRO oscillator. See Figure 15.
fro	The output of the currently selected on-chip FRO oscillator. See Figure 15.

Table 6. Clocking diagram signal name descriptions

Name	Description
main_clk	The main clock used by the CPU and AHB bus, and potentially many others. The main clock and its source selection are shown in Figure 12.
“none”	A tied-off source that should be selected to save power when the output of the related multiplexer is not used.
lposc_clk	The output of the 1 MHz low power oscillator. It must also be enabled in the PDRUNCFG0 register.

9.25.1 Internal oscillators

The LPC804 include two independent oscillators:

1. Free Running Oscillator.
2. Low power oscillator.

Following reset, the LPC804 operates from the FRO until switched by software allowing the part to run without any external clock and the bootloader code to operate at a known frequency.

See Figure 12 for an overview of the LPC804 clock generation.

9.25.1.1 Free Running Oscillator (FRO)

The FRO provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- This oscillator provides a selectable 15 MHz, 12 MHz, and 9 MHz outputs that can be used as a system clock. Also, these outputs can be divided down to 7.5 MHz, 6 MHz, and 4.5 MHz for system clock.
- The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
- By default, the FRO output frequency is default system (CPU) clock frequency of 12 MHz.

9.25.1.2 Low Power Oscillator (LPOsc)

The LPOsc is an independent oscillator which can be used as a system clock. The frequency of the LPCOsc is 1 MHz.

9.25.2 Clock input

An external clock source can be supplied on the selected CLKIN pin. When selecting a clock signal for the CLKIN pin, follow the specifications for digital I/O pins in Table 12 “Static characteristics, supply pins” and Table 18 “Dynamic characteristics: I/O pins[1]”.

The maximum frequency for both clock signals is 15 MHz.

9.25.3 Clock output

The LPC804 features a clock output function that routes any oscillator or the main clock can be selected to the CLKOUT function. The CLKOUT function can be connected to any digital pin through the switch matrix.

9.25.4 Power control

The LPC804 supports the Arm Cortex-M0+ sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

9.25.4.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped. Resumption from the sleep mode does not need any special sequence but re-enabling the clock to the Arm core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

9.25.4.2 Deep-sleep mode

In deep-sleep mode, the LPC804 core is in sleep mode and all peripheral clocks and all clock sources are off except for the FRO or low-power oscillator if selected. The FRO output is disabled. In addition, all analog blocks are shut down and the flash is in standby mode. In deep-sleep mode, the application can keep the low power oscillator and the BOD circuit running for self-timed wakeup and BOD protection.

The LPC804 can wake up from deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, an interrupt from Capacitive Touch, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI (in slave mode), or the I2C blocks (in slave mode).

Any interrupt used for waking up from deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Deep-sleep mode saves power and allows for short wake-up times.

9.25.4.3 Power-down mode

In power-down mode, the LPC804 is in sleep mode and all peripheral clocks and all clock sources are off except for low-power oscillator if selected. In addition, all analog blocks and the flash are shut down. In power-down mode, the application can keep the low-power oscillator and the BOD circuit running for self-timed wake up and BOD protection.

The LPC804 can wake up from power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, an interrupt from Capacitive Touch, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI (in slave mode), or the I2C blocks (in slave mode).

Any interrupt used for waking up from power-down mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Power-down mode reduces power consumption compared to deep-sleep mode at the expense of longer wake-up times.

9.25.4.4 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the $\overline{\text{WAKEUP}}$ pins. The LPC804 can wake up from deep power-down mode via eight $\overline{\text{WAKEUP}}$ pins. See Section 9.19. Five general-purpose registers are available to store information during deep power-down mode.

The LPC804 can be prevented from entering deep power-down mode by setting a lock bit in the PMU block. Locking out deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

When entering deep power-down mode, an external pull-up resistor is required on the $\overline{\text{WAKEUP}}$ pins to hold it HIGH.

Table 7. Peripheral configuration in reduced power modes

Peripheral	Sleep mode	Deep-sleep mode	Power-down mode	Deep power-down mode
FRO	software configurable	on	off	off
FRO output	software configurable	off	off	off
Flash	software configurable	standby	off	off
BOD	software configurable	software configurable	software configurable	off
LPOsc/WWDT	software configurable	software configurable	software configurable	off
Digital peripherals	software configurable	off	off	off
Wake-up buffers	software configurable (cannot be used as wake-up source)	software configurable (cannot be used as wake-up source)	software configurable (cannot be used as wake-up source)	software configurable
ADC	software configurable	off	off	off
DAC	software configurable	off	off	off
Capacitive Touch	software configurable	software configurable	software configurable	off
WKT/low-power oscillator	software configurable	software configurable	software configurable	off
Comparator	software configurable	off	off	off
PLU	off	off	off	off

Table 8. Wake-up sources for reduced power modes

power mode	Wake-up source	Conditions
Sleep	Any interrupt	Enable interrupt in NVIC.
Deep-sleep and power-down	Pin interrupts	Enable pin interrupts in NVIC and STARTERP0 registers.
	BOD interrupt	• Enable interrupt in NVIC and STARTERP1 registers. • Enable interrupt in BODCTRL register. • BOD powered in PDSLEEPCFG register.
	BOD reset	• Enable reset in BODCTRL register. • BOD powered in PDSLEEPCFG register.
	WWDT interrupt	• Enable interrupt in NVIC and STARTERP1 registers. • WWDT running. Enable WWDT in WWDT MOD register and feed. • Enable interrupt in WWDT MOD register. • LPOsc powered in PDSLEEPCFG register.
	WWDT reset	• WWDT running. • Enable reset in WWDT MOD register. • LPOsc powered in PDSLEEPCFG register.
	Self-Wake-up Timer (WKT) time-out	• Enable interrupt in NVIC and STARTERP1 registers. • Enable low-power oscillator in the LPOSCCLKEN register in the SYSCON block. • Select low-power clock for WKT clock in the WKT CTRL register. • Start the WKT by writing a time-out value to the WKT COUNT register.
	Interrupt from USART/SPI/I2C peripheral	• Enable interrupt in NVIC and STARTERP1 registers. • Enable USART/I2C/SPI interrupts. • Provide an external clock signal to the peripheral. • Configure the USART in synchronous slave mode and I2C and SPI in slave mode.
	Interrupt from Capacitive Touch peripheral	• Enable interrupt in NVIC and STARTERP1 registers. • Enable the Capacitive Touch interrupt. • Switch FCLK clock source to the LPOsc. • Set Capacitive Touch registers. • Provide a touch event to the peripheral.
Deep power-down	$\overline{\text{WAKEUP}}$ pins	Enable the $\overline{\text{WAKEUP}}$ function in the WUENAREG register in the PMU.

9.25.5 Wake-up process

The LPC804 begin operation at power-up by using the FRO as the clock source allowing chip operation to resume quickly. If LPOsc or external clock sources are needed by the application, software must enable these features and wait for them to stabilize before they are used as a clock source.

9.26 System control

9.26.1 Reset

Reset has four sources on the LPC804: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the FRO and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

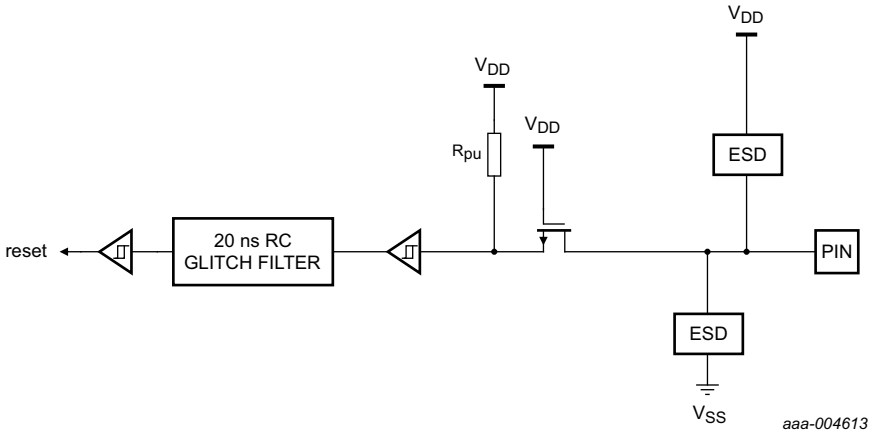


Fig 16. Reset pad configuration

9.26.2 Brownout detection

The LPC804 includes one reset level and three interrupt levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. One threshold level can be selected to cause a forced reset of the chip.

9.26.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP. For details, see the *LPC804 user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled. For details, see the *LPC804 user manual*.

9.26.4 APB interface

The APB peripherals are located on one APB bus.

9.26.5 AHBLite

The AHBLite connects the CPU bus of the Arm Cortex-M0+ to the flash memory, the main static RAM, the ROM, and the APB peripherals.

9.27 Emulation and debugging

Debug functions are integrated into the Arm Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The Arm Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the Arm SWD debug ($\overline{\text{RESET}}$ = HIGH). The Arm SWD debug port is disabled while the LPC804 is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode. See Table 4.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

10. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	–0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP		–0.5	V_{DD}	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq 1.71$ V	[3][4]	–0.5	+5.4	V
		3 V tolerant I/O pin ACMPV_{REF}	[5]	–0.5	+3.6	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[6][7][8]	–0.5	+4.6	V
I_{DD}	supply current	per supply pin (TSSOP20)		-	18	mA
		per supply pin (TSSOP24)		-	22	
		per supply pin (HVQFN33)		-	30	
I_{SS}	ground current	per ground pin (TSSOP20)		-	40	mA
		per ground pin (TSSOP24)		-	45	
		per ground pin (HVQFN33)		-	50	
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[9]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	TSSOP20, based on package heat transfer, not device power consumption	[11]	-	0.36	W

Table 9. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
		TSSOP20, based on package heat transfer, not device power consumption	[12]	-	0.26	W
		TSSOP24, based on package heat transfer, not device power consumption	[11]	-	0.34	W
		TSSOP24, based on package heat transfer, not device power consumption	[12]	-	0.26	W
		HVQFN33, based on package heat transfer, not device power consumption	[11]	-	0.93	W
		HVQFN33, based on package heat transfer, not device power consumption	[12]	-	0.34	W
		WLCSP20, based on package heat transfer, not device power consumption	[11]	-	0.8	W
		WLCSP20, based on package heat transfer, not device power consumption	[12]	-	0.3	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[10]	-	2000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 12) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except the 3 V tolerant pin PIO0_7.

[4] Including the voltage on outputs in 3-state mode.

[5] V_{DD} present or not present.

[6] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[7] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[8] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[9] Dependent on package type.

[10] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[11] JEDEC (4.5 in × 4 in); still air.

[12] Single layer (4.5 in × 3 in); still air.

11. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 10. Thermal resistance

Symbol	Parameter	Conditions	Max/min	Unit
TSSOP20 package				
$R_{th(j-a)}$	thermal resistance from junction-to-ambient	JEDEC (4.5 in × 4 in); still air	108 ± 15 %	°C/W
		single-layer (4.5 in × 3 in); still air	151 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction-to-case		24 ± 15 %	°C/W
TSSOP24 package				
$R_{th(j-a)}$	thermal resistance from junction-to-ambient	JEDEC (4.5 in × 4 in); still air	114 ± 15 %	°C/W
		single-layer (4.5 in × 3 in); still air	153 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction-to-case		31 ± 15 %	°C/W
HVQFN33 package				
$R_{th(j-a)}$	thermal resistance from junction-to-ambient	JEDEC (4.5 in × 4 in); still air	42 ± 15 %	°C/W
		single-layer (4.5 in × 3 in); still air	114 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction-to-case		21 ± 15 %	°C/W
WLCSP20 package				
$R_{th(j-a)}$	thermal resistance from junction-to-ambient	JEDEC (4.5 in × 4 in); still air	56.5 ± 15 %	°C/W
		single-layer (4.5 in × 3 in); still air	148 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction-to-case		0.7 ± 15 %	°C/W

12. Static characteristics

12.1 General operating conditions

Table 11. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	15	MHz
V_{DD}	supply voltage (core and external rail)			1.71	-	3.6	V
		For ADC operations		2.5	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{DDIO}	I/O rail			1.71	-	3.6	V
		For ADC operations		2.5	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{ref}	ADC positive reference voltage	on pin VREFP		2.5	-	V_{DD}	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[2]	-	-	7.1	pF
		pins with digital functions only	[2]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Including bonding pad capacitance. Based on simulation, not tested in production.

12.2 Power consumption

Power measurements in active, sleep, deep-sleep, and power-down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.

Table 12. Static characteristics, supply pins

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[9]	Unit
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;					
		system clock = 1 MHz V_{DD} = 3.3 V	[3][5][6][10]		0.5	-	mA
		system clock = 9 MHz V_{DD} = 3.3 V	[3][4][5][6]		0.8	-	mA
		system clock = 12 MHz V_{DD} = 3.3 V	[3][4][5][6]	-	1.0	-	mA
		system clock = 15 MHz V_{DD} = 3.3 V	[3][4][5][6]	-	1.3	-	mA
		Sleep mode					
		system clock = 9 MHz V_{DD} = 3.3 V	[3][4][5][6]		0.4		
		system clock = 12 MHz V_{DD} = 3.3 V	[3][4][5][6]	-	0.5	-	mA
		system clock = 15 MHz V_{DD} = 3.3 V	[3][4] [5][6]	-	0.6	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[3][7]	-	100	175	µA
		T_{amb} = 105 °C		-	-	240	µA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V T_{amb} = 25 °C	[3][7]	-	6	14	µA
		T_{amb} = 105 °C		-	-	75	µA
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[8]	-	0.15	0.5	µA
		T_{amb} = 105 °C		-	-	7	µA

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), V_{DD} = 3.3 V.

[2] Characterized through bench measurements using typical samples.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] FRO enabled.

[5] BOD disabled.

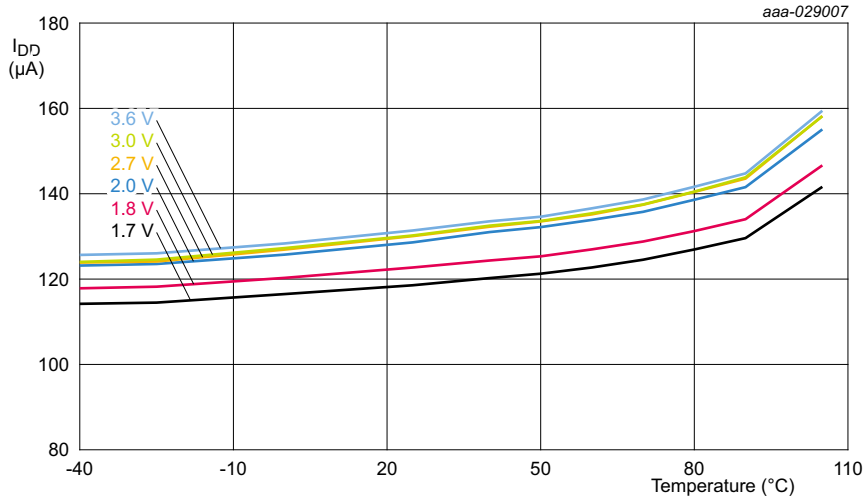
[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks disabled in system configuration block.

[7] All oscillators and analog blocks turned off.

[8] $\overline{\text{WAKEUP}}$ function pin pulled HIGH externally.

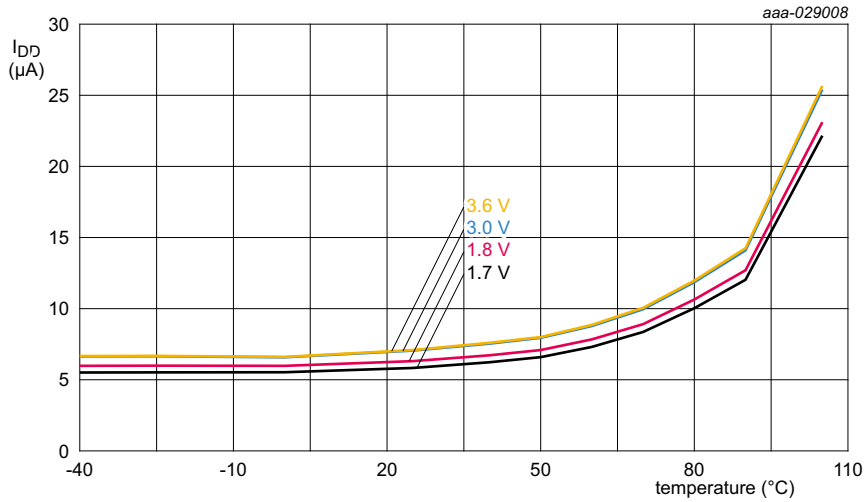
[9] Tested in production, VDD = 3.6 V.

[10] LPOsc enabled, FRO disabled.



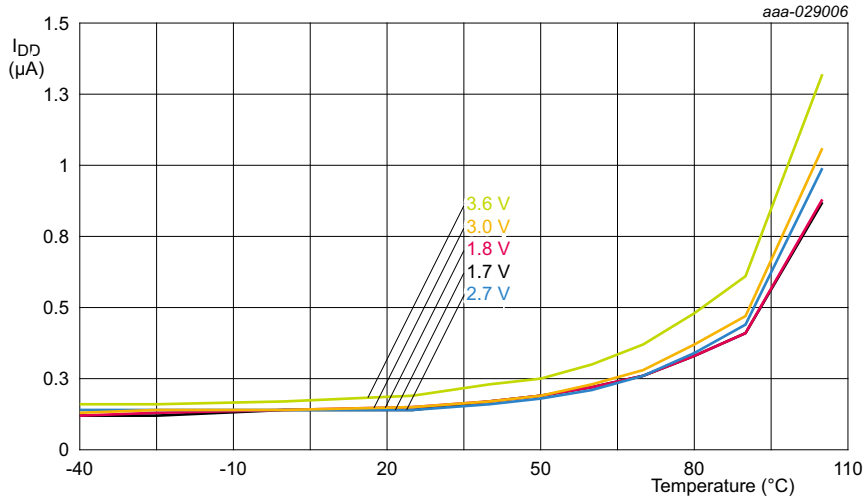
Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register.

Fig 17. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register.

Fig 18. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



WKT not running.

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

12.2.1 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG. and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed. Measured on a typical sample at T_{amb} = 25 °C.

The supply currents are shown for system clock frequencies of 12 MHz and 15 MHz.

Table 13. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	15 MHz	
FRO	74	-	-	FRO = 12MHz. FRO output disabled.
BOD	39	-	-	Independent of main clock frequency.
Flash	80	-	-	-
LPOsc	1	-	-	FRO; independent of main clock frequency.
GPIO + pin interrupt	-	40	54	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	24	30	-
IOCON	-	28	36	-
CTimer	-	28	37	-
MRT	-	45	56	-
WWDT	-	31	41	-
I2C0	-	44	58	-
I2C1	-			
SPI0	-	33	42	-
USART0	-	39	46	-
USART1	-	40	50	-
Comparator ACMP	-	36	46	-
ADC	-	61	78	Digital controller only. Analog portion of the ADC disabled in the PDRUNCFG register.
	-	61	78	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 1 in the ADC CTRL register (ADC in low-power mode).
	-	61	78	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 0 in the ADC CTRL register (ADC powered).
DAC	-	29	35	
Capacitive Touch	-	22	26	
PLU	-	118	149	
CRC	-	37	50	-

12.3 Pin characteristics

Table 14. Static characteristics, electrical pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins configured as digital pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq 1.71$ V; 5 V tolerant pins except PIO0_7		0	-	5.4	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		$V_{DD} - 0.4$	-	-	V
		I_{OH} = 3 mA; 1.71 V <= V_{DD} < 2.5 V		$V_{DD} - 0.5$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		-	-	0.5	V
		I_{OL} = 3 mA; 1.71 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		$V_{OH} = V_{DD} - 0.5$ V; 1.71 V ≤ V_{DD} ≤ 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.71 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[3]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[3]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[4]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V	[4]	10	50	90	µA
		1.71 V ≤ V_{DD} < 2.0 V		7	50	85	µA
		$V_{DD} < V_I < 5$ V		0	0	0	µA
High-drive output pin configured as digital pin (PIO0_2, PIO0_3, PIO0_12, PIO0_18, and PIO0_20)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA

Table 14. Static characteristics, electrical pin characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.5 V <= V_{DD} < 3.6 V		V_{DD} − 0.6	-	-	V
		I_{OH} = 12 mA; 1.71 V <= V_{DD} < 2.5 V		V_{DD} − 0.6	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V I_{OL} = 3 mA; 1.71 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.6 V; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		V_{OH} = V_{DD} − 0.6 V; 1.71 V <= V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.71 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[3]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[4]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V;	[4]				µA
		2.0 V ≤ V_{DD} ≤ 3.6 V		10	50	90	µA
		1.71 V ≤ V_{DD} < 2.0 V		7	50	85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Based on characterization. Not tested in production.

[3] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[4] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 20.

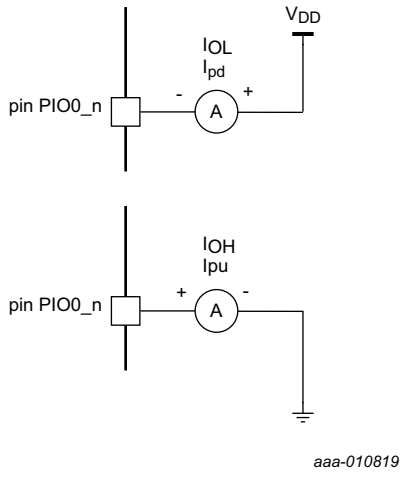
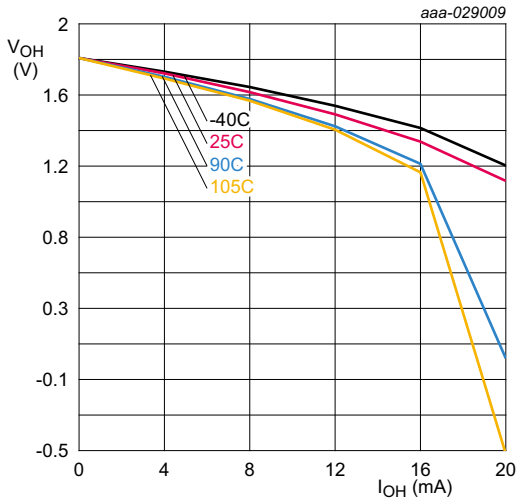
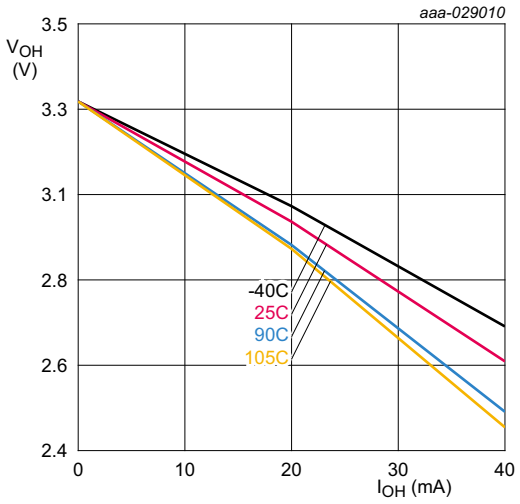


Fig 20. Pin input/output current measurement

12.3.1 Electrical pin characteristics

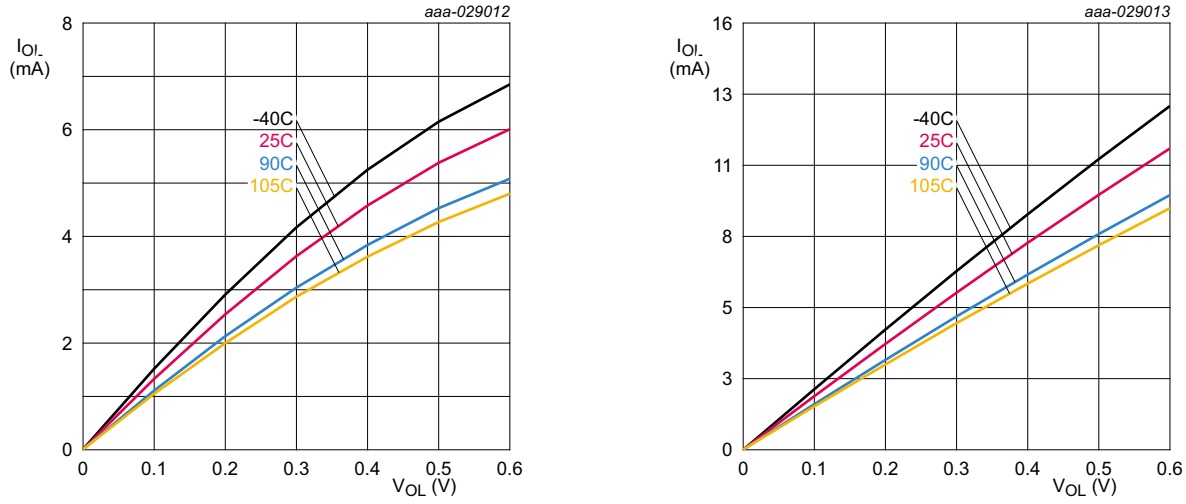


Conditions: V_{DD} = 1.8 V; on pin PIO0_12.



Conditions: V_{DD} = 3.3 V; on pin PIO0_12.

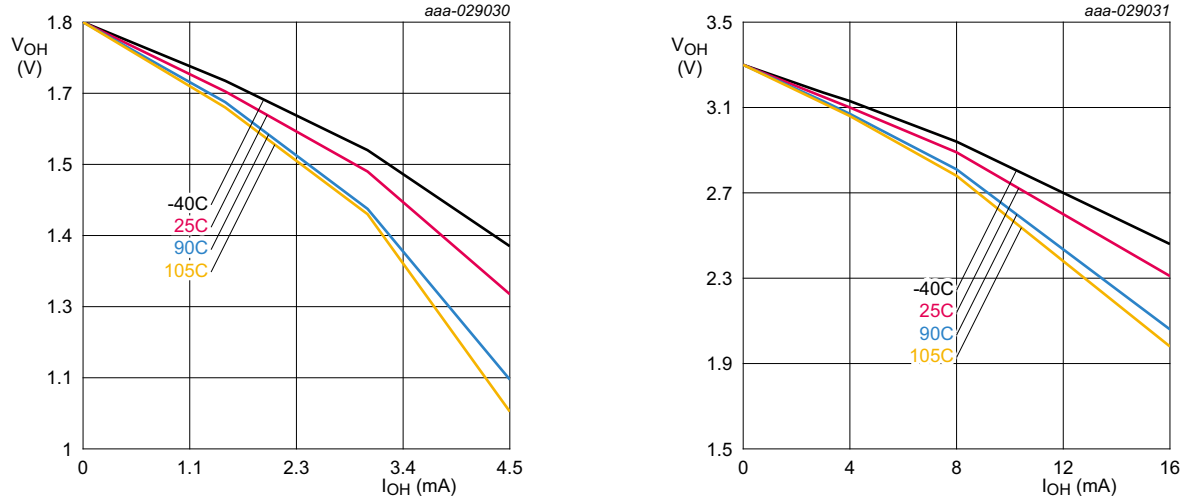
Fig 21. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: V_{DD} = 1.8 V; standard port pins and high-drive pin PIO0_12.

Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_12.

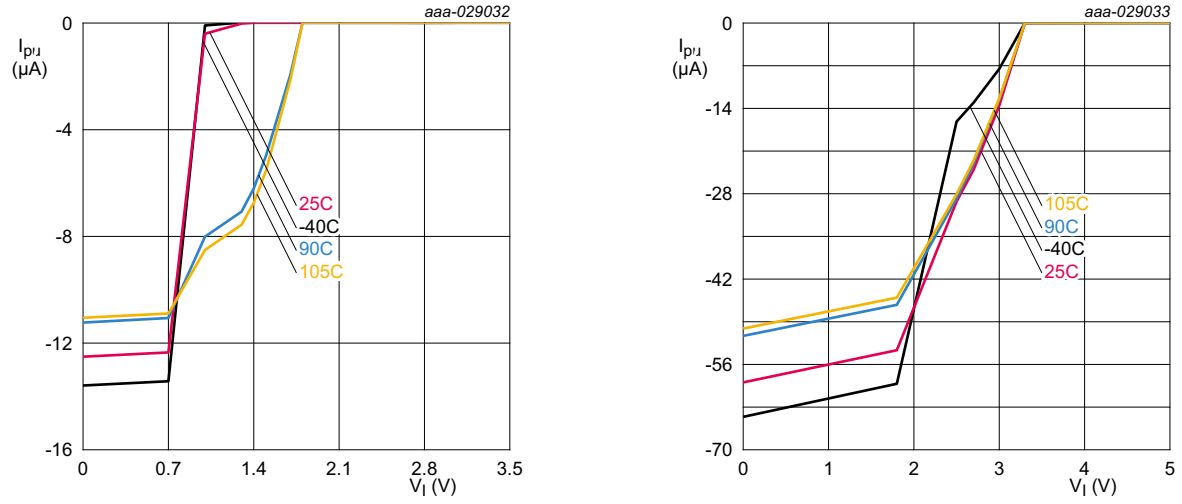
Fig 22. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

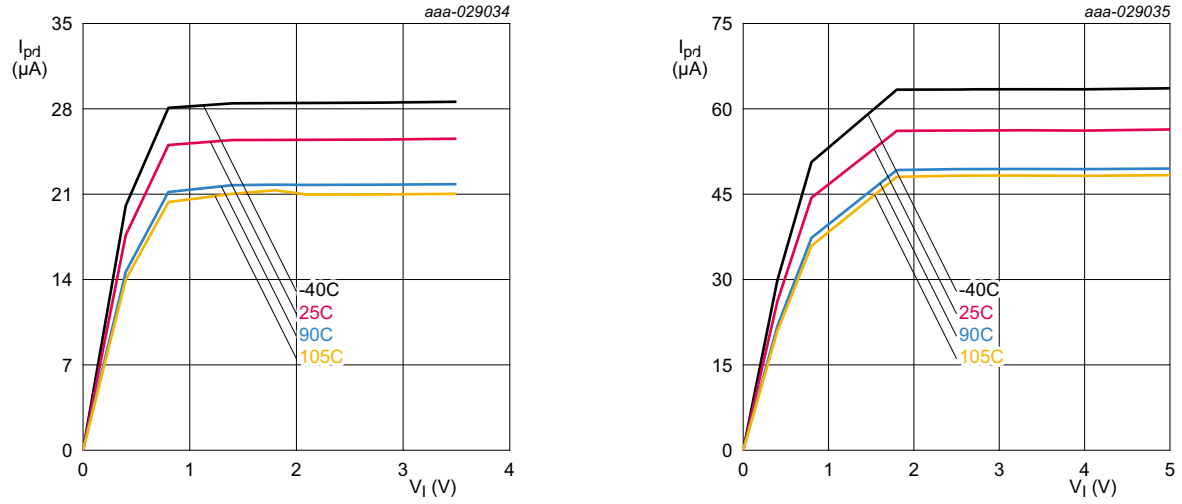
Fig 23. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 24. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 25. Typical pull-down current I_{PD} versus input voltage V_I

13. Dynamic characteristics

13.1 Flash memory (EEPROM based)

Table 15. Flash characteristics

T_{amb} = –40 °C to +105 °C. Based on JEDEC NVM qualification.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	200,000	500,000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		not powered		20	-	-	years
t_{prog}/t_{er}	programming time or erase time	page or multiple consecutive pages, sector or multiple consecutive sectors	[2]	-	2.5	-	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 64 bytes to the flash. T_{amb} <= +85 °C. Flash programming with IAP calls (see *LPC804 user manual*).

13.2 FRO

Table 16. Dynamic characteristic: FRO

T_{amb} = –40 °C to +105 °C; 1.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Min	Typ[1]	Max	Unit
FRO clock frequency; Condition: 0 °C ≤ T_{amb} ≤ 70 °C				
$f_{osc(RC)}$	9 -1 %	9	9 +1 %	MHz
$f_{osc(RC)}$	12 -1 %	12	12 +1 %	MHz
$f_{osc(RC)}$	15 -1 %	15	15 +1 %	MHz
FRO clock frequency; Condition: –20 °C ≤ T_{amb} ≤ 70 °C				
$f_{osc(RC)}$	9 -2 %	9	9 +1 %	MHz
$f_{osc(RC)}$	12 -2 %	12	12 +1 %	MHz
$f_{osc(RC)}$	15 -2 %	15	15 +1 %	MHz
FRO clock frequency; Condition: 70 °C ≤ T_{amb} ≤ 85 °C				
$f_{osc(RC)}$	9 -2 %	9	9 +2 %	MHz
$f_{osc(RC)}$	12 -2 %	12	12 +2 %	MHz
$f_{osc(RC)}$	15 -2 %	15	15 +2 %	MHz
FRO clock frequency; Condition: –40 °C ≤ T_{amb} ≤ 105 °C				
$f_{osc(RC)}$	9 -3.5 %	9	9 +2.5 %	MHz
$f_{osc(RC)}$	12 -3.5 %	12	12 +2.5 %	MHz
$f_{osc(RC)}$	15 -3.5 %	15	15 +2.5 %	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Table 17. Dynamic characteristic: LPOsc

T_{amb} = –40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	LPOsc clock frequency	-		1 -3%	1	1 +3%	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

13.3 I/O pins

Table 18. Dynamic characteristics: I/O pins[1]

T_{amb} = –40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

13.4 WKTCLKIN pin (wake-up clock input)

Table 19. Dynamic characteristics: WKTCLKIN pin

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Max	Unit
f_{clk}	clock frequency	power-down, deep-sleep, and active mode	[1]	-	10	MHz
t_{CHCX}	clock HIGH time	-		50	-	ns
t_{CLCX}	clock LOW time	-		50	-	ns

[1] Assuming a square-wave input clock.

13.5 I²C-bus

Table 20. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
t_f	fall time	[4][5][6]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
$t_{HD;DAT}$	data hold time	[3][4][7]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
$t_{SU;DAT}$	data set-up time	[8][9]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[9] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

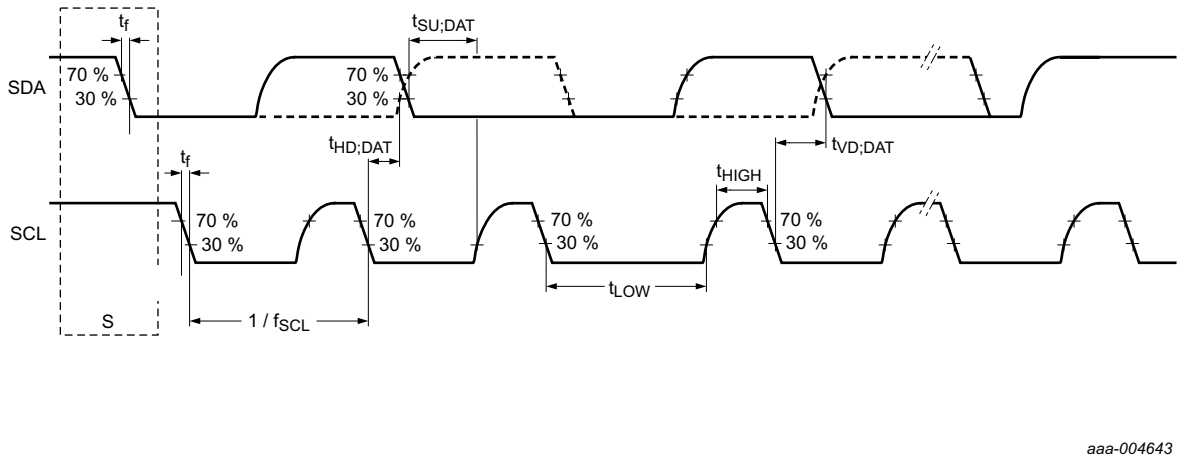


Fig 26. I^2C-bus pins clock timing

13.6 SPI interfaces

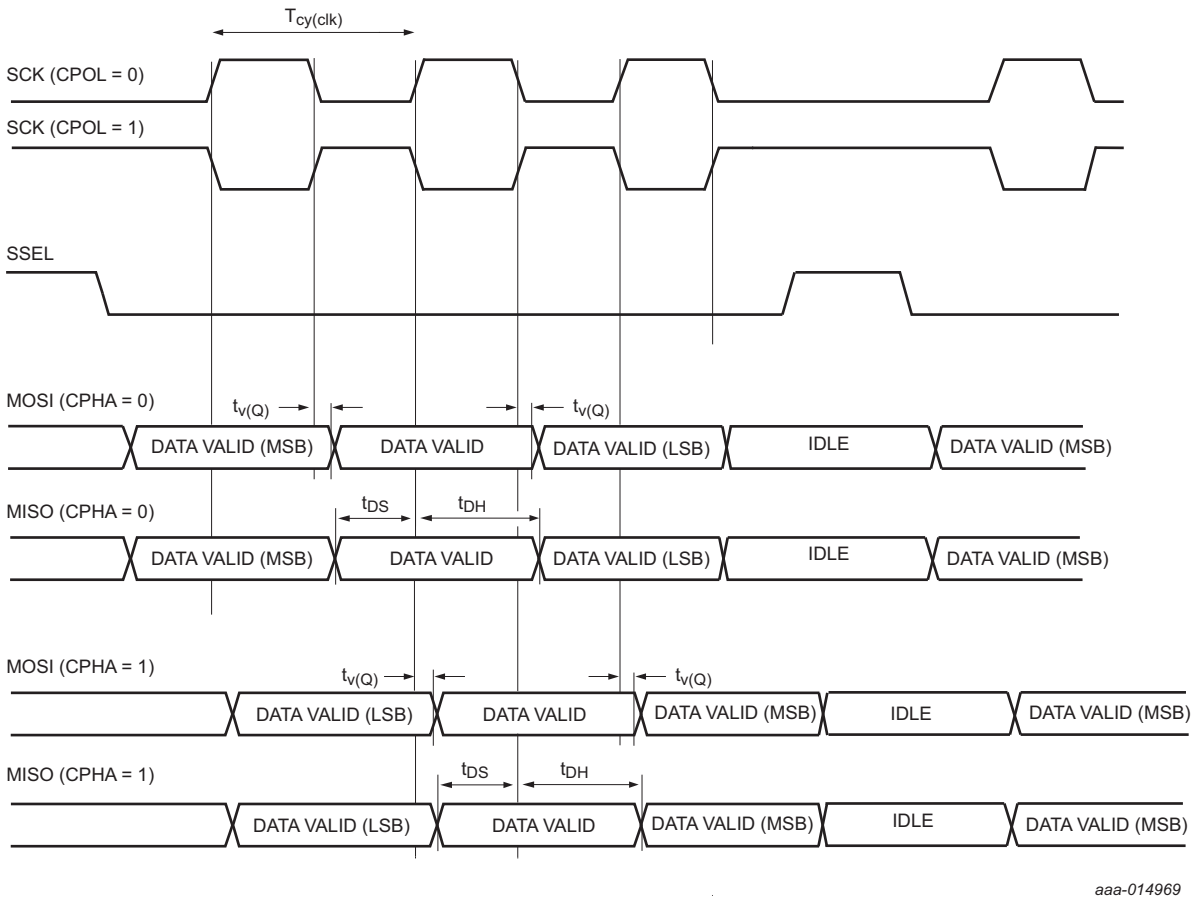
The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 15 Mbit/s, and the maximum supported bit rate for SPI slave mode is 1/(2 x 25 ns) = 20.0 Mbit/s at 3.0v <= VDD <= 3.6v and 1/(2 x 35 ns) = 14.2 Mbit/s at 1.7v <= VDD <= 3.0v.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins.

Table 21. SPI dynamic characteristics

T_{amb} = −40 °C to 105 °C; C_L = 20 pF; input slew = 1 ns. Simulated parameters sampled at the 30 % and 70 % level of the rising or falling edge; values guaranteed by design. Delays introduced by the external trace or external device are not considered.

Symbol	Parameter	Conditions	Min	Max	Unit
SPI master					
t_{DS}	data set-up time	1.71 V <= V_{DD} <= 3.6 V	6	-	ns
t_{DH}	data hold time	1.71 V <= V_{DD} <= 3.6 V	4	-	ns
$t_{v(Q)}$	data output valid time	1.71 V <= V_{DD} <= 3.6 V	0	4	ns
SPI slave					
t_{DS}	data set-up time	1.71 V <= V_{DD} <= 3.6 V	6	-	ns
t_{DH}	data hold time	1.71 V <= V_{DD} <= 3.6 V	4	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	25	ns
		1.71 V <= V_{DD} < 3.0 V	0	35	ns



$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the LPC804 *User manual*.

Fig 27. SPI master timing

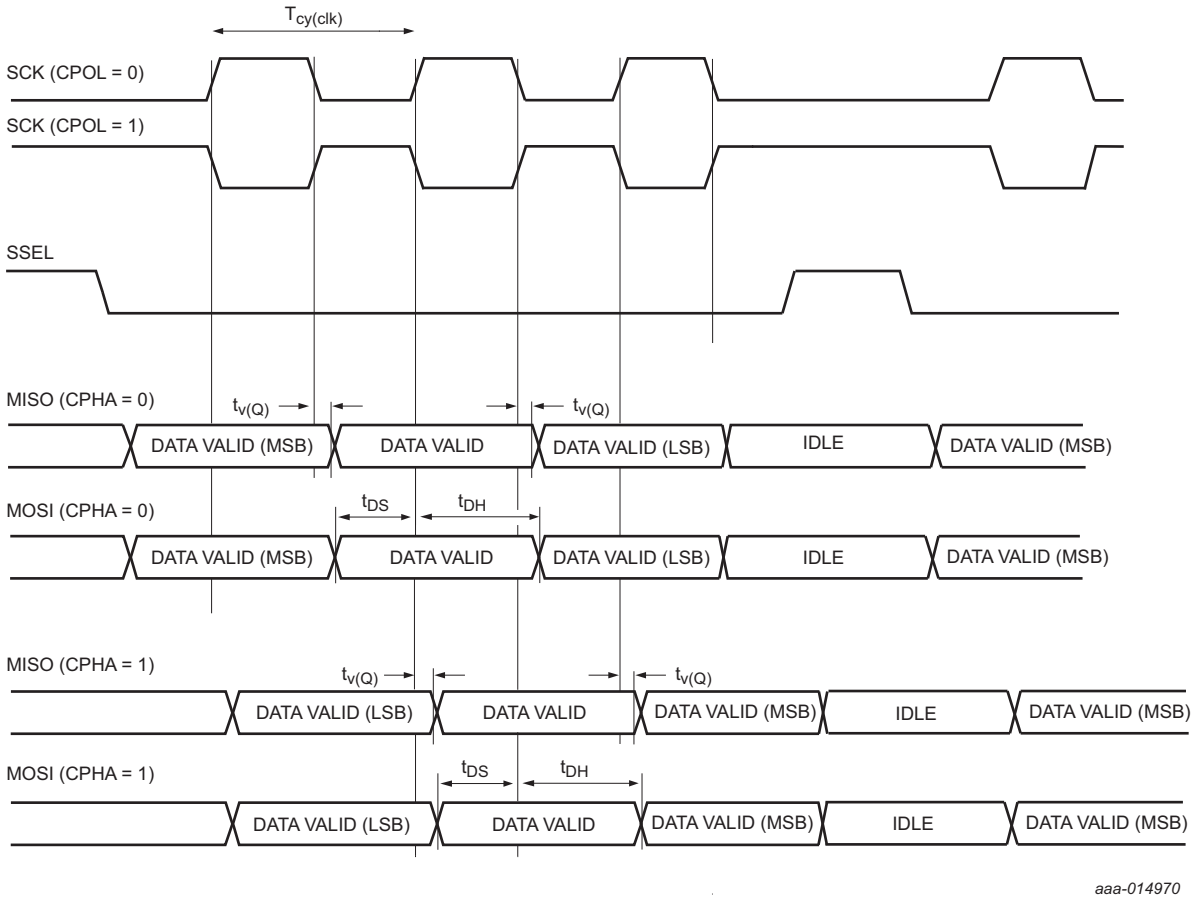


Fig 28. SPI slave timing

13.7 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 10 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 10 Mbit/s.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins

Table 22. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.71 V <= V_{DD} <= 3.6 V unless noted otherwise; C_L = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 30 %/70 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time	3.0 V <= V_{DD} <= 3.6 V	32	-	ns
		1.71 V <= V_{DD} < 3.0 V	38	-	ns
$t_{h(D)}$	data input hold time	3.0 V <= V_{DD} <= 3.6 V	0	-	ns
		1.71 V <= V_{DD} < 3.0 V	0	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	3	ns
		1.71 V <= V_{DD} < 3.0 V	0	4	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time	3.0 V <= V_{DD} <= 3.6 V	5	-	ns
		1.71 V <= V_{DD} < 3.0 V	4	-	ns
$t_{h(D)}$	data input hold time	3.0 V <= V_{DD} <= 3.6 V	6	-	ns
		1.71 V <= V_{DD} < 3.0 V	4	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	31	ns
		1.71 V <= V_{DD} < 3.0 V	0	40	ns

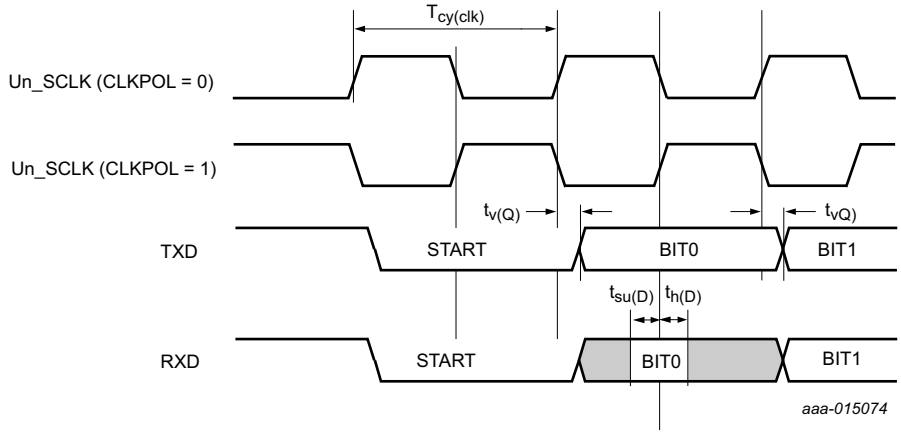


Fig 29. USART timing

13.8 Wake-up process

Table 23. Dynamic characteristic: Typical wake-up times from low power modes

V_{DD} = 3.3 V;T_{amb} = 25 °C; Using FRO (15 MHz) as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	1.97	-	µs
		from deep-sleep mode	[2]	-	2.07	-	µs
		from power-down mode	[2]	-	25	-	µs
		from deep power-down mode	[4]	-	313	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler. ISR is located in SRAM.

[3] FRO enabled, all peripherals off.

[4] Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the Wake-Up pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

14. Characteristics of analog peripherals

14.1 BOD

Table 24. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.24	-	V
		de-assertion		-	2.40	-	V
		interrupt level 2					
		assertion		-	2.52	-	V
		de-assertion		-	2.64	-	V
		interrupt level 3					
		assertion		-	2.81	-	V
		de-assertion		-	2.90	-	V
		reset level 0					
		assertion		-	1.51	-	V
		de-assertion		-	1.54	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC804 *user manual*.

14.2 ADC

Table 25. 12-bit ADC static characteristics

T_{amb} = −25 °C to +105 °C unless noted otherwise; V_{DD} = 2.5 V to 3.6 V; VREFP = V_{DD}; VREFN = V_{SS}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DD}	V
V_{ref}	reference voltage	on pin VREFP		2.5	-	V_{DD}	V
C_{ia}	analog input capacitance			-	-	26	pF
$f_{clk(ADC)}$	ADC clock frequency		[2]	-	-	15	MHz
f_s	sampling frequency		[2]	-	-	480	Ksamples/s
E_D	differential linearity error		[5][4]	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		[6][4]	-	±4	-	LSB
E_O	offset error		[7][4]	-	±3	-	LSB
$V_{err(fs)}$	full-scale error voltage		[8][4]	-	0.1	-	%
Z_i	input impedance	f_s = 480 Ksamples/s	[1][9][10]	0.1	-	-	MΩ

[1] The input resistance of ADC channel 0 is higher than for all other channels. See Figure 30.

[2] In the ADC TRM register, set VRANGE = 0 (default).

[3] In the ADC TRM register, set VRANGE = 1 (default).

[4] Based on characterization. Not tested in production.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 30.

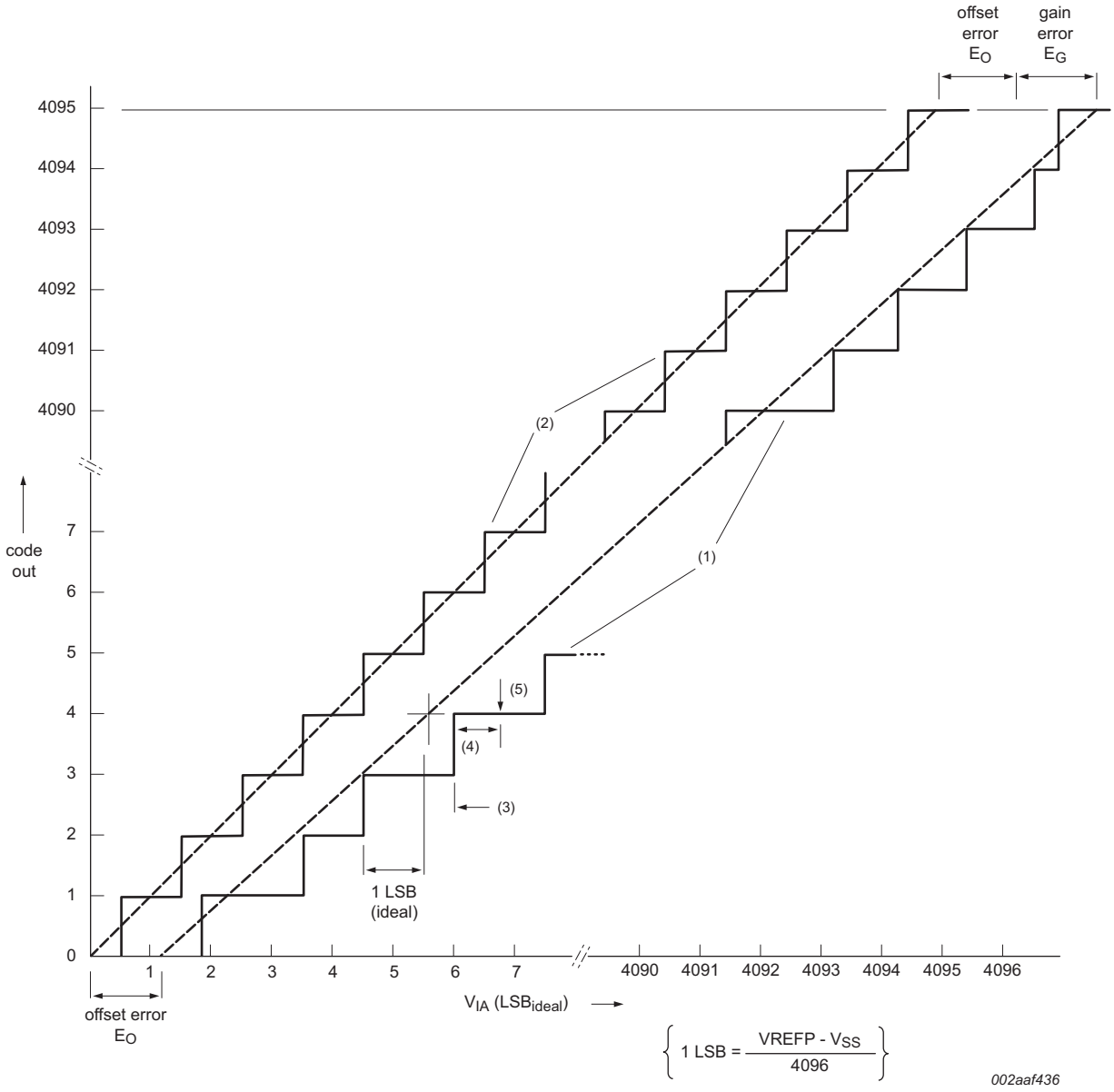
[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 30.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 30. For device revision 1B, typical offset value is ±3 LSB. For device revision 1A, the typical offset value is ±8 LSB.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 30.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 480 Ksamples/s and analog input capacitance C_{ia} = 26 pF.

[10] Input impedance Z_i (see Section 14.2.1) is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 12 for C_{io}.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 30. 12-bit ADC characteristics

14.2.1 ADC input impedance

Figure 31 shows the ADC input impedance. In this figure:

- ADCx represents ADC input channel 0.
- ADCy represents ADC input channels 1 to 11.
- R_1 and R_{sw} are the switch-on resistance on the ADC input channel.
- If ADC input channel 0 is selected, the ADC input signal goes through $R_1 + R_{sw}$ to the sampling capacitor (C_{ia}).
- If ADC input channels 1 to 11 are selected, the ADC input signal goes through R_{sw} to the sampling capacitor (C_{ia}).
- Typical values, R_1 = 5.6 kΩ, R_{sw} = 6.9 kΩ
- To calculate total resistance, use the following equation:
  - $R_{TOTAL} = R_{external} + R_{internal}$
  - $R_{external}$ = External resistance on the ADC input channel.
  - $R_{internal}$ for channel 0 = $R_1 + R_{SW}$ = 12.5 kΩ.
  - $R_{internal}$ for channels 1 to 11 = 6.9 kΩ.
- See Table 11 for C_{io}.
- See Table 25 for C_{ia}.

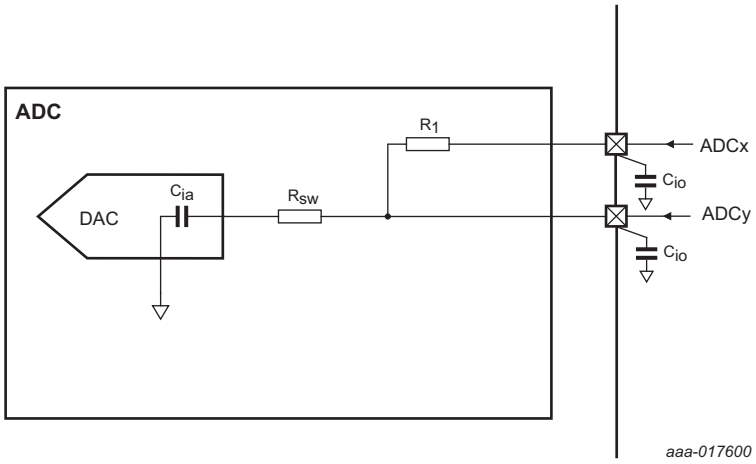


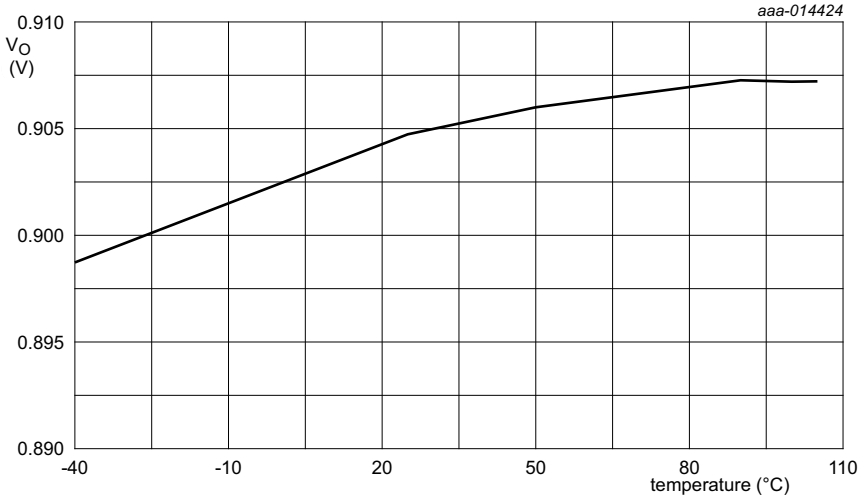
Fig 31. ADC input impedance

14.3 Comparator and internal voltage reference

Table 26. Internal voltage reference static and dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 3.3 V; hysteresis disabled in the comparator CTRL register.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = 25 °C to 105°C		860	-	940	mV
		T_{amb} = 25 °C			904		mV



V_{DD} = 3.3 V; characterized through bench measurements on typical samples.

Fig 32. Typical internal voltage reference output voltage

Table 27. Comparator characteristics

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = 1.71 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{ref(cmp)}$	comparator reference voltage	pin ACMPV_{REF}		1.5	-	3.6	V
I_{DD}	supply current	VP > VM; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	90	-	µA
		VM > VP; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	60	-	µA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_O	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V; V_{DD} = 3.0 V	[2]	-	4	-	mV
		V_{IC} = 1.5 V; V_{DD} = 3.0 V	[2]	-	6	-	mV
		V_{IC} = 2.9 V; V_{DD} = 3.0V	[2]	-	6	-	mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process; V_{DD} = 3.3 V; T_{amb} = 25 °C		-	13	-	µs

Table 27. Comparator characteristics *...continued*

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = 1.71 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 3.0 V; T_{amb} = 105 °C			320		
		V_{IC} = 0.1 V; 100 mV overdrive input	[1][2][4]	-		-	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1][2]	-	260	-	ns
		V_{IC} = 1.5 V; 100 mV overdrive input	[1][2][4]	-	300	-	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1][2]	-	160	-	ns
		V_{IC} = 2.9 V; 100 mV overdrive input	[1][2][4]	-	400	-	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1][2]	-	80	-	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DD} = 3.0 V; T_{amb} = 105 °C			170		
		V_{IC} = 0.1 V; 100 mV overdrive input	[1][2][4]	-		-	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1][2]	-	80	-	ns
		V_{IC} = 1.5 V; 100 mV overdrive input	[1][2][4]	-	120	-	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1][2]	-	220	-	ns
		V_{IC} = 2.9 V; 100 mV overdrive input	[1][2][4]	-	160	-	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1][2]	-	320	-	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V; T_{amb} = 105 °C; settings:	[3]	-	6	-	
		5 mV					mV
		10 mV		-	11	-	mV
		20 mV		-	21	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V; T_{amb} = 105 °C; settings:	[1][3]		11		
		5 mV		-		-	mV
		10 mV		-	18	-	mV
		20 mV		-	30	-	mV
R_{lad}	ladder resistance	-		-	1	-	MΩ

[1] C_L = 10 pF

[2] Characterized on typical samples, not tested in production.

[3] Input hysteresis is relative to the reference input channel and is software programmable.

[4] 100 mV overdrive corresponds to a square wave from 50 mV below the reference (V_{IC}) to 50 mV above the reference.

Table 28. Comparator voltage ladder dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	17	-	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1]	-	18	-	µs

[1] Characterized on typical samples, not tested in production.

Table 29. Comparator voltage ladder reference static characteristics

V_{DD} = 1.8 V to 3.6 V. T_{amb} = -40 °C to + 105°C; external or internal reference.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$E_{V(O)}$	output voltage error	decimal code = 00	[2]	-	±6	-	mV
		decimal code = 08		-	±1	-	%
		decimal code = 16		-	±1	-	%
		decimal code = 24		-	±1	-	%
		decimal code = 30		-	±1	-	%
		decimal code = 31		-	±1	-	%

[1] Characterized though limited samples. Not tested in production.

[2] All peripherals except comparator, temperature sensor, and FRO turned off.

14.4 DAC

Table 30. 10-bit DAC electrical characteristics

$V_{DD} = V_{DDA}$ = 2.7 V to 3.6 V; T_{amb} = –40 °C to +105 °C unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
E_D	differential linearity error	[1][2]	-	0.4	-	LSB
$E_{L(adj)}$	integral non-linearity	[1][2]	-	6.0	-	LSB
E_O	offset error	[1][2]	-	±57.0	-	mV
E_G	gain error	[1][2]	-	±36.0	-	mV
C_L	load capacitance		-	200	-	pF
R_{OUT}	PIO0_19/DACOUT_0 pin resistance	[3]	-	90	200	Ω
V_{OUT}	Output voltage range		0.175	-	V_{DDA}-0.175	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C) and $V_{DD} = V_{DDA}$ = 3.6 V.

[2] Characterized through bench measurements, not tested in production.

[3] DAC output voltage depends on the voltage divider ratio of the R_{OUT} and external load resistance.

15. Application information

15.1 Start-up behavior

Figure 33 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

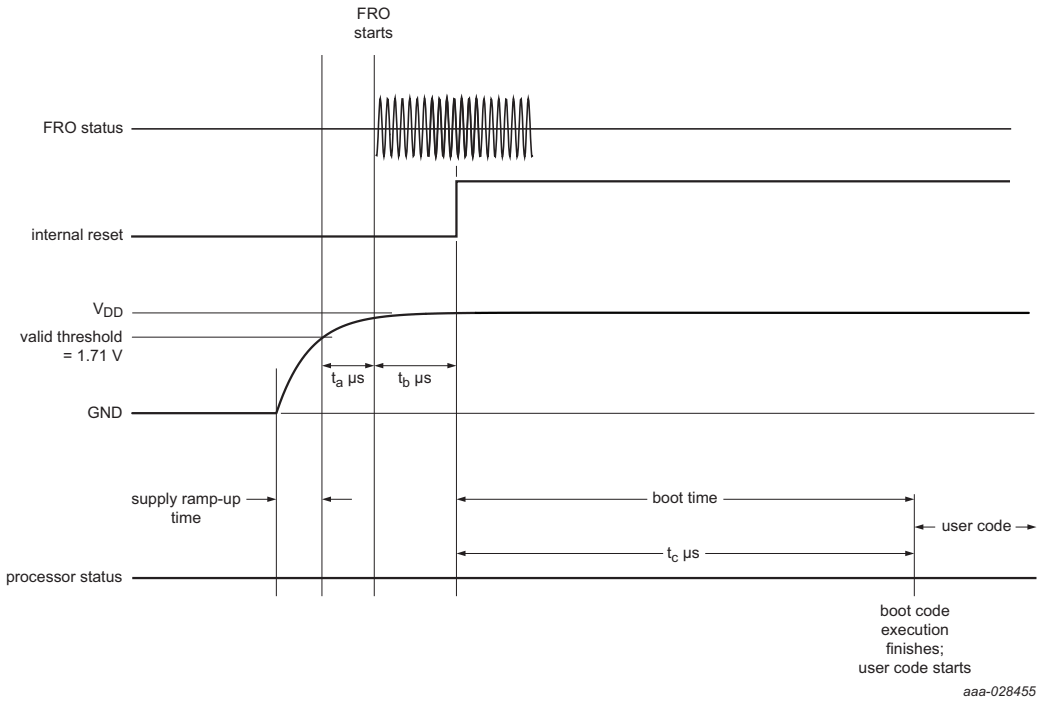


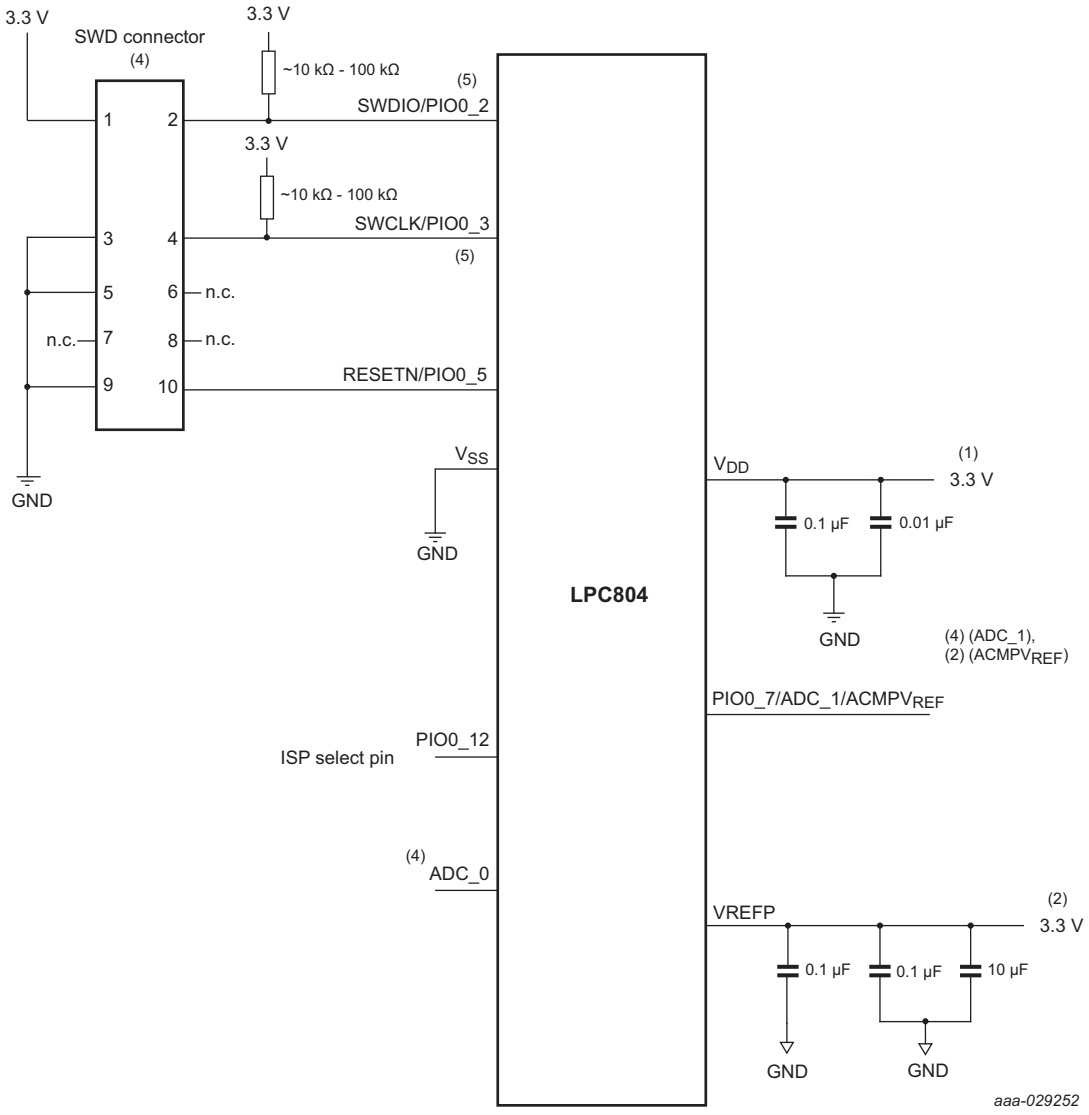
Fig 33. Start-up timing

Table 31. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 26 µs
t_b	Internal reset de-asserted	101 µs
t_c	Boot time	36 µs

15.2 Connecting power, clocks, and debug functions

Figure 34 shows the basic board connections used to power the LPC804 and provide debug capabilities via the serial wire port.



(1) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(2) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DD} pins. The 10 µF bypass capacitor filters the power line. Tie VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(3) Uses the Arm 10-pin interface for SWD.

(4) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 4.

(5) External pull-up resistors on SWDIO and SWCLK pins are optional because these pins have an internal pull-up enabled by default.

Fig 34. Power, clock, and debug connections

15.3 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 14 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 14, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 14 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

15.4 Termination of unused pins

Table 32 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 32. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
all PIOn_m	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
VREFP	-	Tie to VDD.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

15.5 Pin states in different power modes

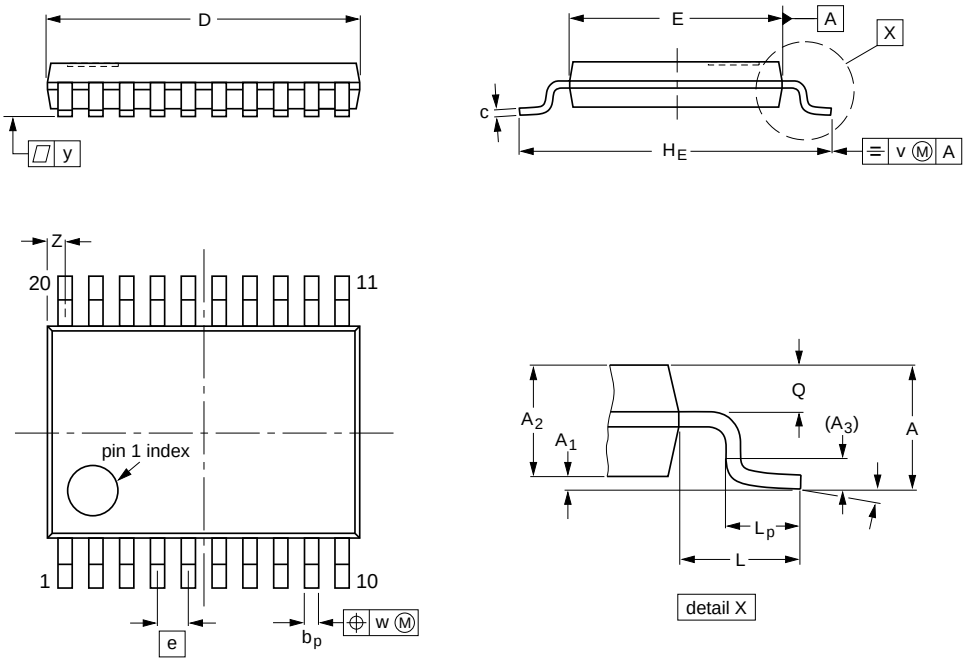
Table 33. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/power-down	Deep power-down
PIOn_m pins	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

16. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

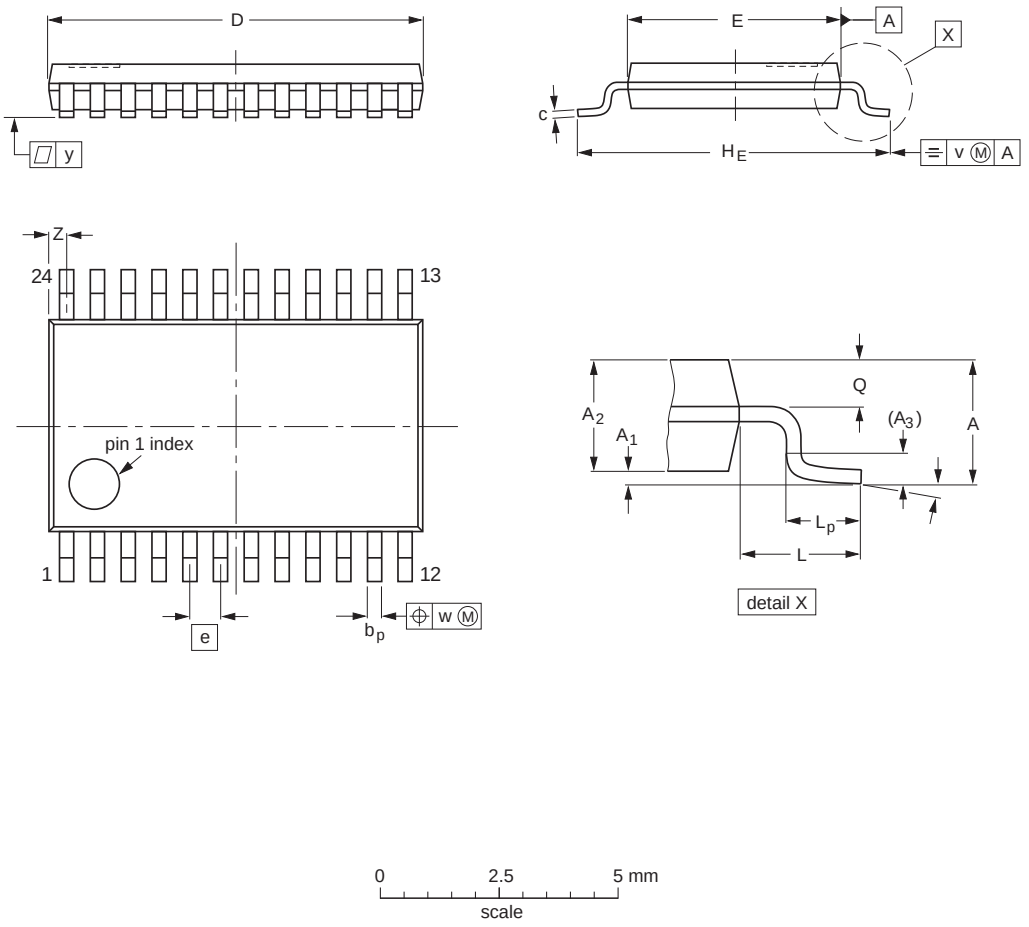
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 35. Package outline SOT360-1 (TSSOP20)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

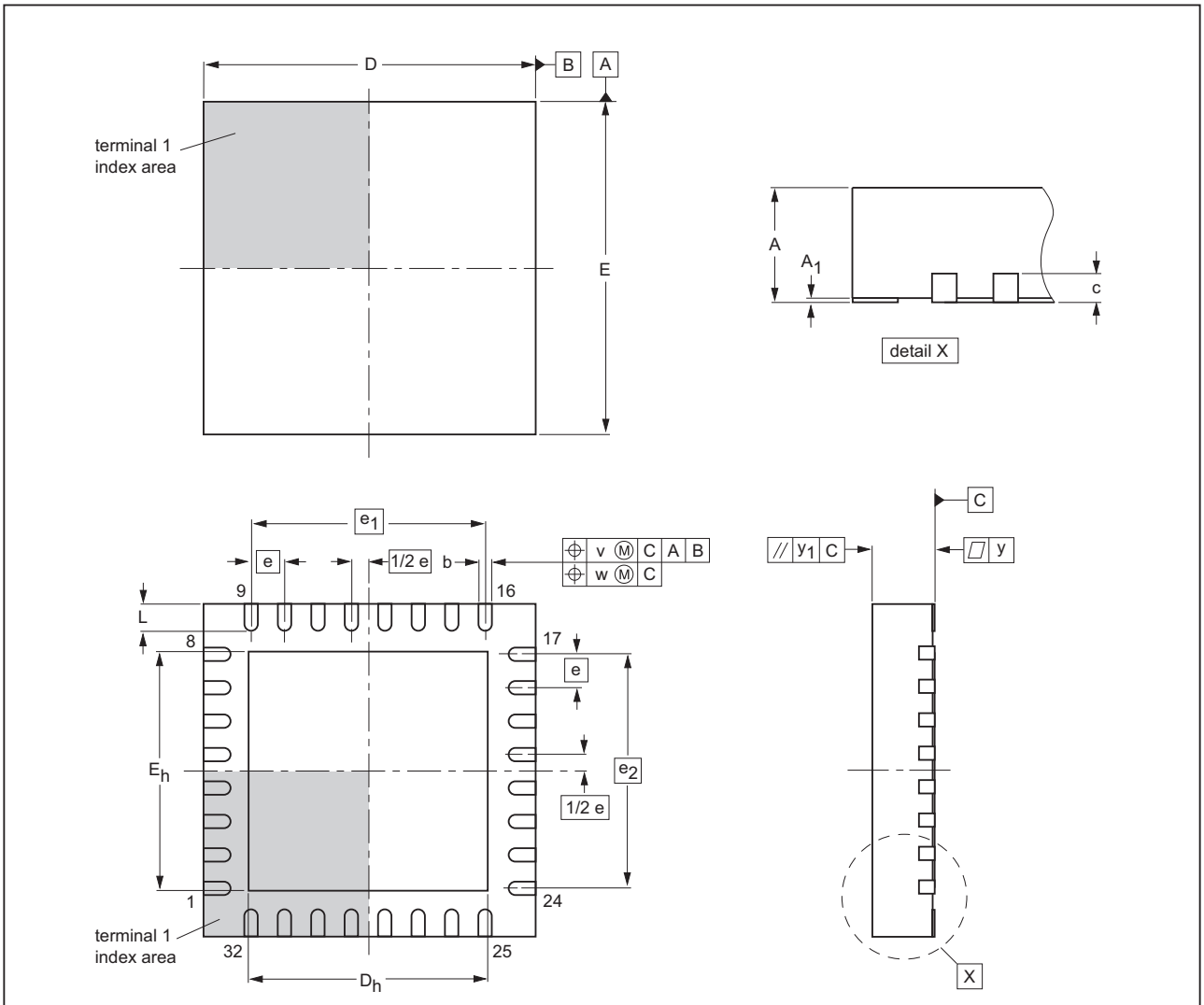
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 36. Package outline SOT355-1 (TSSOP24)

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

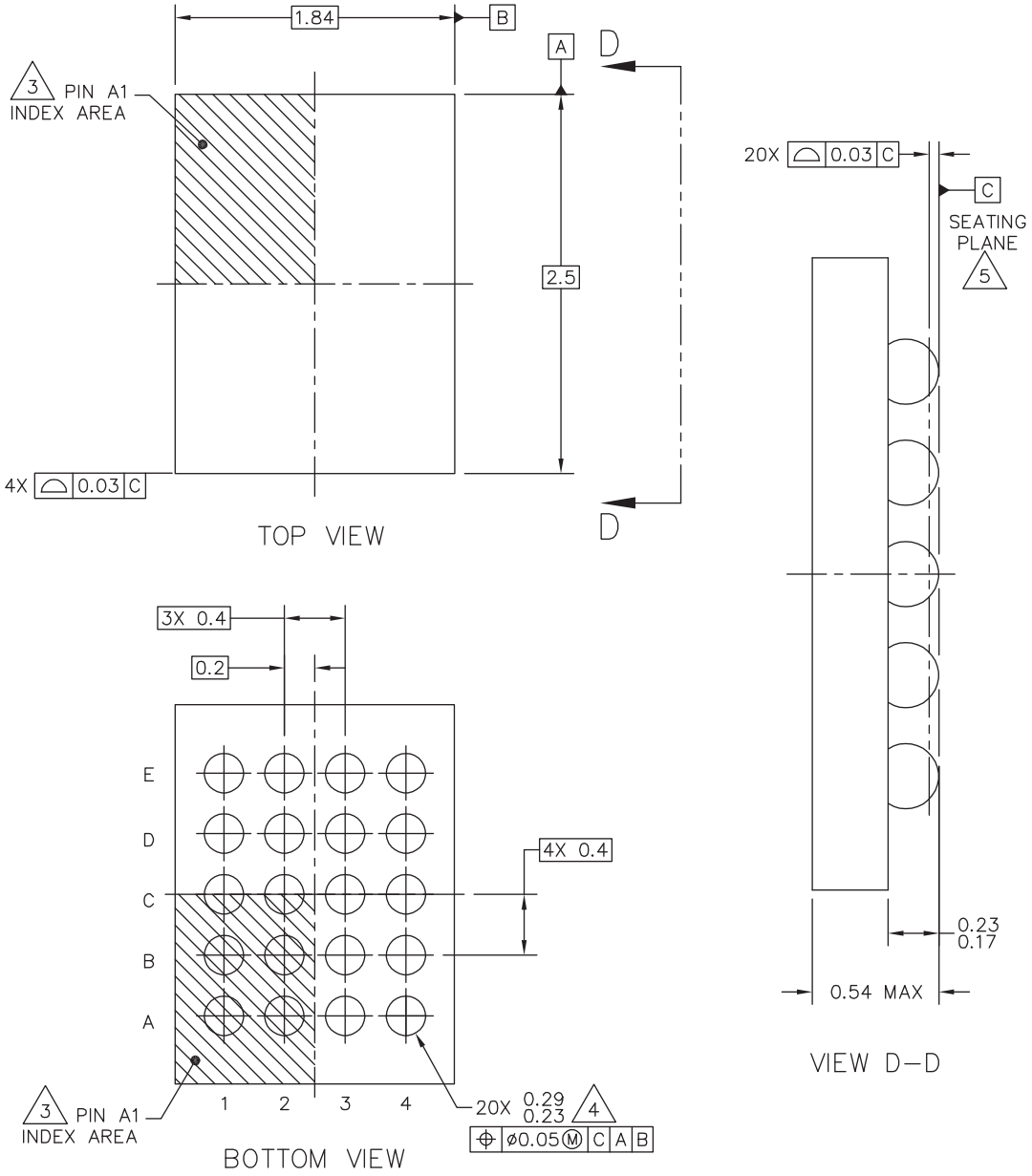
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 37. Package outline HVQFN33 (5 x 5 x 0.85 mm)



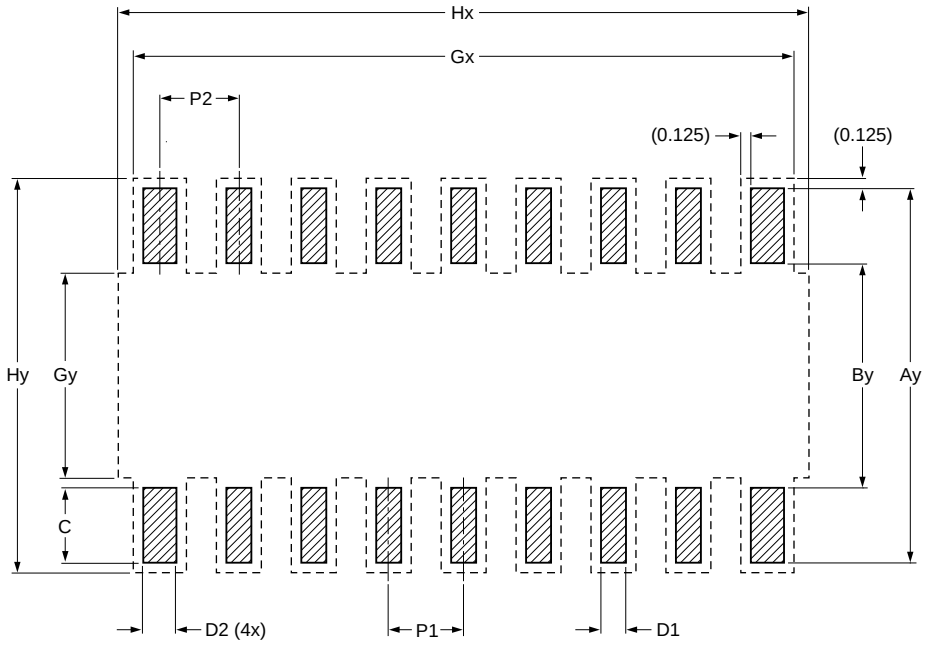
DATE: 24 MAY 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01253D	REVISION: O	

Fig 38. Package outline WLCSP20 (2.50 × 1.84 × 0.5 mm)

17. Soldering

Footprint information for reflow soldering of TSSOP20 package **SOT360-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

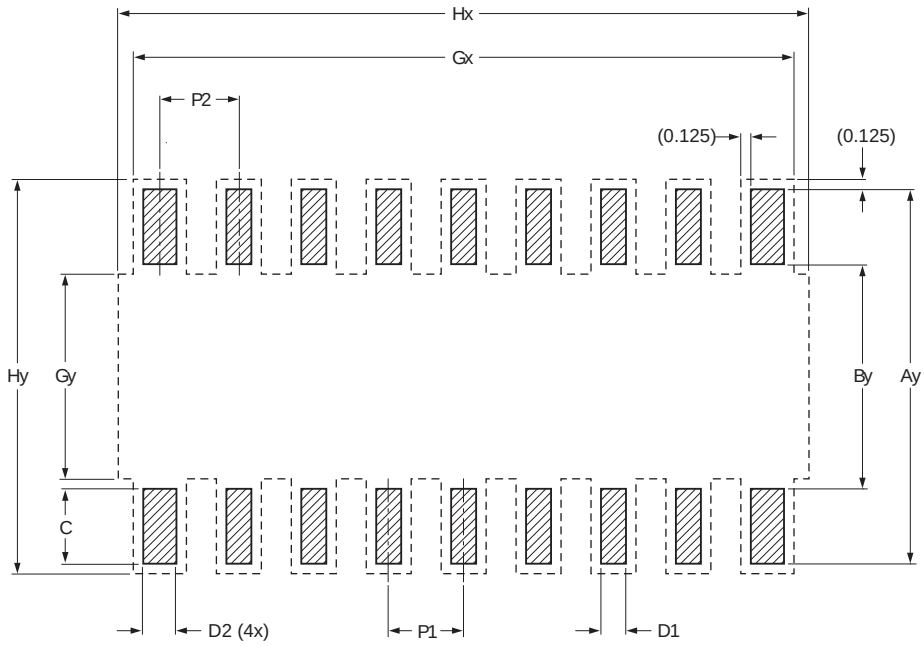
DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

sot360-1_fr

Fig 39. Reflow soldering of the TSSOP20 package

Footprint information for re ow soldering of TSSOP24 package **SOT355-**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

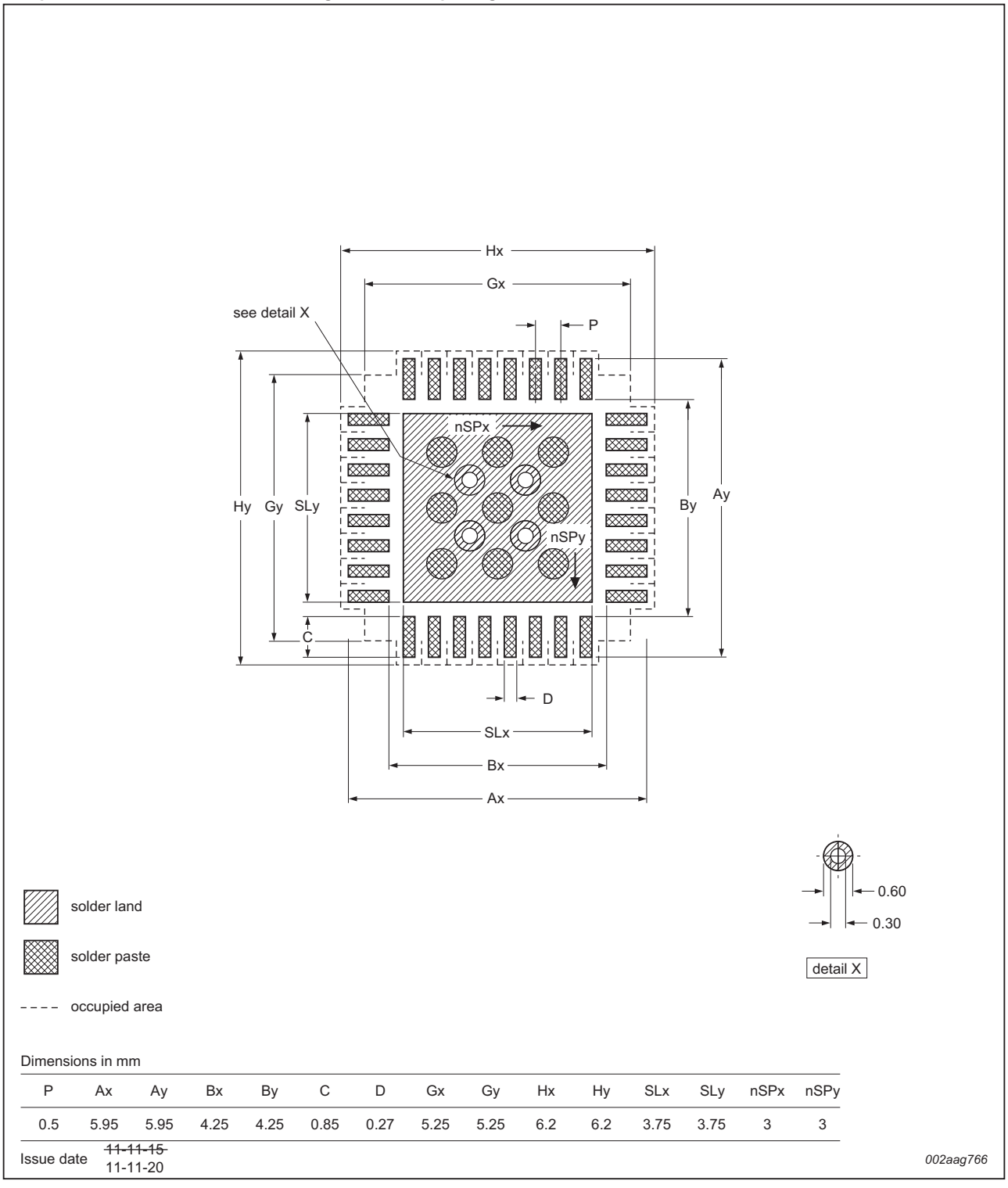
DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	8.200	5.300	8.600	7.450

sot355-1_fr

Fig 40. Reflow soldering of the TSSOP24 package

Footprint information for reflow soldering of HVQFN33 package



Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

Fig 41. Reflow soldering for the HVQFN33 (5x5) package

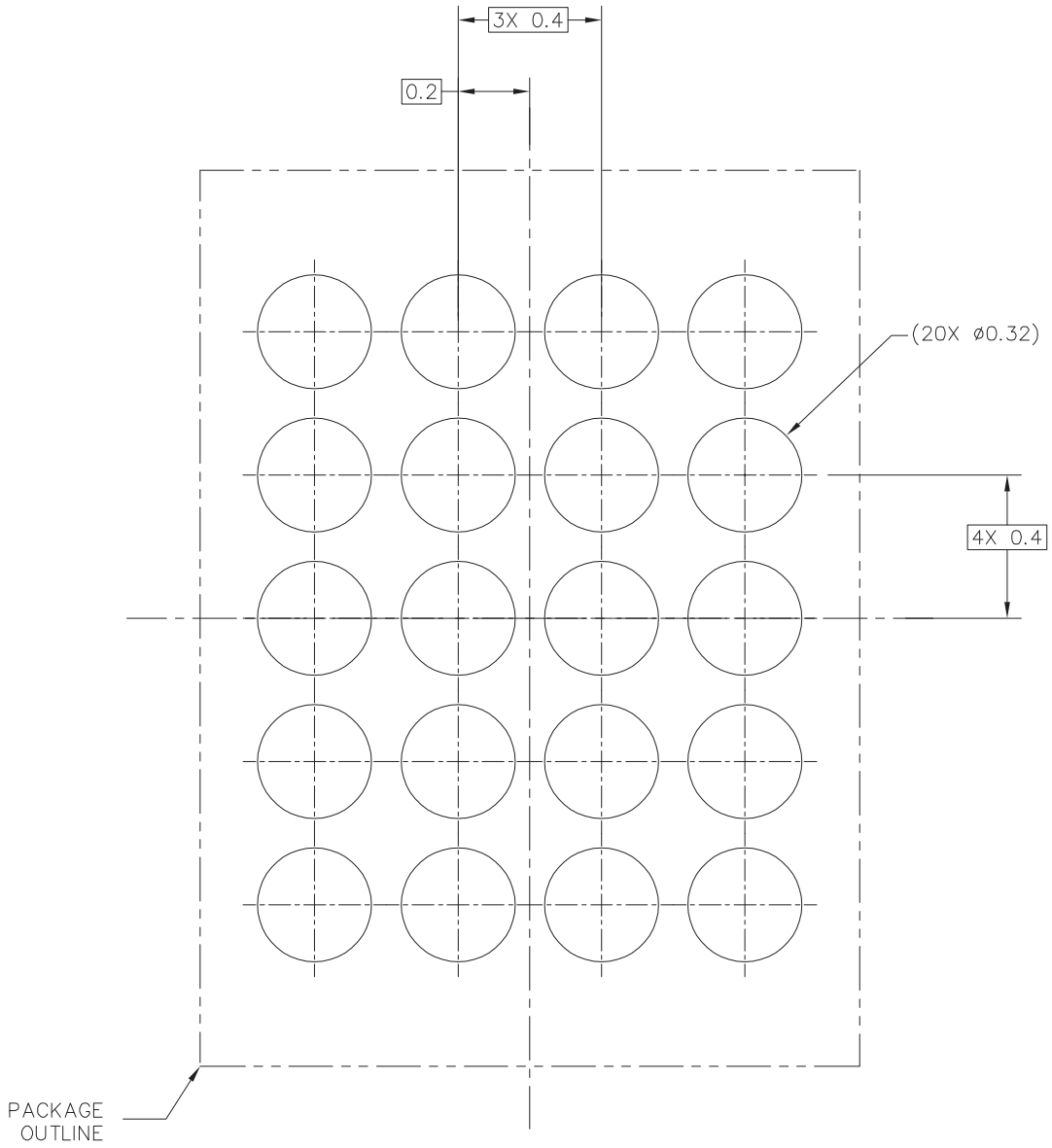


Fig 42. Reflow soldering for the WLCSP20 package (1 of 3)

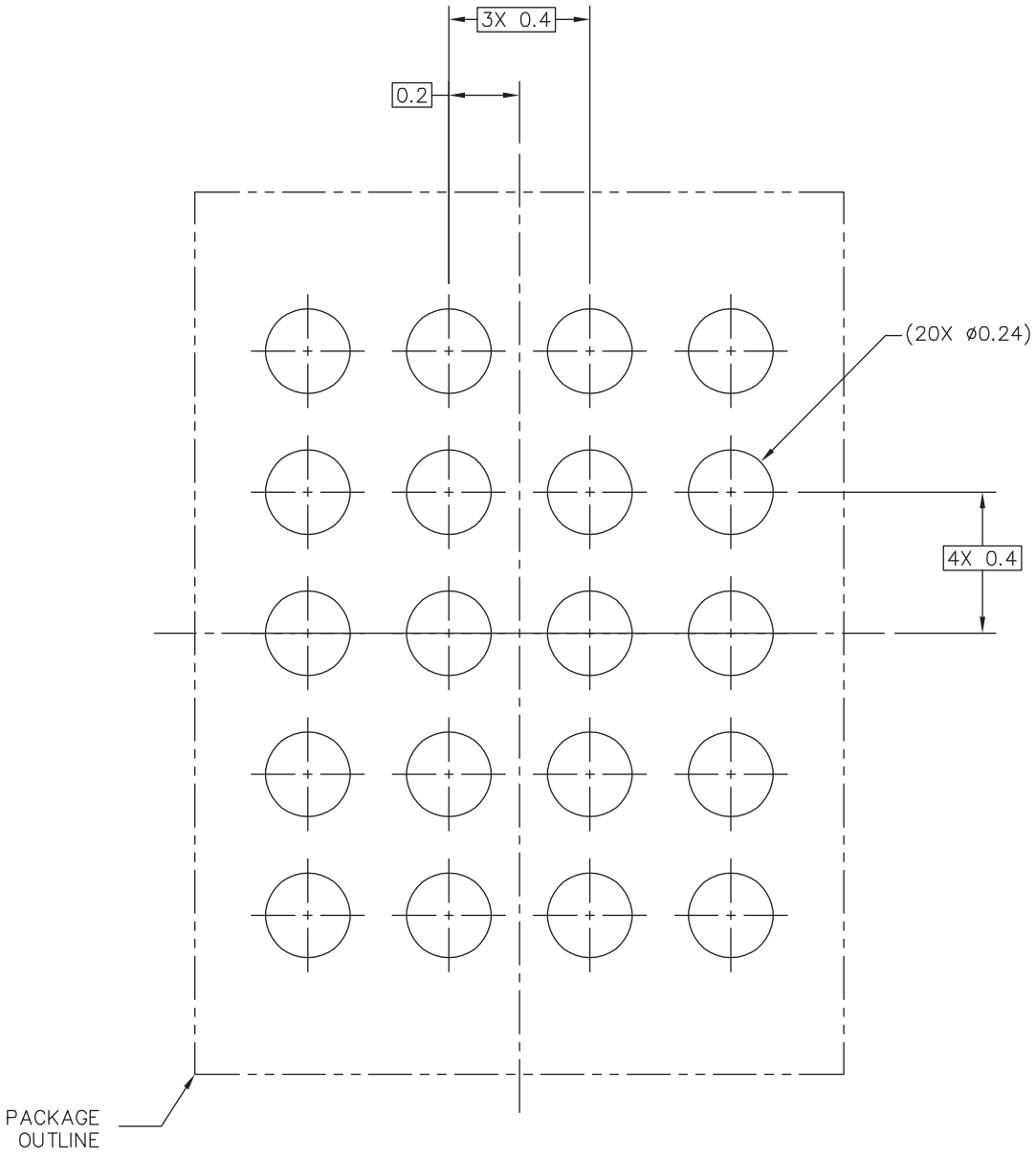


Fig 43. Reflow soldering for the WLCSP20 package (2 of 3)

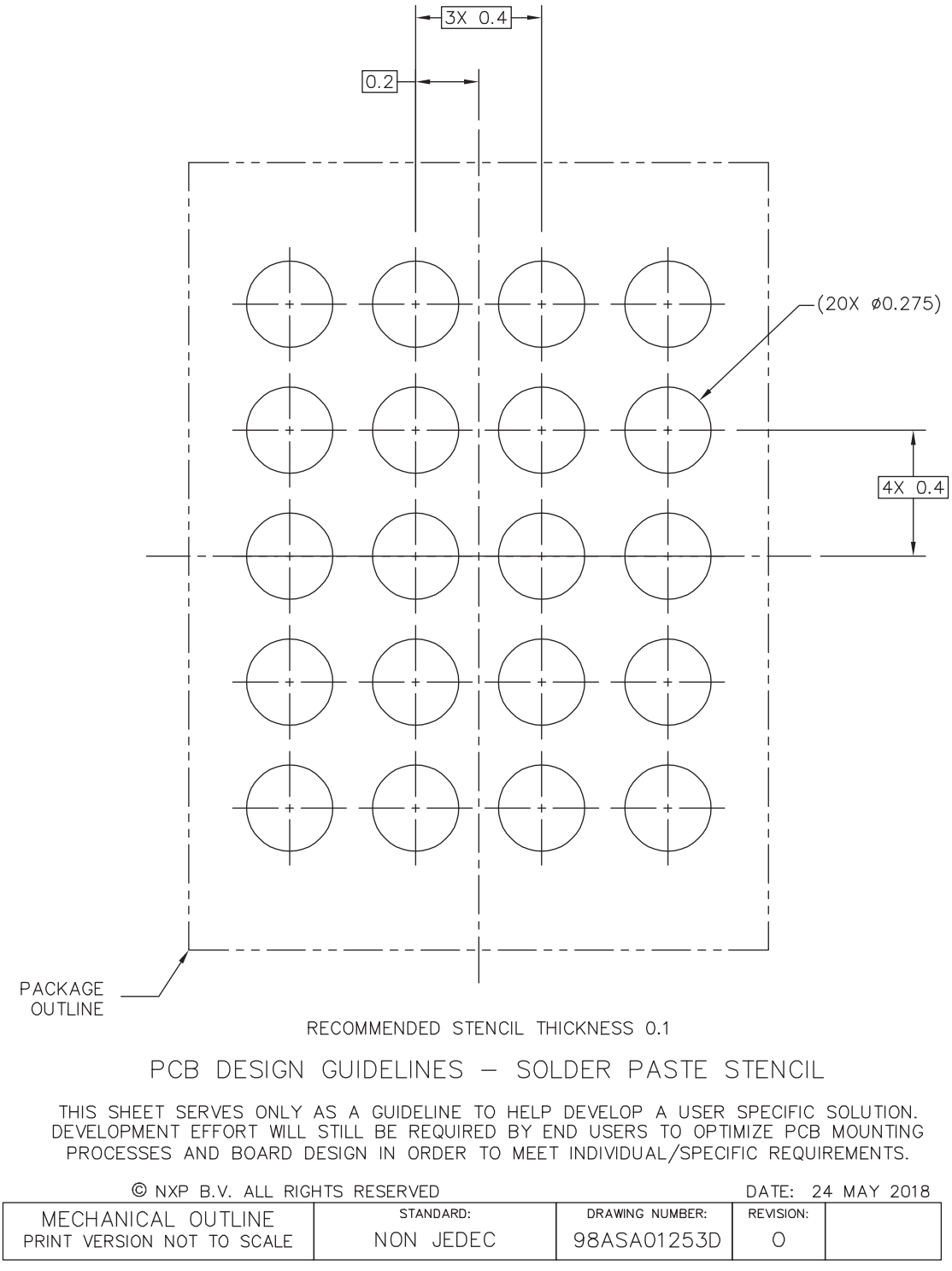


Fig 44. Reflow soldering for the WLCSP20 package (3 of 3)

18. Abbreviations

Table 34. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

19. References

[1] LPC804 User manual UM11065:

[2] LPC804 Errata sheet:

[3] I2C-bus specification *UM10204*.

[4] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

20. Revision history

Table 35. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC804 v.1.8	20210318	Product data sheet	-	LPC804 v.1.7
	Updated Table 4 “Pin description” .			
	Updated Figure 12 “LPC804 clock generation”.			
LPC804 v.1.7	20200904	Product data sheet	-	LPC804 v.1.6
	Updated Table 9 “Limiting values” and Table 10 “Thermal resistance” to include WLCSP20 data.			
LPC804 v.1.6	20200513	Product data sheet	-	LPC804 v.1.5
	Updated Device revision table to include revision identifier 1C.			
LPC804 v.1.5	20190630	Product data sheet	-	LPC804 v.1.4
	Updated Table 16 “Dynamic characteristic: FRO”. to include spec for Temp = 70 C to 85 C			
LPC804 v.1.4	20180712	Product data sheet	201804020F01	LPC804 v.1.3
	• Added LPC804UK device. • Updated Section 5 “Marking”. • Updated Table 25 “12-bit ADC static characteristics”: Changed typical offset error ($E_{O)}$ to ±3 LSB. Added table note text: For device revision 1B, typical offset value is ±3 LSB. For device revision 1A, the typical offset value is ±8 LSB. • Updated Section 9.25.1 “Internal oscillators”. Changed heading title. • Updated Section 15.2 “Connecting power, clocks, and debug functions”: removed text: connect the external crystal.			
LPC804 v.1.3	20180323	Product data sheet	-	LPC804 v.1.2
Modifications:	• Fixed revision number. • Updated Table 15 “Flash characteristics”. t_{er} consolidated to t_{prog}/t_{er}. • Updated Section 9.25.4.4 “Deep power-down mode” with text: Five general-purpose registers are available to store information during deep power-down mode.			
LPC804 v.1.2	20180227	Product data sheet	-	LPC804 v.1.1
Modifications:	• Updated Table 12 “Static characteristics, supply pins”: Added condition: system clock = 1 MHz, V_{DD} = 3.3 V. • Updated Table 16 “Dynamic characteristic: FRO”: Max values: FRO clock frequency; Condition: –20 °C ≤ T_{amb} ≤ 70 °C and FRO clock frequency; Condition: –40 °C ≤ T_{amb} ≤ 105 °C. • Updated title of Section 13.1 “Flash memory (EEPROM based)”.			
LPC804 v.1.1	20180214	Product data sheet	-	LPC804 v.1
Modifications:	• Updated Section 2 “Features and benefits”. • Updated Table 5 “Movable functions (assign to pins PIO0_0 to PIO0_5, PIO0_7 to PIO0_30 through switch matrix)”. • Added level shifter functionality to Section 9.8 “I/O configuration”. • Updated Table 16 “Dynamic characteristic: FRO”: Changed frequencies to 9 MHz, 12 MHz, and 15 MHz. Added Condition: –20 °C ≤ T_{amb} ≤ 70 °C and Condition: –40 °C ≤ T_{amb} ≤ 70 °C.			
LPC804 v.1	20180126	Product data sheet	-	-

23. Contents

continued >>

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Document identifier: LPC804

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Table continues on the next page...

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