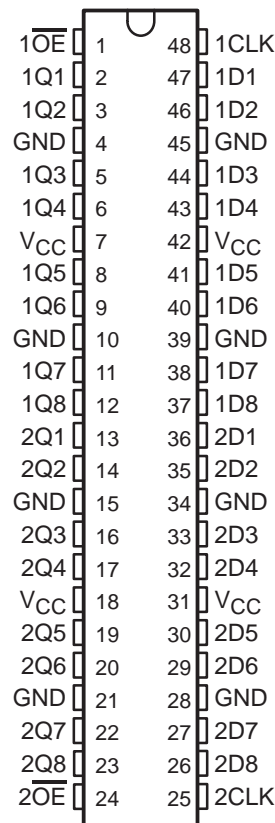


SN54ACT16374, 74ACT16374 16-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus*™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Bus-Driving True Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Distributed Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

SN54ACT16374 . . . WD PACKAGE
74ACT16374 . . . DL PACKAGE
(TOP VIEW)



description

The SN54ACT16374 and 74ACT16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

An output-enable input (\overline{OE}) can be used to place the outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state provides the capability to drive bus lines in a bus-organized system without need for interface or pullup components. \overline{OE} does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16374 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit board area.

The SN54ACT16374 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT16374 is characterized for operation from -40°C to 85°C .



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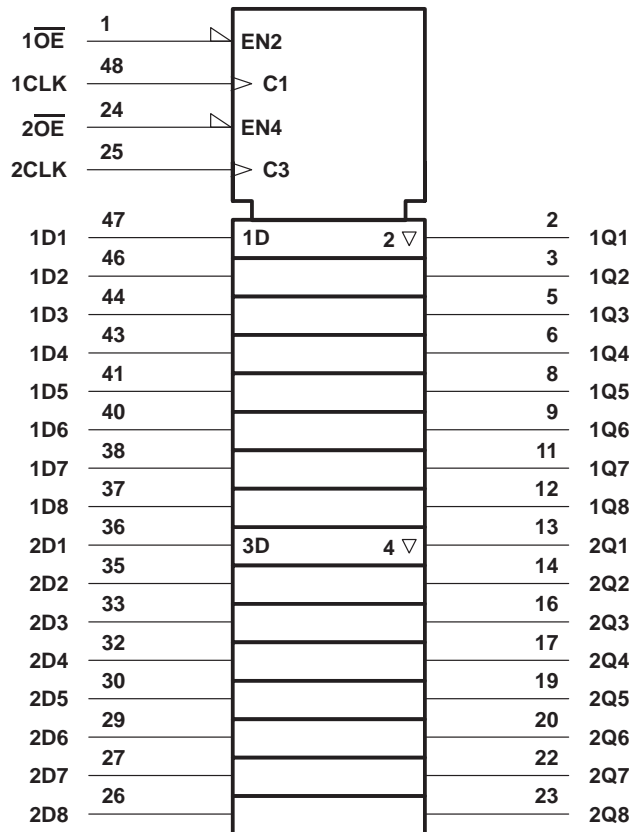
SN54ACT16374, 74ACT16374 16-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS124B – MARCH 1990 – REVISED APRIL 1996

FUNCTION TABLE
(each section)

INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†

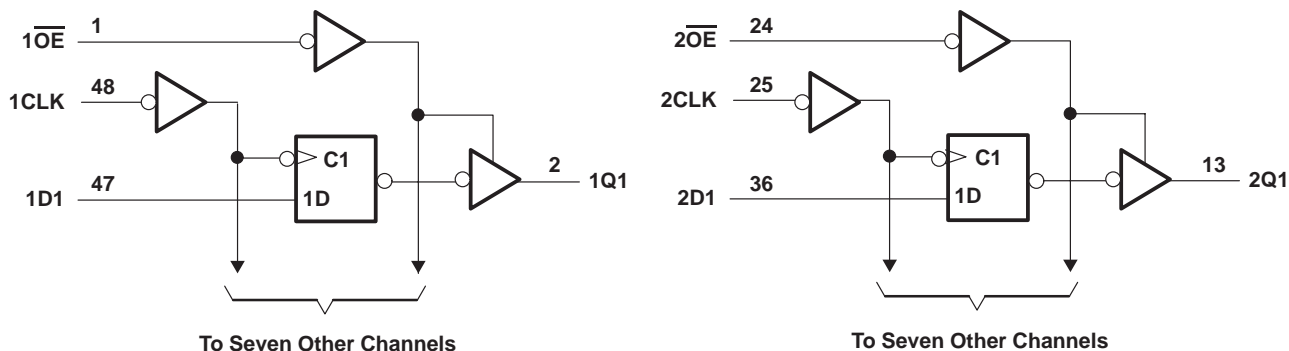


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ACT16374, 74ACT16374 16-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS124B – MARCH 1990 – REVISED APRIL 1996

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 400 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.2 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

	SN54ACT16374			74ACT16374			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage (see Note 4)	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_I Input voltage	0	V_{CC}		0	V_{CC}		V
V_O Output voltage	0	V_{CC}		0	V_{CC}		V
I_{OH} High-level output current			-24			-24	mA
I_{OL} Low-level output current			24			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0	10		0	10		ns/V
T_A Operating free-air temperature	-55	125		-40	85		$^\circ\text{C}$

- NOTES: 3. Unused inputs must be held high or low to prevent them from floating.
4. All V_{CC} and GND pins must be connected to the proper voltage supply.

SN54ACT16374, 74ACT16374
16-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCAS124B – MARCH 1990 – REVISED APRIL 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT16374		74ACT16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4	V	
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
I _{OH} = -75 mA [†]	5.5 V						3.85			
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1	0.1	V	
		5.5 V			0.1		0.1	0.1		
	I _{OL} = 24 mA	4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	I _{OL} = 50 mA [†]	5.5 V					1.65			
I _{OL} = 75 mA [†]	5.5 V						1.65			
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10	±5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160	80	μA	
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1	1	mA	
C _i	V _I = V _{CC} or GND	5 V			4.5				pF	
C _o	V _O = V _{CC} or GND	5 V			12				pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54ACT16374		74ACT16374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	65	0	65	0	65	MHz
t _w	Pulse duration	CLK low	7.5		7.5		7.5	ns
		CLK high	4.5		4.5		4.5	
t _{su}	Setup time, data before CLK [↑]	6.5		6.5		6.5	ns	
t _h	Hold time, data after CLK [↑]	1		1		1	ns	



SN54ACT16374, 74ACT16374
16-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCAS124B – MARCH 1990 – REVISED APRIL 1996

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			SN54ACT16374		74ACT16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			65			65		65		MHz
t _{PLH}	CLK	Q	5.1	8.8	10.9	5.1	13.2	5.1	12.4	ns
t _{PHL}			5.3	8.8	10.9	5.3	13.1	5.3	12.2	
t _{PZH}	\overline{OE}	Q	3.7	8.4	10.5	3.7	12.7	3.7	11.9	ns
t _{PZL}			4.4	9.7	11.9	4.4	14.3	4.4	13.4	
t _{PHZ}	\overline{OE}	Q	5.4	7.9	9.8	5.4	10.9	5.4	10.4	ns
t _{PLZ}			4.9	7.2	9.1	4.9	10.2	4.9	9.8	

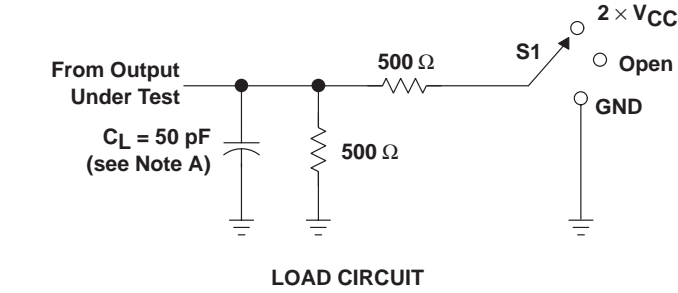
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C _L = 50 pF, f = 1 MHz	52	pF
		Outputs disabled		38	

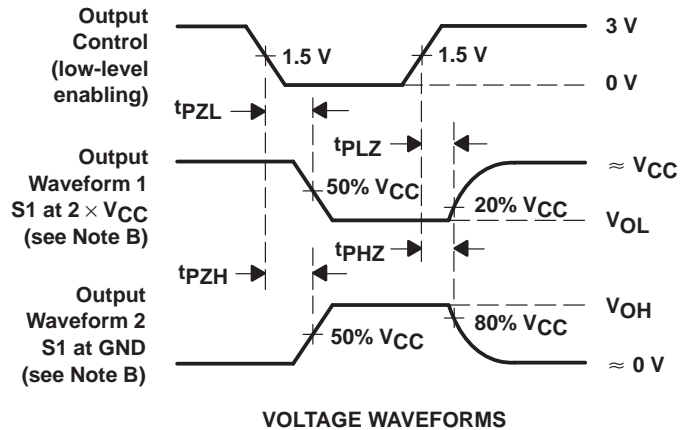
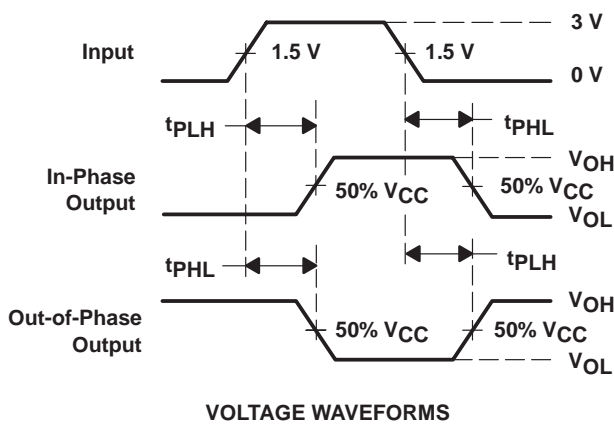
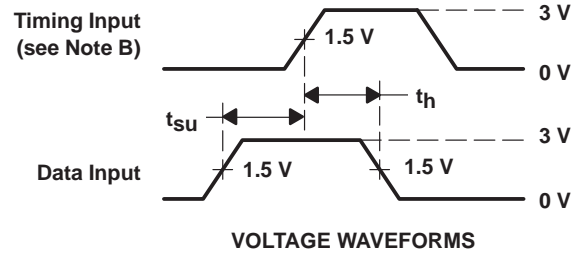
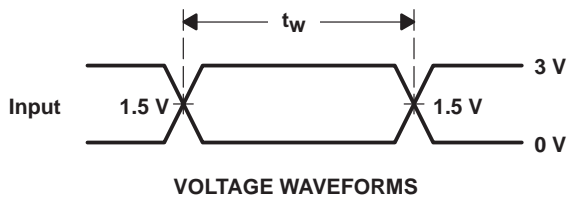
SN54ACT16374, 74ACT16374 16-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS124B – MARCH 1990 – REVISED APRIL 1996

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ACT16374DL	LIFEBUY	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16374	
74ACT16374DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16374	Samples
74ACT16374DLRG4	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16374	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

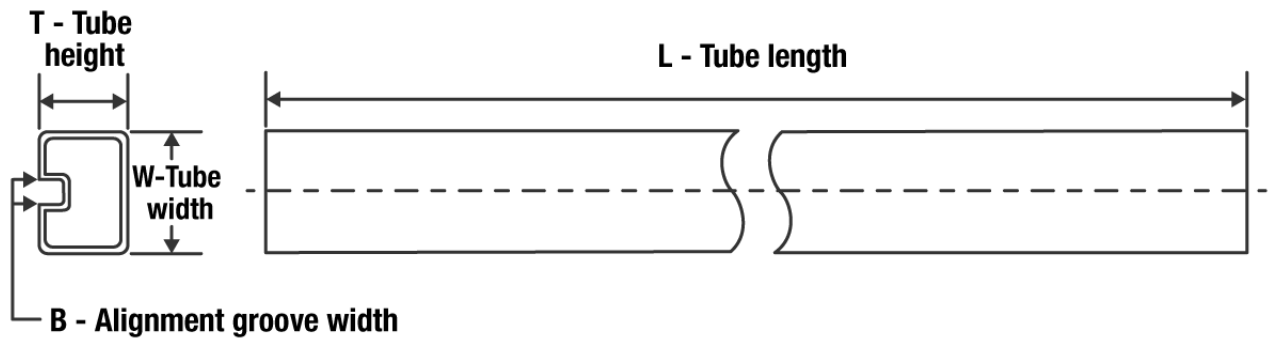

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16374DLR	SSOP	DL	48	1000	367.0	367.0	55.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
74ACT16374DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

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