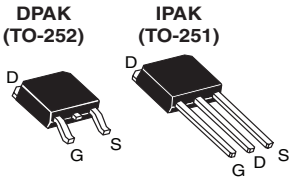
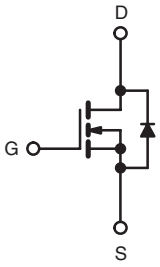
# Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 100 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 5.0 V | 0.54 |
| $Q_g$ (Max.) (nC) | 6.1 | |
| $Q_{gs}$ (nC) | 2.0 | |
| $Q_{gd}$ (nC) | 3.3 | |
| Configuration | Single | |




N-Channel MOSFET

## FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRLR110, SiHLR110)
- Straight Lead (IRLU110, SiHLU110)
- Available in Tape and Reel
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS}$ = 4 V and 5 V
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS* COMPLIANT
HALOGEN FREE Available

## DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRLU, SiHLU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

| ORDERING INFORMATION | | | | |
|---|---|---|---|---|
| Package | DPAK (TO-252) | DPAK (TO-252) | DPAK (TO-252) | IPAK (TO-251) |
| Lead (Pb)-free and Halogen-free | SiHLR110-GE3 | SiHLR110TR-GE3 | SiHLR110TRL-GE3 | SiHLU110-GE3 |
| Lead (Pb)-free | IRLR110PbF | IRLR110TRPbF[a] | IRLR110TRLPbF | IRLU110PbF |
| | SiHLR110-E3 | SiHLR110T-E3[a] | SiHLR110TL-E3 | SiHLU110-E3 |
| SnPb | IRLR110 | IRLR110TR[a] | IRLR110TRL[a] | IRLU110 |
| | SiHLR110 | SiHLR110T[a] | SiHLR110TL[a] | SiHLU110 |

**Note**
a. See device orientation.

| ABSOLUTE MAXIMUM RATINGS $T_C$ = 25 °C, unless otherwise noted | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | | | **SYMBOL** | **LIMIT** | **UNIT** |
| Drain-Source Voltage | | | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 10 | |
| Continuous Drain Current | $V_{GS}$ at 5.0 V | $T_C$ = 25 °C | $I_D$ | 4.3 | A |
| | | $T_C$ = 100 °C | | 2.7 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 17 | |
| Linear Derating Factor | | | | 0.20 | W/°C |
| Linear Derating Factor (PCB Mount)[e] | | | | 0.020 | |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 100 | mJ |
| Repetitive Avalanche Current[a] | | | $I_{AR}$ | 4.3 | A |
| Repetitive Avalanche Energy[a] | | | $E_{AR}$ | 2.5 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 25 | W |
| Maximum Power Dissipation (PCB Mount)[e] | $T_A$ = 25 °C | | | 2.5 | |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | 5.5 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 260[d] | |

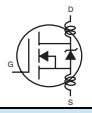
**Notes**
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. $V_{DD}$ = 25 V, starting $T_J$ = 25 °C, L = 8.1 mH, $R_g$ = 25 Ω, $I_{AS}$ = 4.3 A (see fig. 12).
c. $I_{SD}$ ≤ 5.6 A, dI/dt ≤ 140 A/µs, $V_{DD}$ ≤ $V_{DS}$, $T_J$ ≤ 150 °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | - | 110 | °C/W |
| Maximum Junction-to-Ambient (PCB Mount)[a] | $R_{thJA}$ | - | - | 50 | |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | - | 5.0 | |

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

| **SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 100 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 0.12 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = - 250 µA | 1.0 | - | 2.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 10 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | - | - | 25 | µA |
| | | $V_{DS}$ = 80 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 5.0 V, $I_D$ = 2.6 A[b] | - | - | 0.54 | Ω |
| | | $V_{GS}$ = 4.0 V, $I_D$ = 2.2 A[b] | - | - | 0.76 | |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 2.6 A | 2.3 | - | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | - | 250 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 80 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 15 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 5.0 V, $I_D$ = 5.6 A, $V_{DS}$ = 80 V, see fig. 6 and 13[b] | - | - | 6.1 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | - | 2.0 | |
| Gate-Drain Charge | $Q_{gd}$ | | - | - | 3.3 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 50 V, $I_D$ = 5.6 A, $R_g$ = 12 Ω, $R_D$ = 8.4 Ω, see fig. 10[b] | - | 9.3 | - | ns |
| Rise Time | $t_r$ | | - | 47 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 16 | - | |
| Fall Time | $t_f$ | | - | 17 | - | |
| Internal Drain Inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact[c]  | - | 4.5 | - | nH |
| Internal Source Inductance | $L_S$ | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 4.3 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | - | - | 17 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ =4.3 A, $V_{GS}$ = 0 V[b] | - | - | 2.5 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 5.6 A, dI/dt = 100 A/µs[b] | - | 100 | 130 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 0.50 | 0.65 | µC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

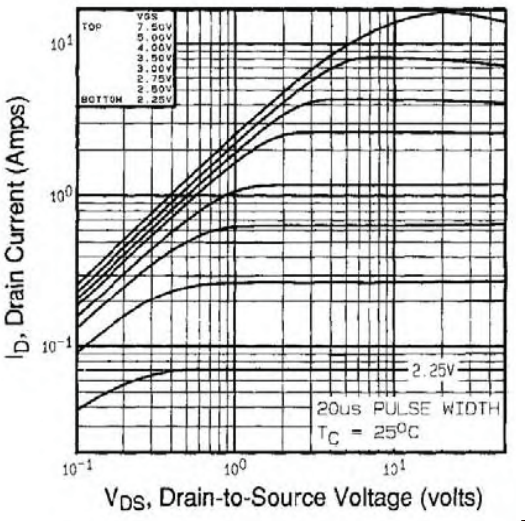



**Fig. 1 - Typical Output Characteristics, $T_C$ = 25 °C**

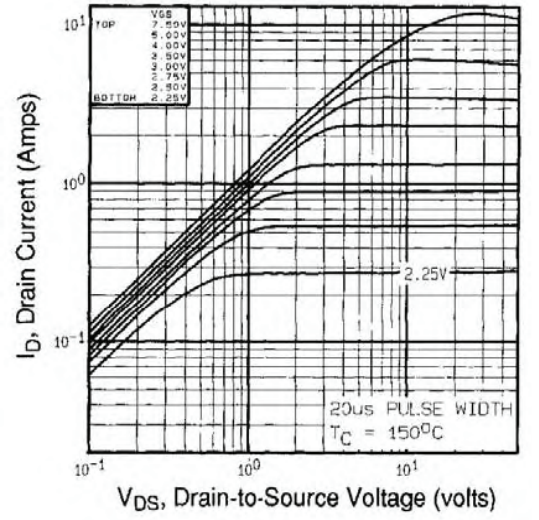



**Fig. 2 - Typical Output Characteristics, $T_C$ = 150 °C**

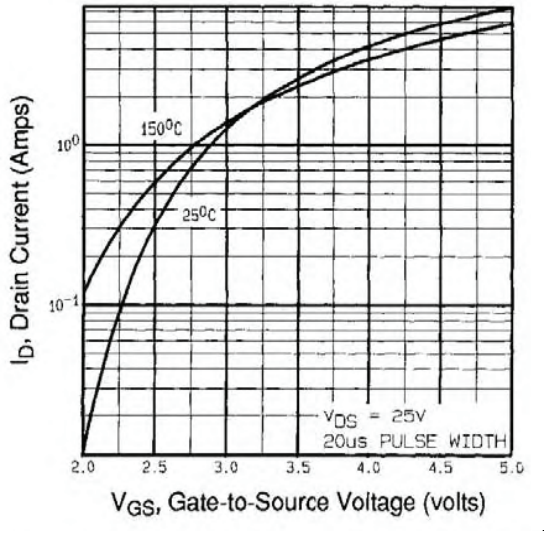



**Fig. 3 - Typical Transfer Characteristics**

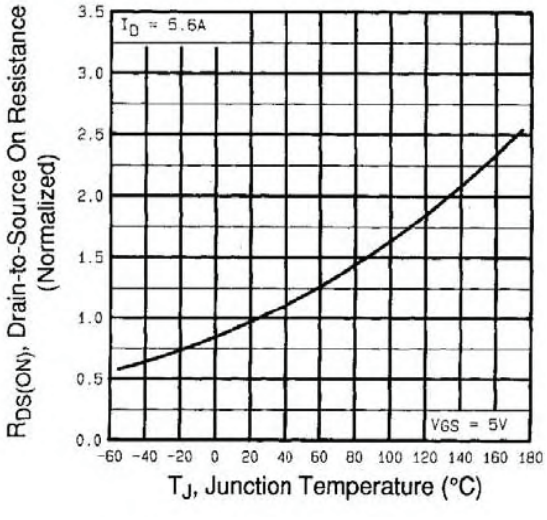



**Fig. 4 - Normalized On-Resistance vs. Temperature**

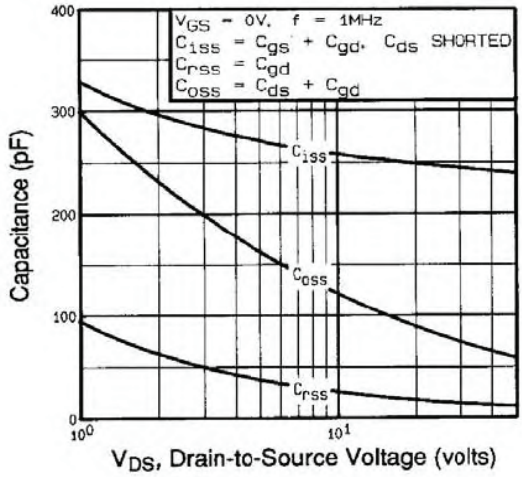



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

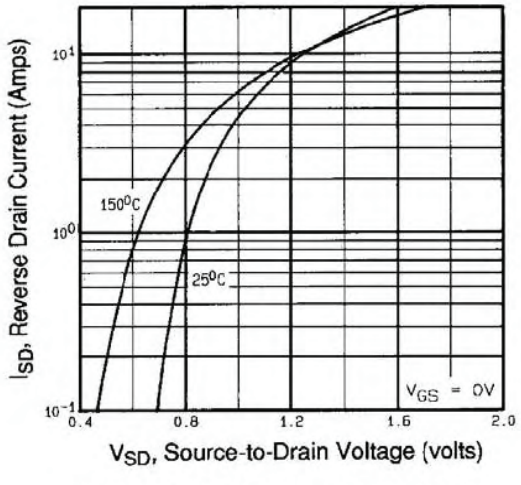



Fig. 7 - Typical Source-Drain Diode Forward Voltage

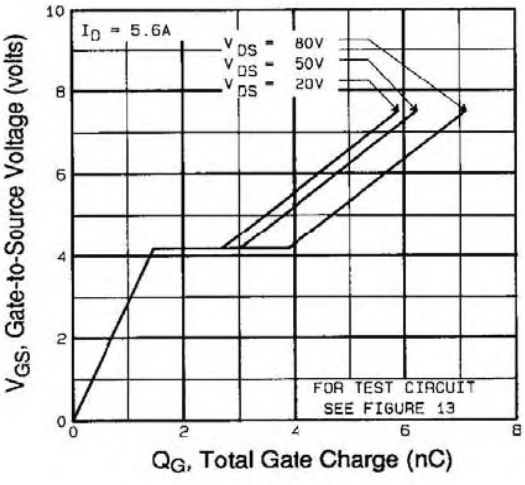



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

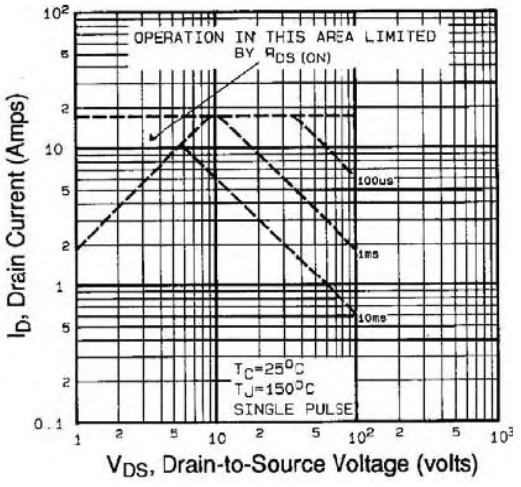



Fig. 8 - Maximum Safe Operating Area

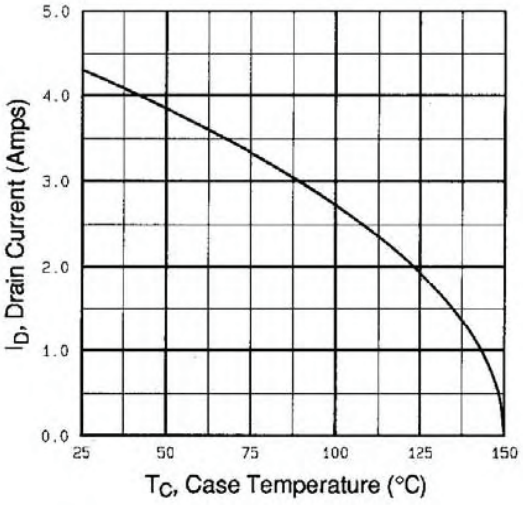



**Fig. 9 - Maximum Drain Current vs. Case Temperature**

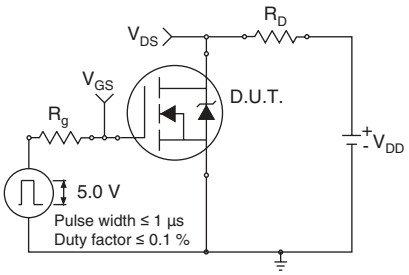



**Fig. 10a - Switching Time Test Circuit**

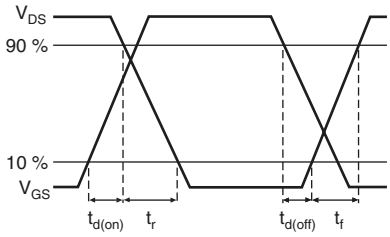



**Fig. 10b - Switching Time Waveforms**

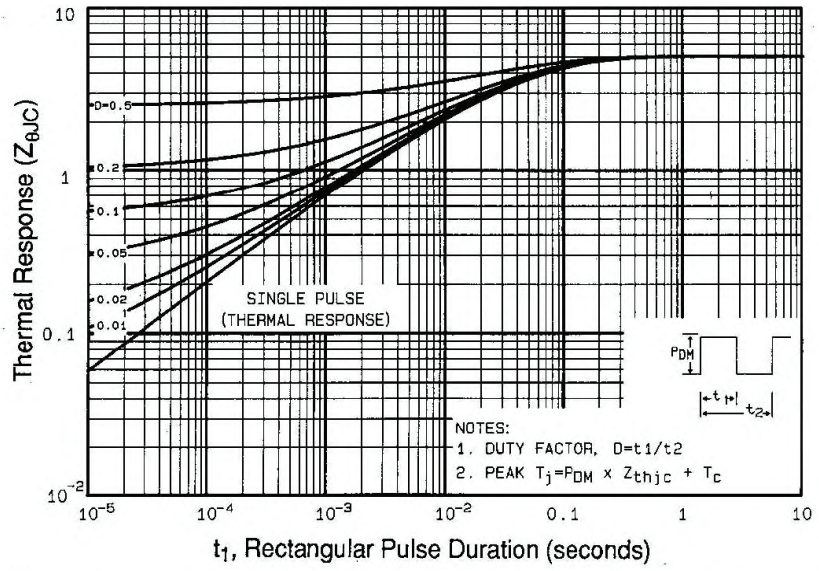



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

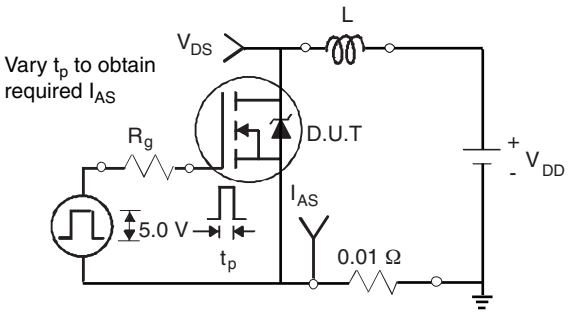



**Fig. 12a - Unclamped Inductive Test Circuit**

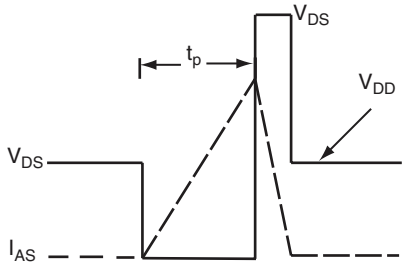



**Fig. 12b - Unclamped Inductive Waveforms**

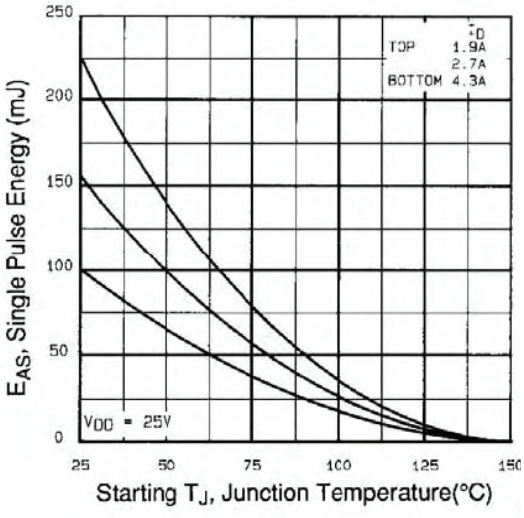



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

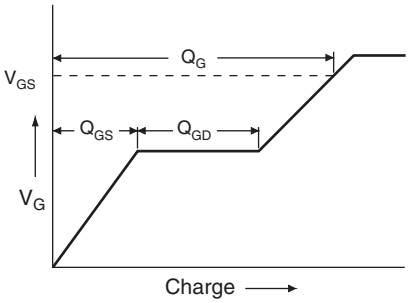



**Fig. 13a - Basic Gate Charge Waveform**

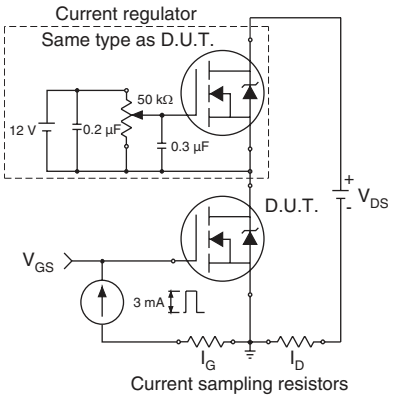
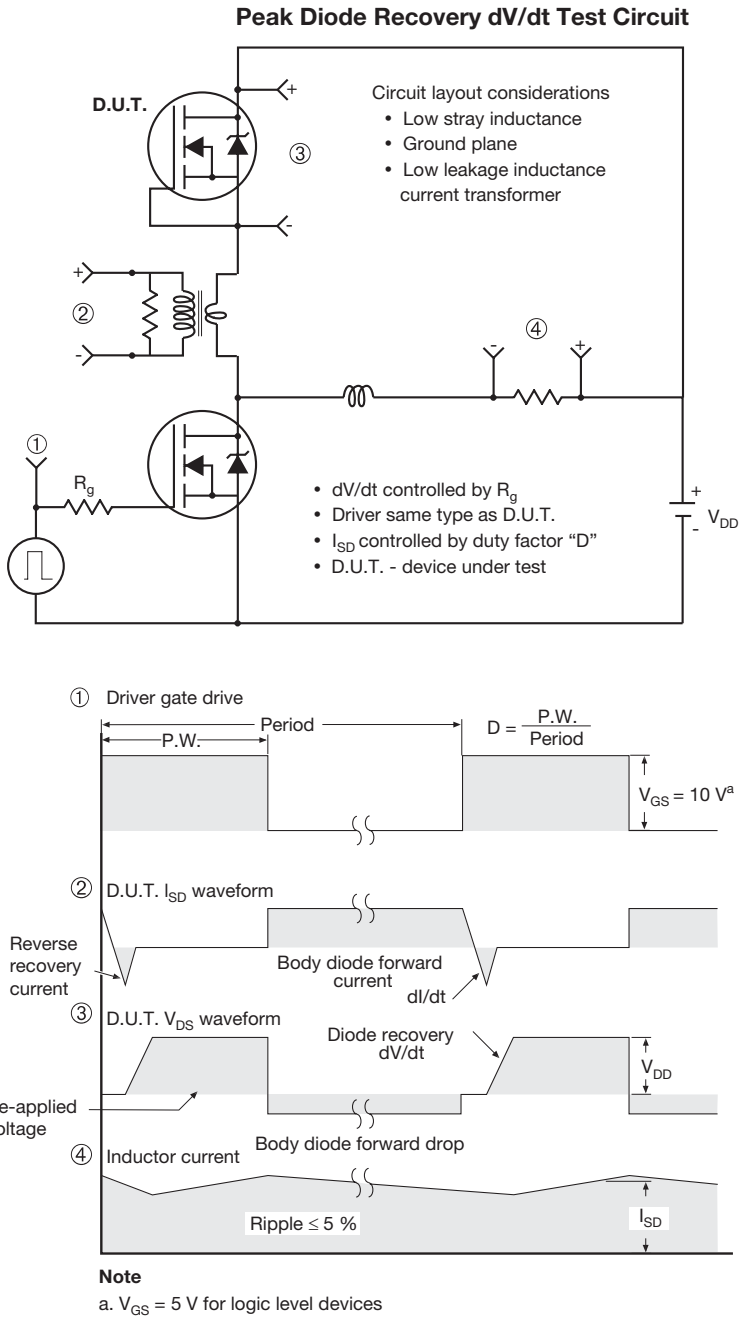



**Fig. 13b - Gate Charge Test Circuit**



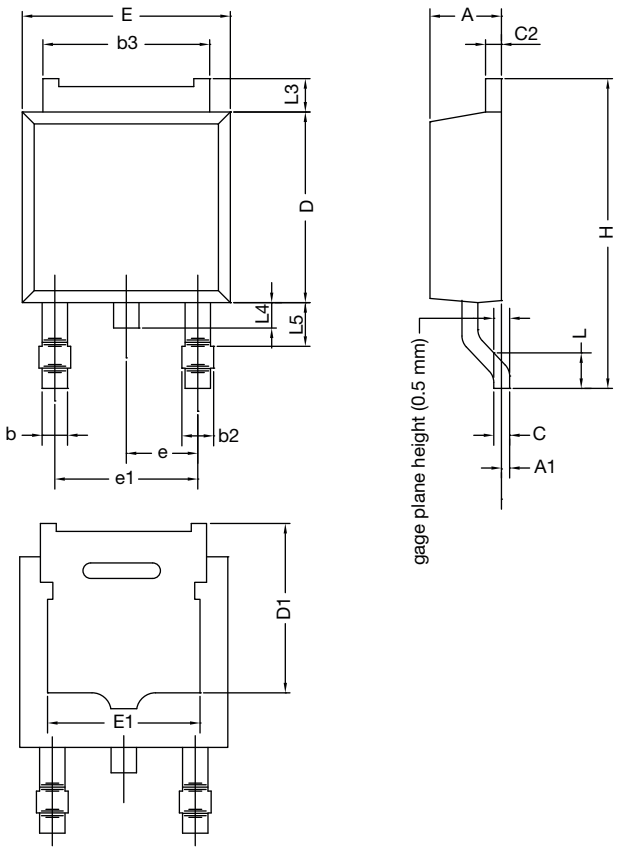

**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91323.*

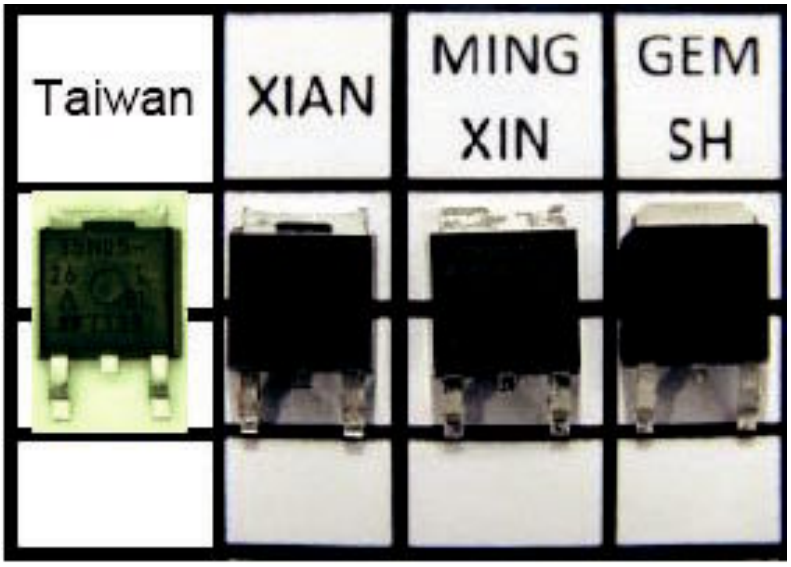
# TO-252AA Case Outline



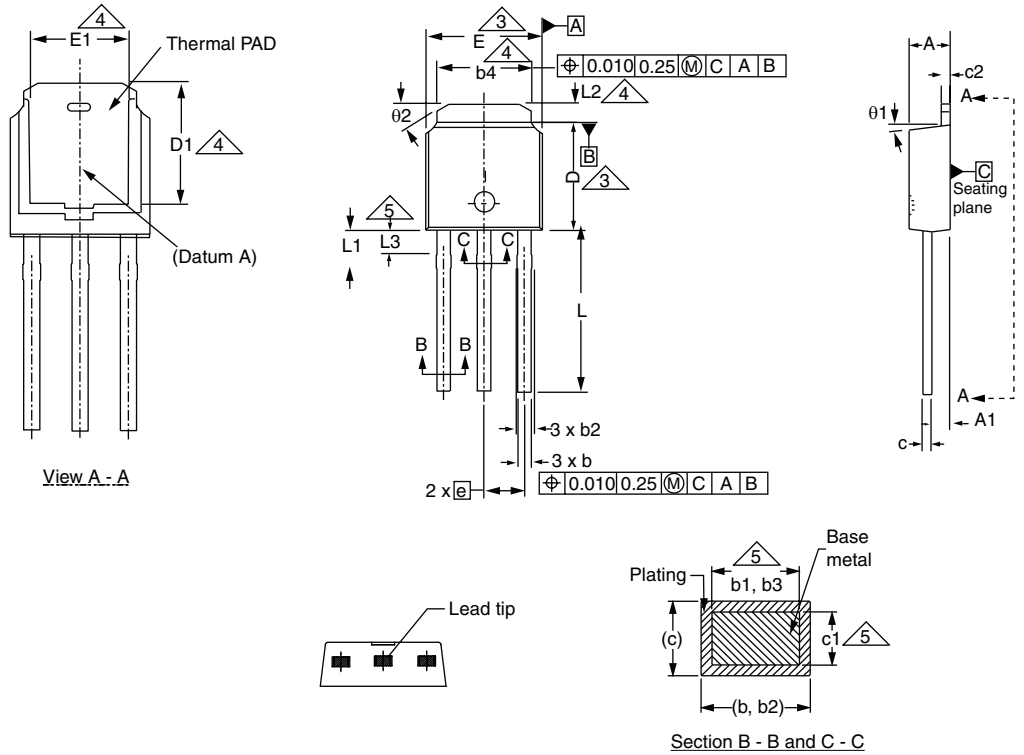

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 2.18 | 2.38 | 0.086 | 0.094 |
| A1 | - | 0.127 | - | 0.005 |
| b | 0.64 | 0.88 | 0.025 | 0.035 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 |
| b3 | 4.95 | 5.46 | 0.195 | 0.215 |
| C | 0.46 | 0.61 | 0.018 | 0.024 |
| C2 | 0.46 | 0.89 | 0.018 | 0.035 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |
| D1 | 4.10 | - | 0.161 | - |
| E | 6.35 | 6.73 | 0.250 | 0.265 |
| E1 | 4.32 | - | 0.170 | - |
| H | 9.40 | 10.41 | 0.370 | 0.410 |
| e | 2.28 BSC | | 0.090 BSC | |
| e1 | 4.56 BSC | | 0.180 BSC | |
| L | 1.40 | 1.78 | 0.055 | 0.070 |
| L3 | 0.89 | 1.27 | 0.035 | 0.050 |
| L4 | - | 1.02 | - | 0.040 |
| L5 | 1.01 | 1.52 | 0.040 | 0.060 |
| ECN: T13-0359-Rev. O, 03-Jun-13<br>DWG: 5347 | | | | |

**Notes**

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



## TO-251AA (HIGH VOLTAGE)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 2.18 | 2.39 | 0.086 | 0.094 |
| A1 | 0.89 | 1.14 | 0.035 | 0.045 |
| b | 0.64 | 0.89 | 0.025 | 0.035 |
| b1 | 0.65 | 0.79 | 0.026 | 0.031 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 |
| b3 | 0.76 | 1.04 | 0.030 | 0.041 |
| b4 | 4.95 | 5.46 | 0.195 | 0.215 |
| c | 0.46 | 0.61 | 0.018 | 0.024 |
| c1 | 0.41 | 0.56 | 0.016 | 0.022 |
| c2 | 0.46 | 0.86 | 0.018 | 0.034 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |

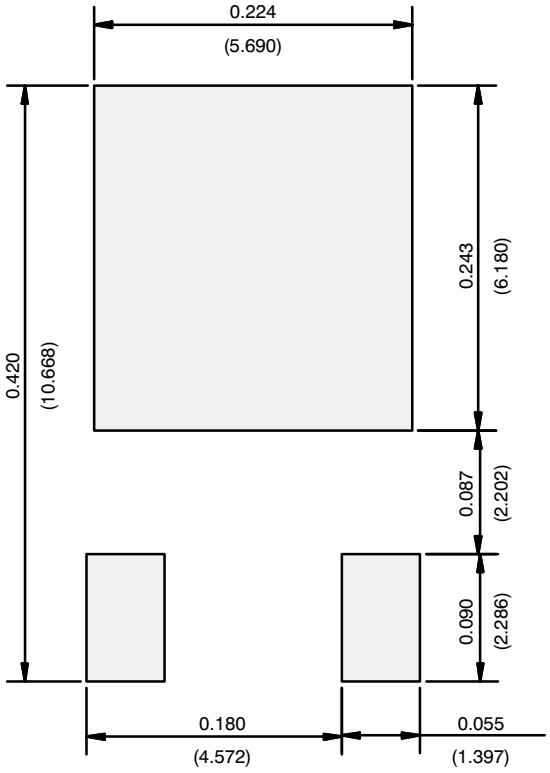
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 5.21 | - | 0.205 | - |
| E | 6.35 | 6.73 | 0.250 | 0.265 |
| E1 | 4.32 | - | 0.170 | - |
| e | 2.29 BSC | | 2.29 BSC | |
| L | 8.89 | 9.65 | 0.350 | 0.380 |
| L1 | 1.91 | 2.29 | 0.075 | 0.090 |
| L2 | 0.89 | 1.27 | 0.035 | 0.050 |
| L3 | 1.14 | 1.52 | 0.045 | 0.060 |
| θ1 | 0' | 15' | 0' | 15' |
| θ2 | 25' | 35' | 25' | 35' |

ECN: S-82111-Rev. A, 15-Sep-08
DWG: 5968

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)




Recommended Minimum Pads
Dimensions in Inches/(mm)

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# Material Category Policy

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.**

**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**