

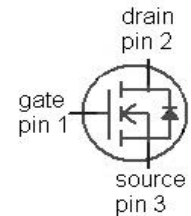
OptiMOS™ 3 Power-Transistor

Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target application
- Ideal for high-frequency switching and synchronous rectification
- Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}	150	V
$R_{DS(on),max}$	20	mΩ
I_D	50	A



Type	IPB200N15N3 G	IPD200N15N3 G	IPI200N15N3 G	IPP200N15N3 G
Package	PG-TO263-3	PG-TO252-3	PG-TO262-3	PG-TO220-3
Marking	200N15N	200N15N	200N15N	200N15N

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	50	A
		$T_C=100\text{ °C}$	40	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	200	
Avalanche energy, single pulse	E_{AS}	$I_D=50\text{ A}$, $R_{GS}=25\text{ Ω}$	170	mJ
Reverse diode dv/dt	dv/dt	$I_D=50\text{ A}$, $V_{DS}=120\text{ V}$, $di/dt=100\text{ A/μs}$, $T_{j,max}=175\text{ °C}$	6	kV/μs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	150	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

¹⁾J-STD20 and JESD22

²⁾ See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	75	
		6 cm ² cooling area ³⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	150	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=90\text{ }\mu\text{A}$	2	3	4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=120\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=120\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=50\text{ A}$	-	16	20	m Ω
		$V_{GS}=8\text{ V}, I_D=25\text{ A}$	-	16	20	
Gate resistance	R_G		-	2.4	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=50\text{ A}$	29	57	-	S

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=75\text{ V},$ $f=1\text{ MHz}$	-	1820	-	pF
Output capacitance	C_{oss}		-	214	-	
Reverse transfer capacitance	C_{rss}		-	5	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=75\text{ V}, V_{GS}=10\text{ V},$ $I_D=50\text{ A}, R_{G,ext}=1.6\ \Omega$	-	14	21	ns
Rise time	t_r		-	11	17	
Turn-off delay time	$t_{d(off)}$		-	23	35	
Fall time	t_f		-	6	9	

Gate Charge Characteristics⁴⁾

Gate to source charge	Q_{gs}	$V_{DD}=75\text{ V}, I_D=50\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	10	14	nC
Gate to drain charge	Q_{gd}		-	4	6	
Switching charge	Q_{sw}		-	9	13	
Gate charge total	Q_g		-	23	31	
Gate plateau voltage	$V_{plateau}$		-	5.7	-	V
Output charge	Q_{oss}	$V_{DD}=75\text{ V}, V_{GS}=0\text{ V}$	-	60	79	nC

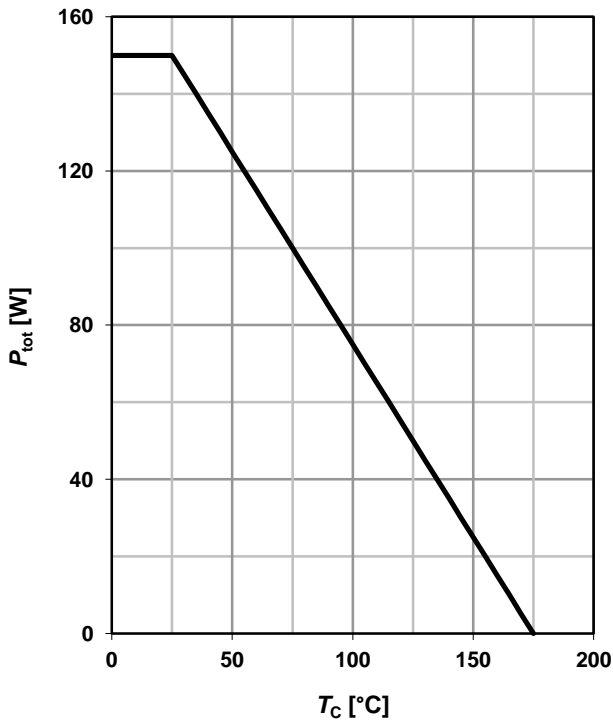
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	220	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	1	1.2	V
Reverse recovery time	t_{rr}	$V_R=75\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	106	-	ns
Reverse recovery charge	Q_{rr}		-	332	-	nC

⁴⁾ See figure 16 for gate charge parameter definition

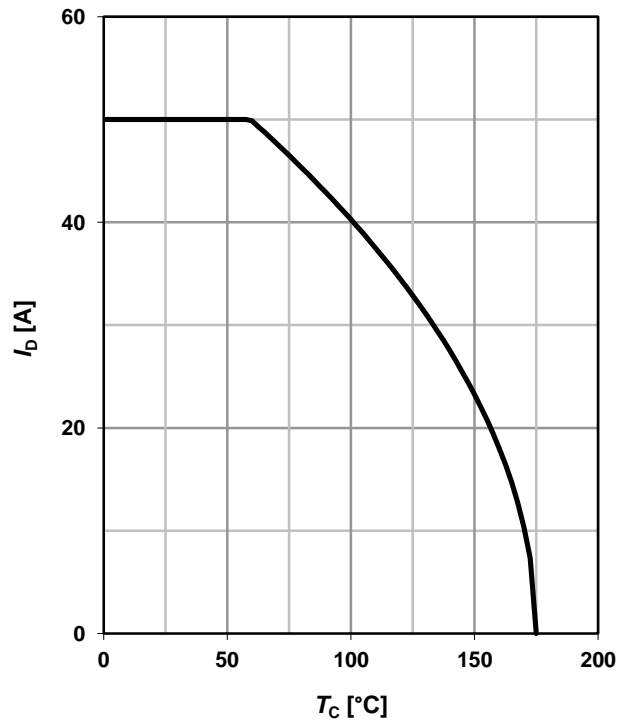
1 Power dissipation

$$P_{tot}=f(T_C)$$



2 Drain current

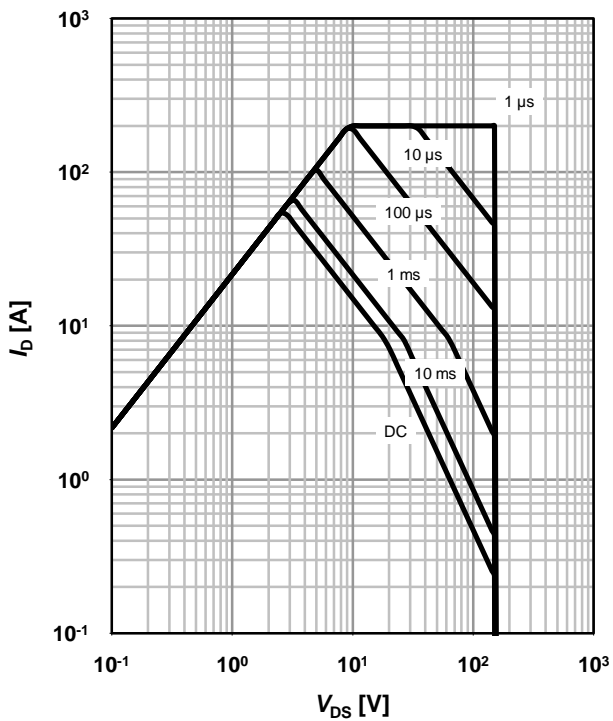
$$I_D=f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D=f(V_{DS}); T_C=25 \text{ °C}; D=0$$

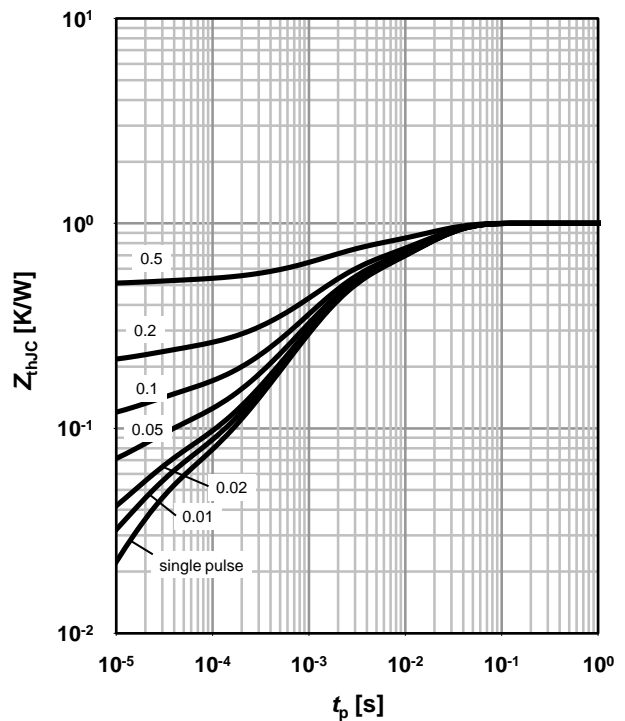
parameter: t_p



4 Max. transient thermal impedance

$$Z_{thJC}=f(t_p)$$

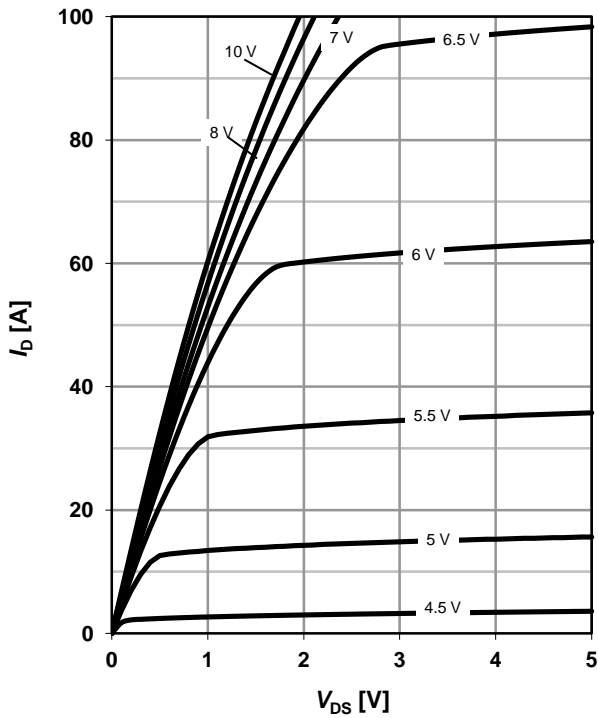
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

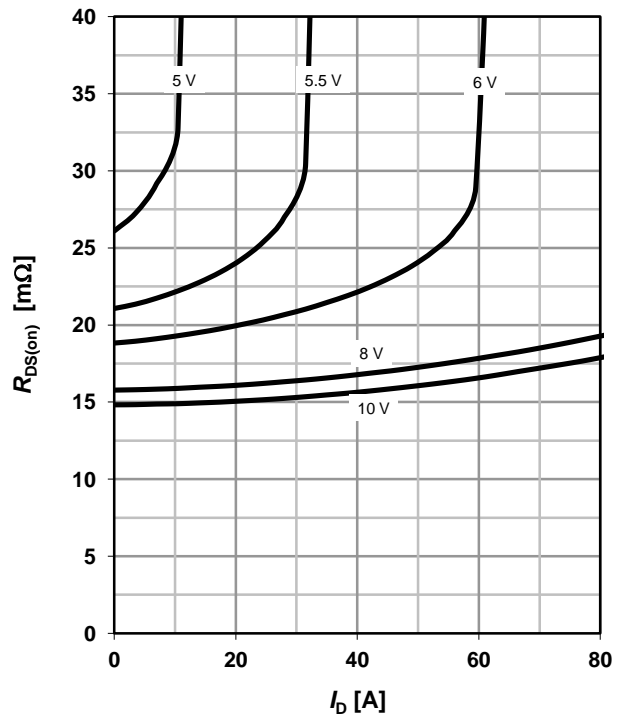
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

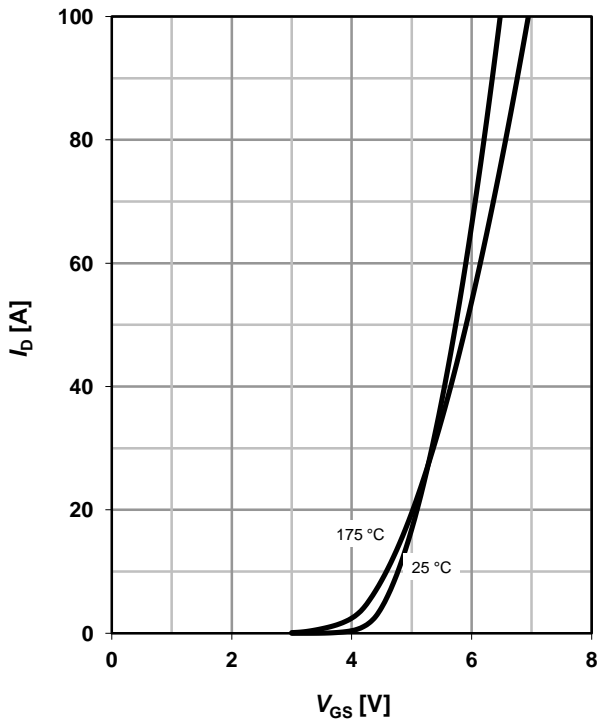
parameter: V_{GS}



7 Typ. transfer characteristics

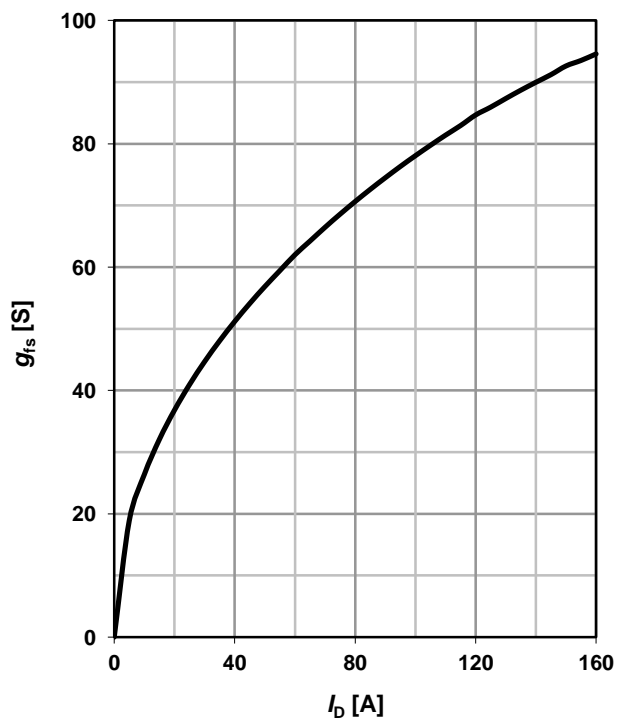
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



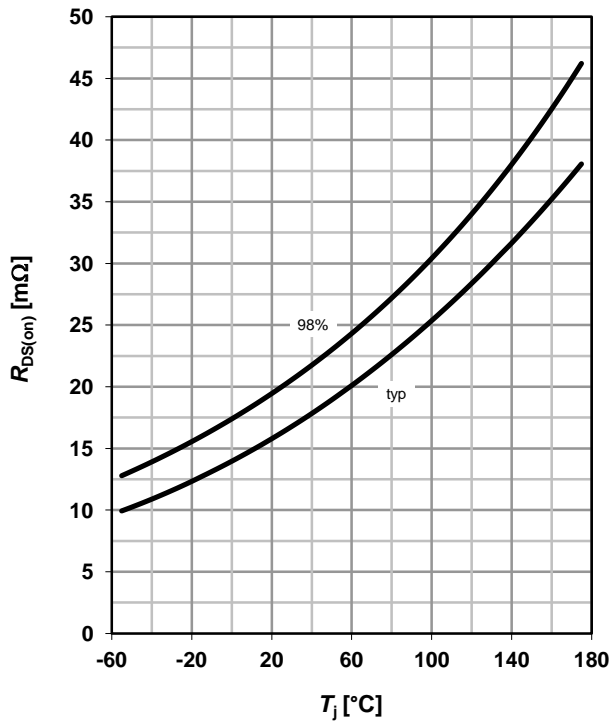
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



9 Drain-source on-state resistance

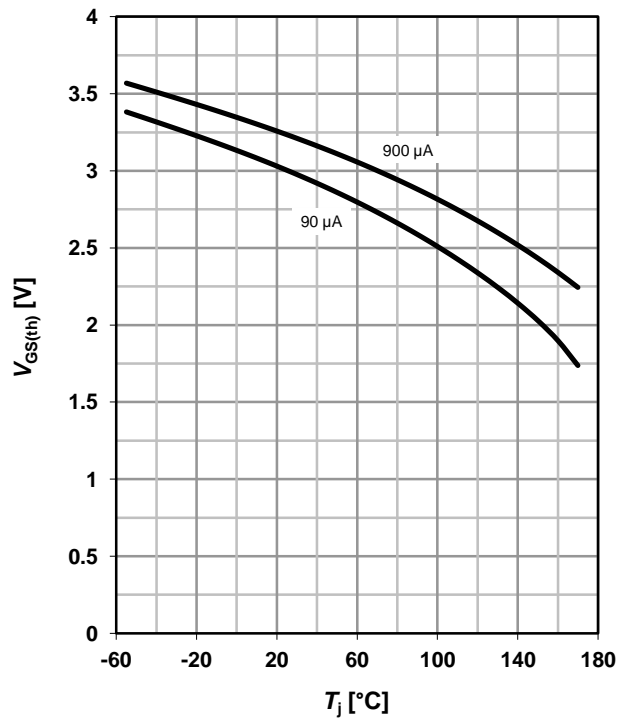
$$R_{DS(on)} = f(T_j); I_D = 50 \text{ A}; V_{GS} = 10 \text{ V}$$



10 Typ. gate threshold voltage

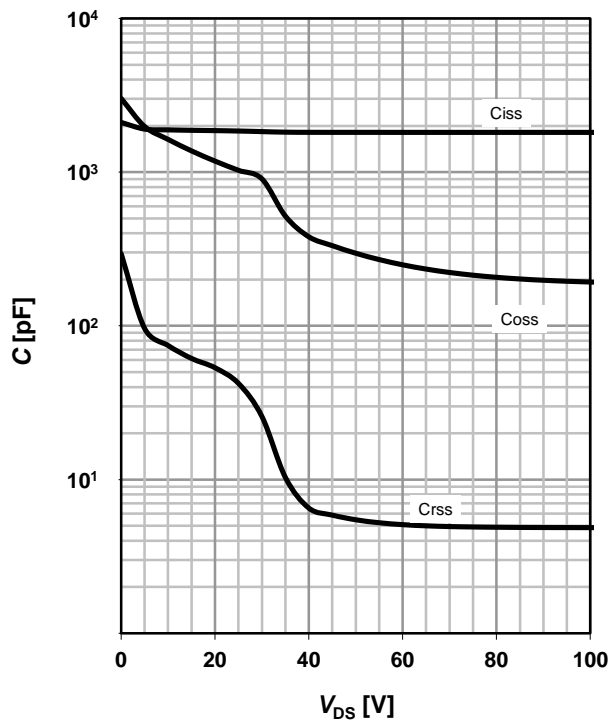
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



11 Typ. capacitances

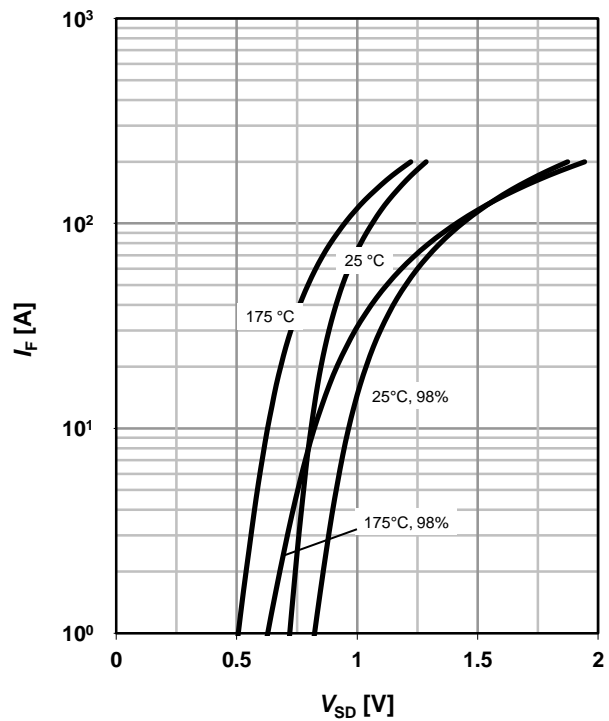
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

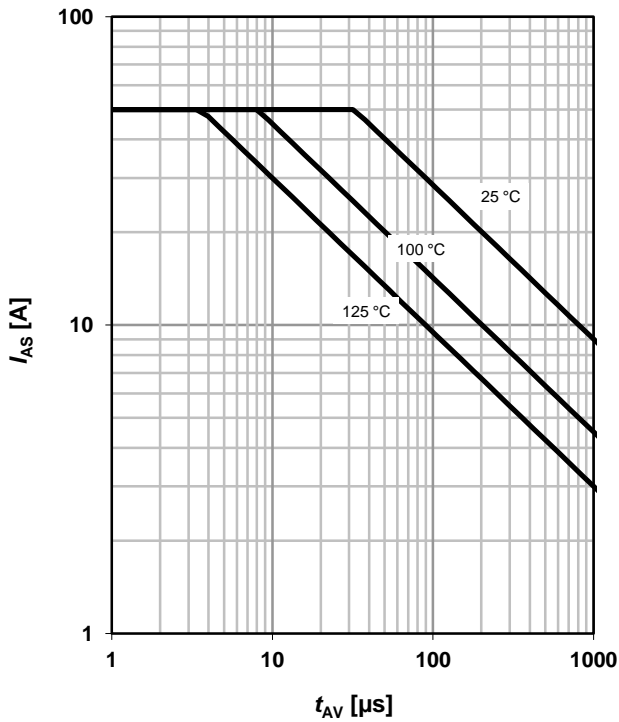
parameter: T_j



13 Avalanche characteristics

$$I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega$$

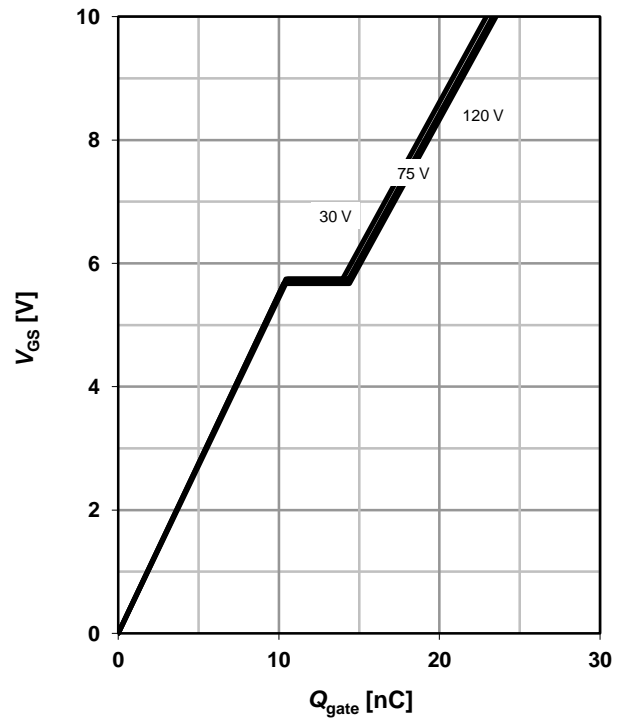
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

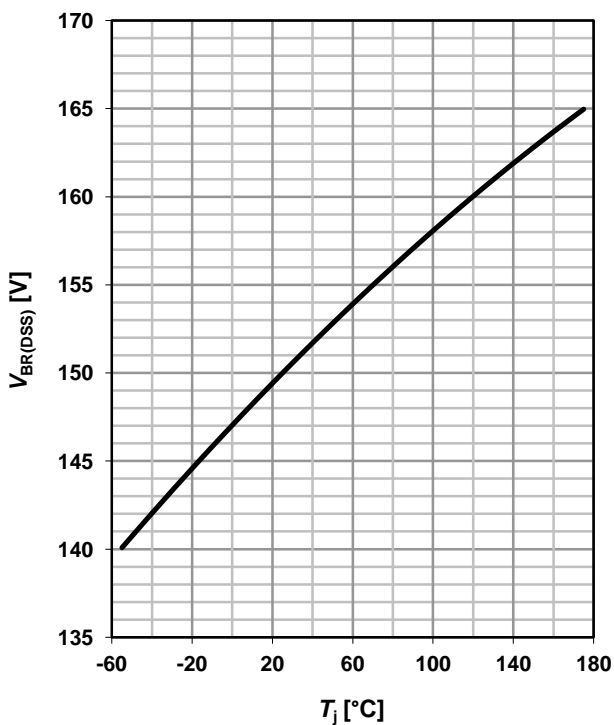
$$V_{GS} = f(Q_{\text{gate}}); I_D = 50 \text{ A pulsed}$$

parameter: V_{DD}

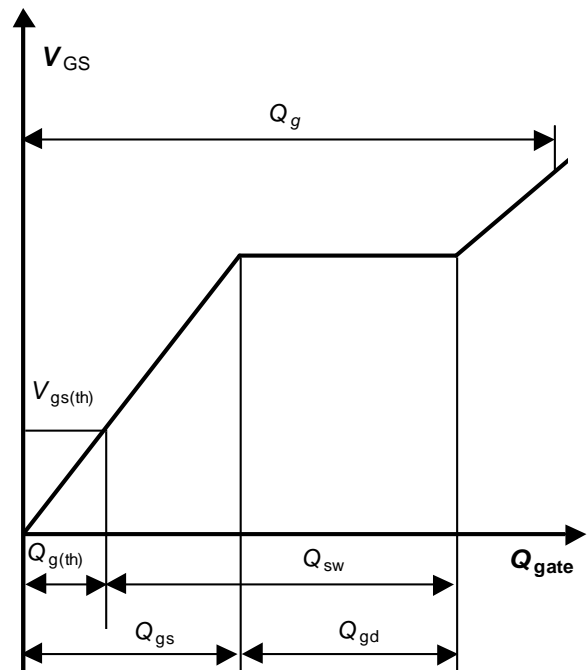


15 Drain-source breakdown voltage

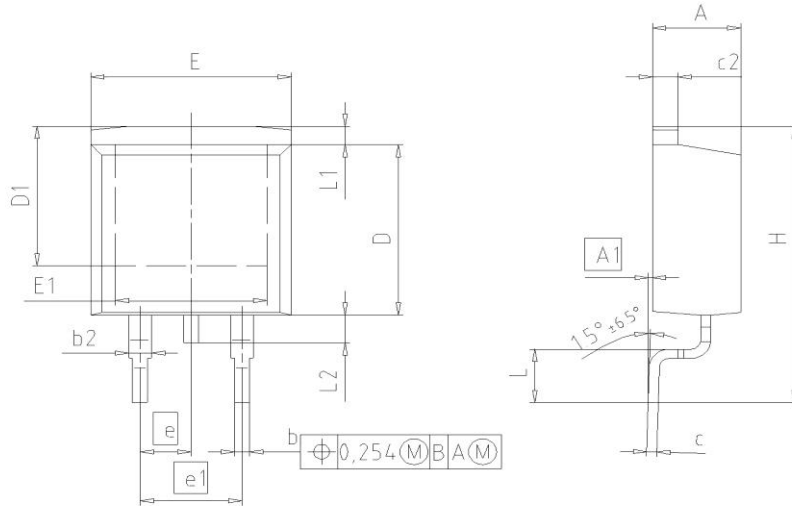
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



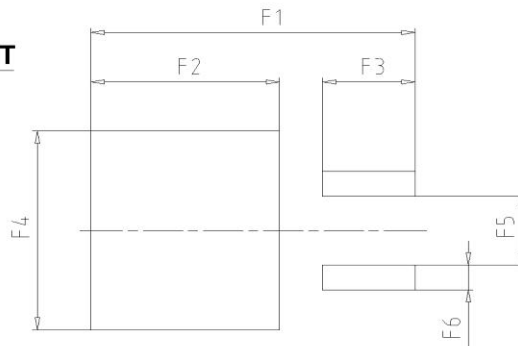
16 Gate charge waveforms



PG-TO263-3 Outline



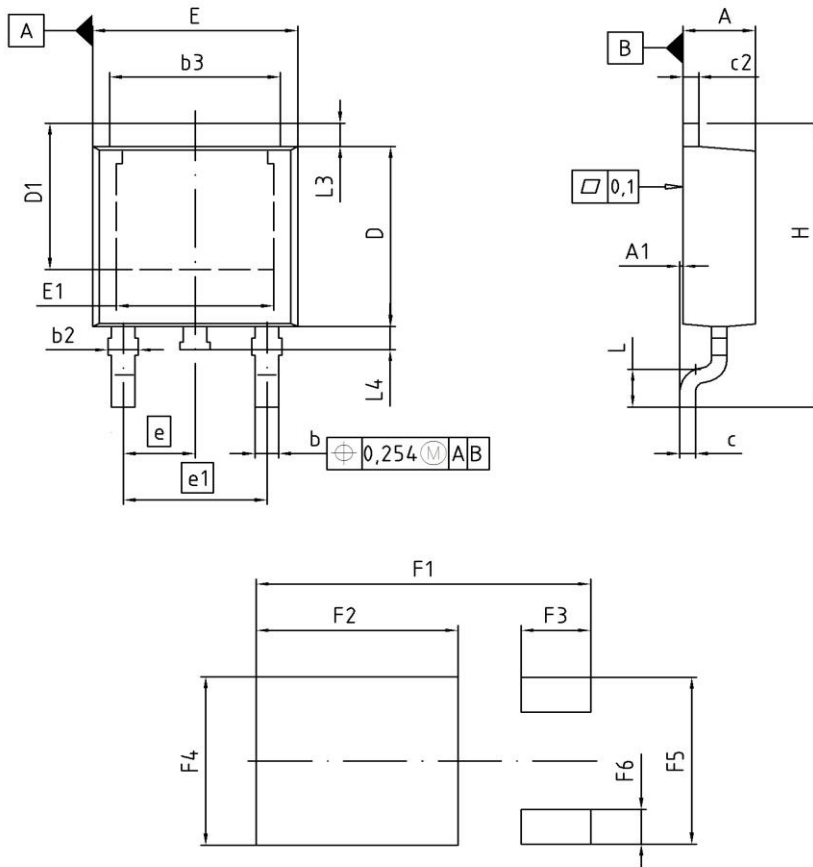
FOOTPRINT



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

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PG-TO252-3 Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051

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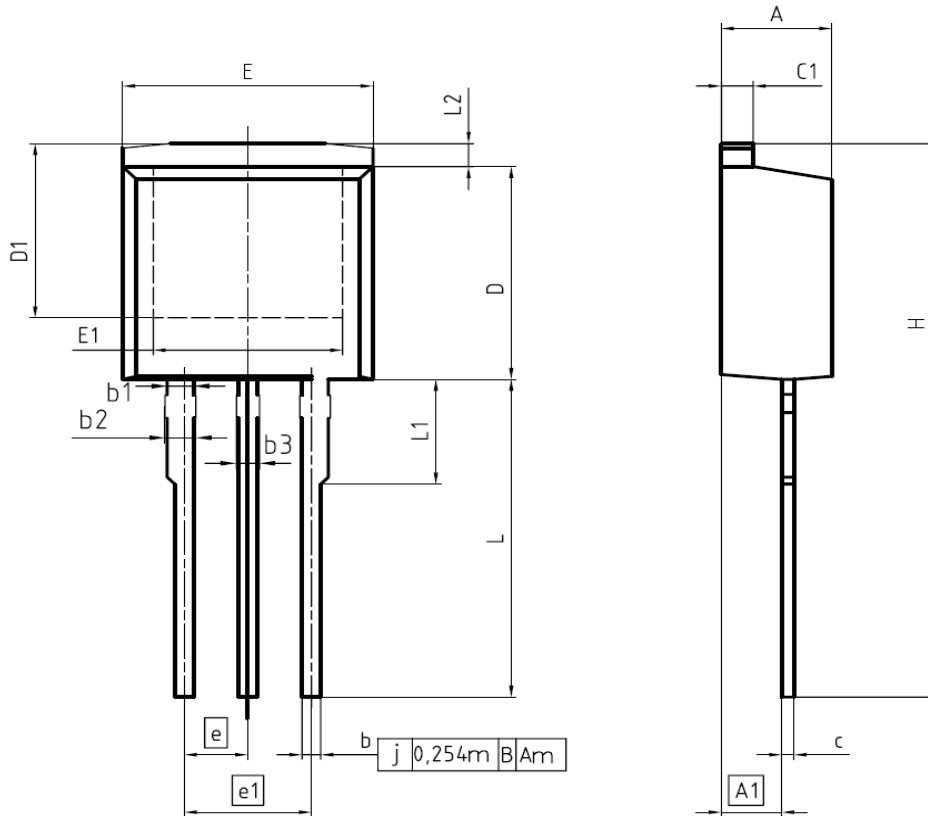
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REVISION
03

PG-TO262-3 Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	2.150	2.718	0.085	0.107
b	0.650	0.864	0.026	0.034
b1	0.950	1.093	0.037	0.043
b2	0.950	1.400	0.037	0.055
b3	0.650	1.118	0.026	0.044
c	0.330	0.600	0.013	0.024
c1	1.170	1.400	0.046	0.055
D	8.509	9.450	0.335	0.372
D1	6.900	-	0.272	-
E	9.700	10.363	0.382	0.408
E1	6.500	8.600	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
L	13.000	14.000	0.512	0.551
L1	-	4.800	-	0.189
L2	-	1.727	-	0.068

REFERENCE
JEDEC TO262

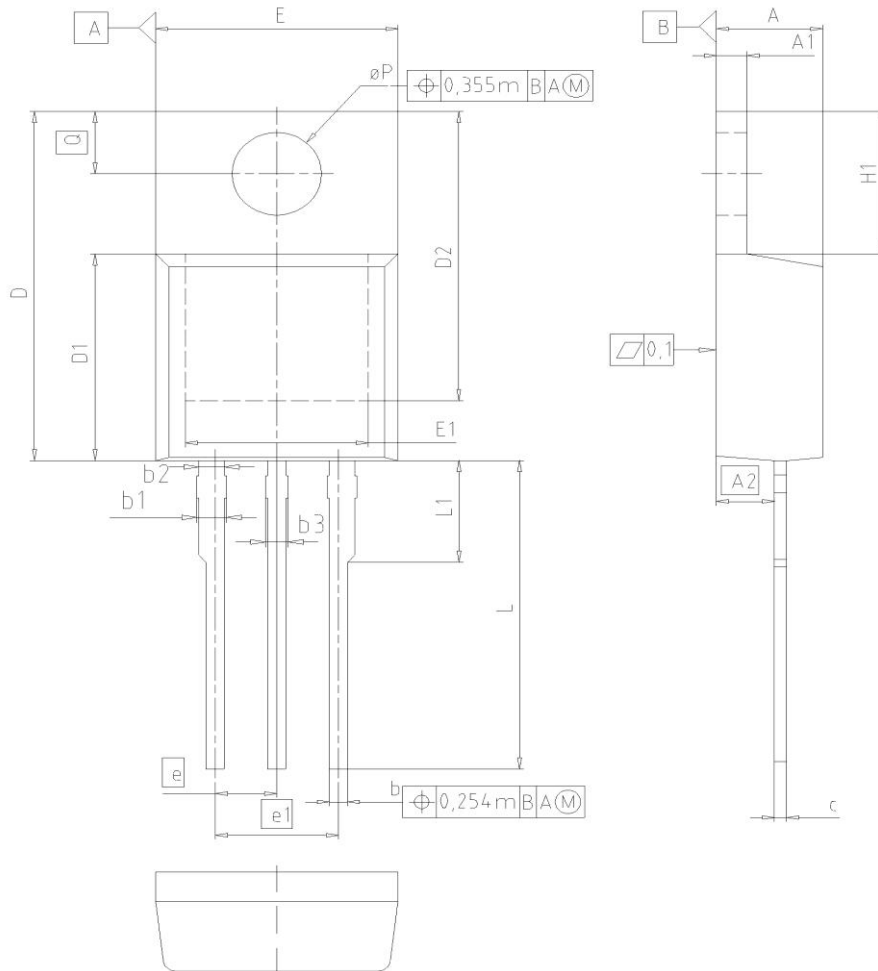
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05-05-2006

FILE
TO262_1

PG-TO220-3 Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

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