
4-Mbit, 3.3V, SPI Serial Flash

Features

- Single Voltage Read and Write Operations
 - 2.3V-3.6V
- Serial Interface Architecture
 - SPI Compatible: Mode 0 and Mode 3
- High-Speed Clock Frequency
 - 40 MHz
- Dual Input/Output Support
 - Fast-Read Dual-Output Instruction (3BH)
 - Fast-Read Dual I/O Instruction (BBH)
- Superior Reliability
 - Endurance: 100,000 Cycles
 - Greater than 20 years Data Retention
- Ultra-Low Power Consumption:
 - Active Read current: 5 mA (typical)
 - Standby current: 5 μ A (typical)
 - Power-down Mode Standby current: 3 μ A (typical)
- Flexible Erase Capability
 - Uniform 4-Kbyte sectors
 - Uniform 64-Kbyte overlay blocks
- Page Program Mode
 - 256 bytes per Page
- Fast Erase and Page Program:
 - Chip Erase Time: 250 ms (typical)
 - Sector Erase Time: 40 ms (typical)
 - Block Erase Time: 80 ms (typical)
 - Page Program Time: 4 ms/ 256 bytes (typical)
- End-of-Write Detection
 - Software polling the BUSY bit in STATUS Register
- Hold Pin (HOLD#)
 - Suspend a serial sequence without deselecting the device
- Write Protection (WP#)
 - Enables/Disables the Lock-Down function of the STATUS register
- Software Write Protection
 - Write protection through Block-Protection bits in STATUS register

- Temperature Range
 - Industrial: -40°C to +85°C
 - Industrial Plus: -40°C to +105°C
 - Extended: -40°C to +125°C
- Automotive AEC-Q100 Qualified
- All devices are RoHS compliant

Packages

- 8-contact USON (2 mm x 3 mm)
- 8-lead SOIC (150 mils)
- 8-contact WDFN (5 mm x 6 mm)

Product Description

SST25PF040C is a member of the Serial Flash 25 Series family and feature a four-wire, SPI-compatible interface that allows for a low pin-count package which occupies less board space and ultimately lowers total system costs. SPI serial flash memory is manufactured with proprietary, high-performance CMOS SuperFlash[®] technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

This Serial Flash significantly improve performance and reliability, while lowering power consumption. The device writes (Program or Erase) with a single power supply of 2.3V-3.6V. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

See [Figure 2-1](#) for the pin assignments.

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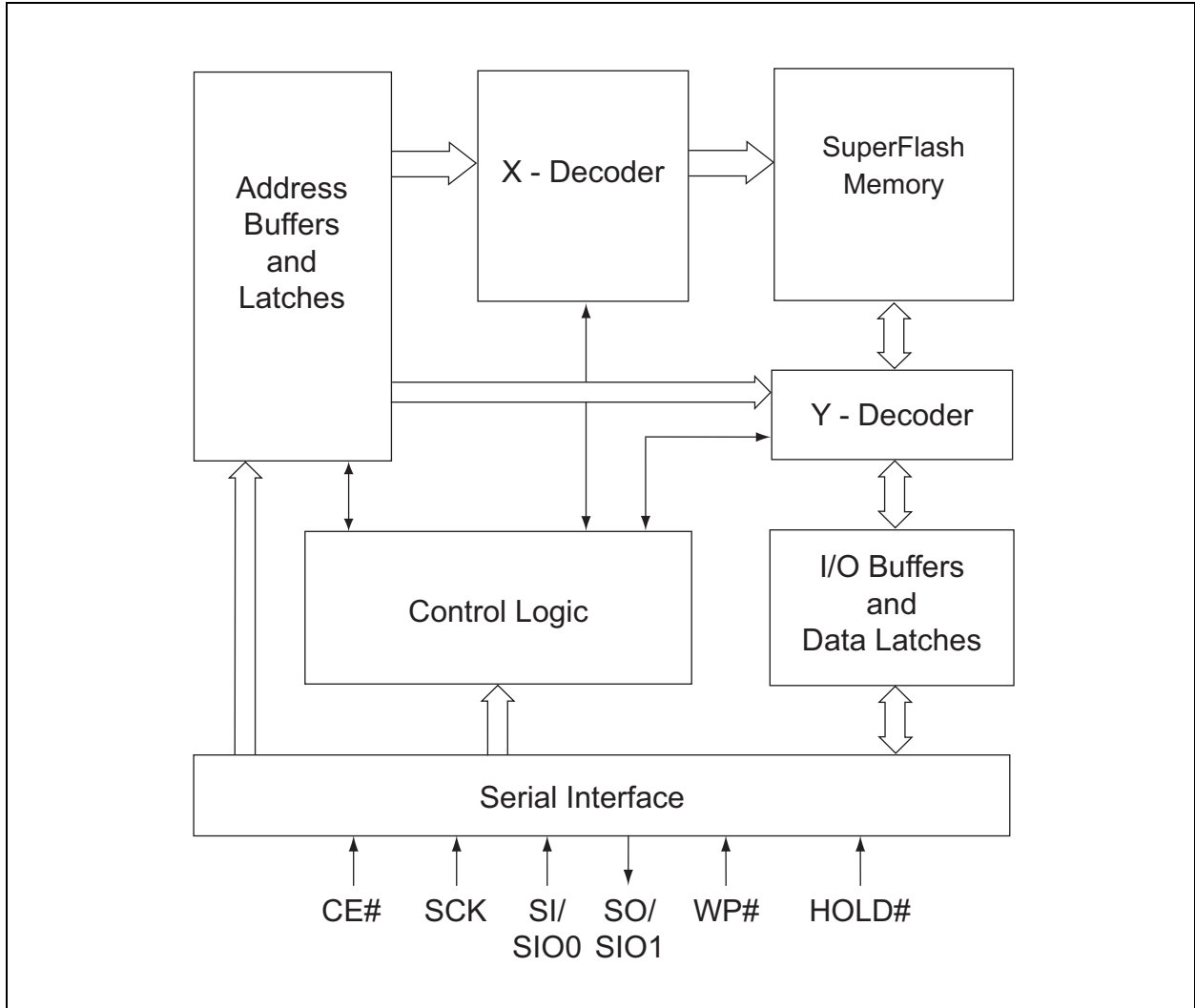
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1.0 FUNCTIONAL BLOCKS

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



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2.0 PIN ASSIGNMENTS

FIGURE 2-1: PIN ASSIGNMENTS

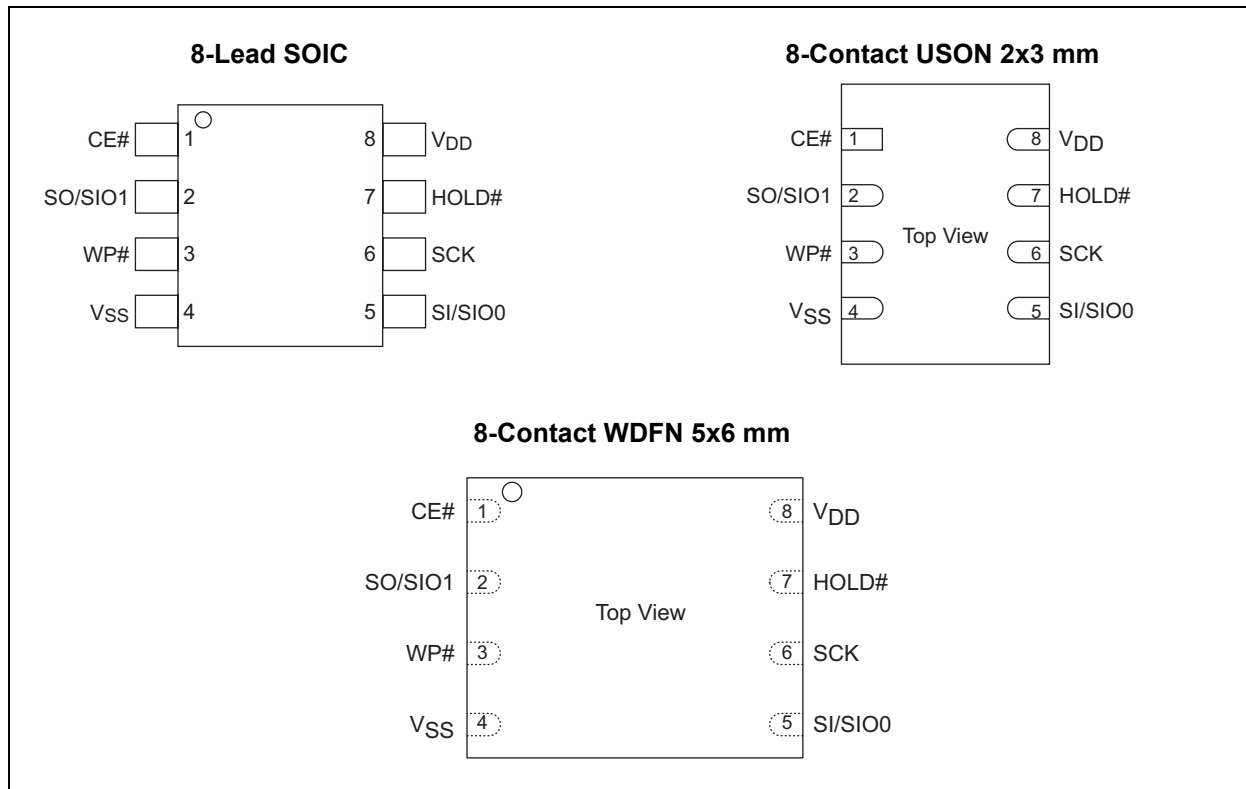


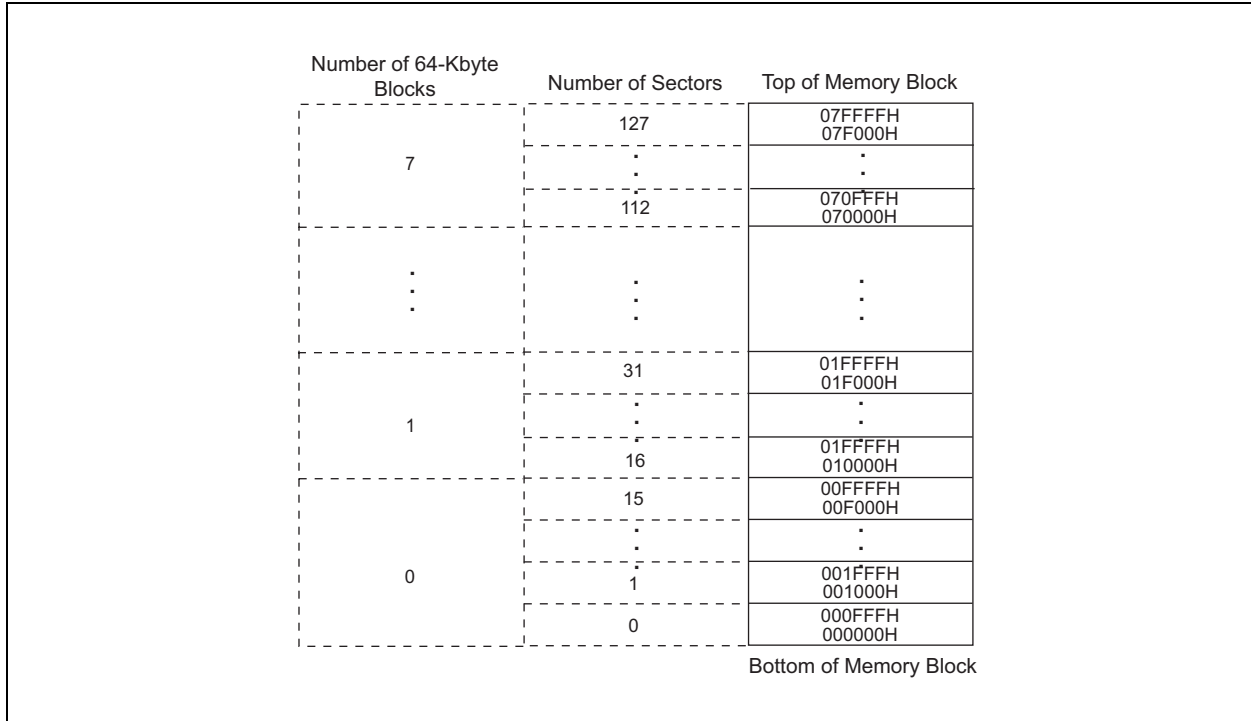
TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence. The device is deselected and placed in Standby mode when CE# is high.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock.
SIO[0:1]	Serial Data Input/Output for Dual I/O Mode	To transfer commands, addresses, or data serially into the device, or data out of the device. Inputs are latched on the rising edge of the serial clock. Data is shifted out on the falling edge of the serial clock. These pins are used in Dual I/O mode
WP#	Write-Protect	The Write-Protect (WP#) pin is used to enable/disable BPL bit in the STATUS register.
VSS	Ground	
VDD	Power Supply	To provide power supply voltage: 2.3V-3.6V
HOLD#	Hold	To temporarily stop serial communication with SPI Flash memory while device is selected.
SCK	Serial Clock	To provide the input/output timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.

3.0 MEMORY ORGANIZATION

The SST25PF040C SuperFlash memory arrays are organized in 128 uniform 4-Kbyte sectors, with eight 64-Kbyte overlay erasable blocks.

FIGURE 3-1: MEMORY MAP

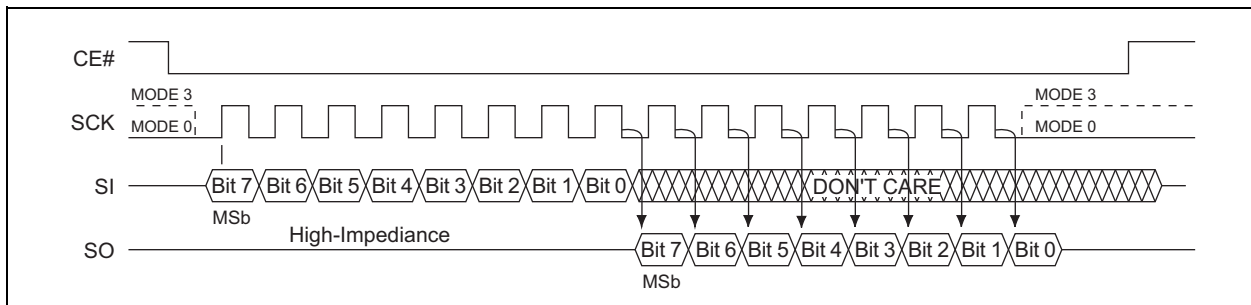


4.0 DEVICE OPERATION

SST25PF040C is accessed through the SPI (Serial Peripheral Interface) bus compatible protocol. The SPI bus consist of four control lines: Chip Enable (CE#) is used to select the device, and data is accessed through the Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK).

The SST25PF040C supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 4-1, is the state of the SCK signal when the bus host is in Standby mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

FIGURE 4-1: SPI PROTOCOL



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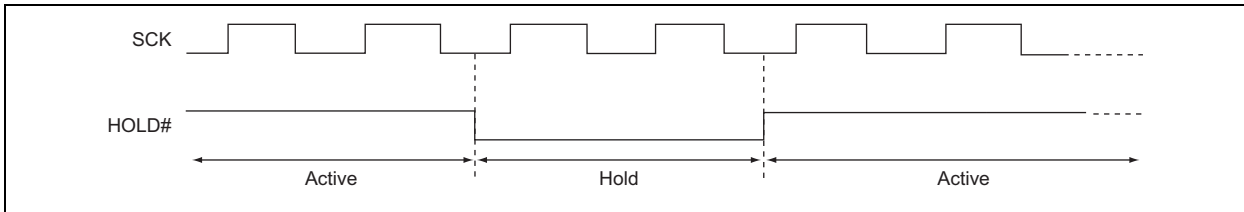
4.0.1 HOLD

In the hold mode, serial sequences underway with the SPI Flash memory are paused without resetting the clocking sequence. To activate the HOLD# mode, CE# must be in active low state. The HOLD# mode begins when the SCK active low state coincides with the falling edge of the HOLD# signal. The Hold mode ends when the rising edge of the HOLD# signal coincides with the SCK active low state. HOLD# must not rise or fall when SCK logic level is high. See Figure 4-2 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be V_{IL} or V_{IH} .

If CE# is driven active high during a Hold condition, the device returns to standby mode. The device can then be re-initiated with the command sequences listed in Table 5-1. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active high, and CE# must be driven active low. See Figure 4-2 for Hold timing.

FIGURE 4-2: HOLD CONDITION WAVEFORM



4.1 Write Protection

SST25PF040C provides software Write protection. The Write-Protect pin (WP#) enables or disables the lock-down function of the STATUS register. The Block Protection bits (BP0, BP1, BP2, TB, and BPL) in the STATUS register provide Write protection to the memory array and the STATUS register. See Table 4-3 for the Block-Protection description.

4.1.1 WRITE-PROTECT PIN (WP#)

The Write-Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the STATUS register. When WP# is driven low, the execution of the Write STATUS Register (WRSR) instruction is determined by the value of the BPL bit (see Table 4-1). When WP# is high, the lock-down function of the BPL bit is disabled.

TABLE 4-1: CONDITIONS TO EXECUTE WRITE STATUS REGISTER (WRSR) INSTRUCTION

WP#	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

4.2 STATUS Register

The software STATUS register provides status on whether the flash memory array is available for any read or write operation, whether the device is Write enabled, and the state of the Memory Write protection.

During an internal erase or program operation, the STATUS register may be read only to determine the completion of an operation in progress. [Table 4-2](#) describes the function of each bit in the software STATUS register.

TABLE 4-2: SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	Write operation status 1 = Internal write operation is in progress 0 = No internal write operation is in progress	0	R
1	WEL	Write Enable Latch status 1 = Device is memory write-enabled 0 = Device is not memory write-enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 4-3)	0 or 1	R/W
3	BP1 ⁽¹⁾	Indicate current level of block write protection (See Table 4-3)	0 or 1	R/W
4	BP2 ⁽¹⁾	Indicate current level of block write protection (See Table 4-3)	0 or 1	R/W
5	TB ⁽¹⁾	1 = 1/8, 1/4, or 1/2 Bottom Memory Blocks are protected (See Table 4-3) 0 = 1/8, 1/4, or 1/2 Top Memory Blocks are protected	0 or 1	R/W
6	RES	Reserved for future use	0	N/A
7	BPL ⁽¹⁾	1 = BP0, BP1, BP2, TB, and BPL are read-only bits 0 = BP0, BP1, BP2, TB, and BPL are read/writable	0 or 1	R/W

Note 1: BP0, BP1, BP2, TB, and BPL bits are non-volatile memory bits.

4.2.1 BUSY (BIT 0)

The BUSY bit determines whether there is an internal Erase or Program operation in progress. A '1' for the BUSY bit indicates the device is busy with an operation in progress. A '0' indicates the device is ready for the next valid operation.

4.2.2 WRITE ENABLE LATCH (WEL—BIT 1)

The Write-Enable Latch bit indicates the status of the internal Write-Enable Latch memory. If the WEL bit is set to '1', it indicates the device is Write enabled. If the bit is set to '0' (reset), it indicates the device is not Write enabled and does not accept any Write (Program/Erase) commands. The Write-Enable-Latch bit is automatically reset under the following conditions:

- Power-Up
- Write Disable (WRDI) instruction completion
- Page Program instruction completion
- Sector Erase instruction completion
- 64-Kbyte Block Erase instruction completion
- Chip Erase instruction completion
- Write STATUS Register instruction completion

4.2.3 BLOCK PROTECTION (BP0, BP1, BP2, AND TB—BITS 2, 3, 4, AND 5)

The Block Protection (BP0, BP1, BP2, and TB) bits define the size of the memory area to be software protected against any memory Write (Program or Erase) operation, see [Table 4-3](#). The Write STATUS Register (WRSR) instruction is used to program the BP0, BP1, BP2, and TB bits as long as WP# is high or the Block Protect Lock (BPL) bit is '0'. Chip Erase can only be executed if Block Protection bits are all '0'. BP0, BP1, and BP2 select the protected area and TB allocates the protected area to the higher-order address area (Top Blocks) or lower-order address area (Bottom Blocks).

SST25PF040C

4.2.4 BLOCK PROTECTION LOCK-DOWN (BPL-BIT 7)

When the WP# pin is driven low (V_{IL}), it enables the Block Protection Lock-Down (BPL) bit. When BPL is set to '1', it prevents any further alteration of the BP0,

BP1, BP2, TB, and BPL bits. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect and its value is 'Don't Care'.

TABLE 4-3: SOFTWARE STATUS REGISTER BLOCK PROTECTION

Protection Level	STATUS Register Bit				Protected Memory Address
	TB	BP2	BP1	BP0	
0 (Full Memory Array unprotected)	X	0	0	0	None
T1 (1/8 Top Memory Block protected)	0	0	0	1	070000H-07FFFFH
T2 (1/4 Top Memory Block protected)	0	0	1	0	060000H-07FFFFH
T3 (1/2 Top Memory Block protected)	0	0	1	1	040000H-07FFFFH
B1 (1/8 Bottom Memory Block protected)	1	0	0	1	000000H-00FFFFH
B2 (1/4 Bottom Memory Block protected)	1	0	1	0	000000H-01FFFFH
B3 (1/2 Bottom Memory Block protected)	1	0	1	1	000000H-03FFFFH
4 (Full Memory Block protected)	X	1	X	X	000000H-07FFFFH

5.0 INSTRUCTIONS

Instructions are used to read, write (erase and program), and configure the SST25PF040C devices. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. The Write Enable (\overline{WREN}) instruction must be executed prior to Sector Erase, Block Erase, Page Program, Write STATUS Register, or Chip Erase instructions. The complete instructions are provided in Table 5-1. All instructions are synchronized off a high-to-low transition of CE#. Inputs will be accepted on the rising edge of SCK start-

ing with the most significant bit. CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID, and Read STATUS Register instructions). Any low-to-high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to standby mode. Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSb) first.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS

Instruction	Description	Op Code Cycle ⁽¹⁾	Address Cycle(s) ⁽²⁾	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞	25 MHz

- Note 1:** One bus cycle is eight clock periods.
- 2:** Address bits above the most significant bit of each density can be VIL or VIH.
- 3:** One bus cycle is four clock periods in Dual Operation.
- 4:** 4-Kbyte Sector Erase addresses: use AMS-A12, remaining addresses are don't care but must be set either at VIL or VIH.
- 5:** 64-Kbyte Block Erase addresses: use AMS-A16, remaining addresses are don't care but must be set either at VIL or VIH.
- 6:** The Read STATUS Register is continuous with ongoing clock cycles until terminated by a low-to-high transition on CE#.
- 7:** Device ID is read after three dummy address bytes. The Device ID output stream is continuous until terminated by a low-to-high transition on CE#.
- 8:** The instructions Release from Deep Power down and Read-ID are similar instructions (ABH). Executing Read-ID requires the ABH instruction, followed by 24 dummy address bits to retrieve the Device ID. Release from Deep Power-Down only requires the instruction ABH.

SST25PF040C

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS (CONTINUED)

Instruction	Description	Op Code Cycle ⁽¹⁾	Address Cycle(s) ⁽²⁾	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
High-Speed Read	Read Memory at Higher Speed	0000 1011b (0BH)	3	1	1 to ∞	40 MHz
Fast-Read Dual-Output	Read Memory with Dual Output	0011 1011b (3BH)	3	1 ⁽³⁾	1 to ∞ ⁽³⁾	
Fast-Read Dual I/O	Read Memory with Dual Address Input and Data Output	1011 1011b (BBH)	3 ⁽³⁾	1 ⁽³⁾	1 to ∞ ⁽³⁾	
4-Kbyte Sector-Erase ⁽⁴⁾	Erase 4 -Kbyte of memory array	0010 0000b (20H) 1101 0111b (D7H)	3	0	0	
64-Kbyte Block-Erase ⁽⁵⁾	Erase 64-Kbyte block of memory array	1101 1000b (D8H)	3	0	0	
Chip-Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0	
Page Program	To program up to 256 Bytes	0000 0010b (02H)	3	0	1 to 256	
RDSR ⁽⁶⁾	Read STATUS Register	0000 0101b (05H)	0	0	1 to ∞	
WRSR	Write STATUS Register	0000 0001b (01H)	0	0	1	
WREN	Write Enable	0000 0110b (06H)	0	0	0	
WRDI	Write Disable	0000 0100b (04H)	0	0	0	
RDID ^(7, 8)	Read-ID	1010 1011b (ABH)	3	0	1 to ∞	
JEDEC-ID	JEDEC ID Read	1001 1111b (9FH)	0	0	4 to ∞	
DPD	Deep Power-Down Mode	1011 1001b (B9H)	0	0	0	
RDPD ⁽⁸⁾	Release from Deep Power-Down or Read ID	1010 1011b (ABH)	0	0	0	

Note 1: One bus cycle is eight clock periods.

2: Address bits above the most significant bit of each density can be V_{IL} or V_{IH}.

3: One bus cycle is four clock periods in Dual Operation.

4: 4-Kbyte Sector Erase addresses: use AMS-A12, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.

5: 64-Kbyte Block Erase addresses: use AMS-A16, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.

6: The Read STATUS Register is continuous with ongoing clock cycles until terminated by a low-to-high transition on CE#.

7: Device ID is read after three dummy address bytes. The Device ID output stream is continuous until terminated by a low-to-high transition on CE#.

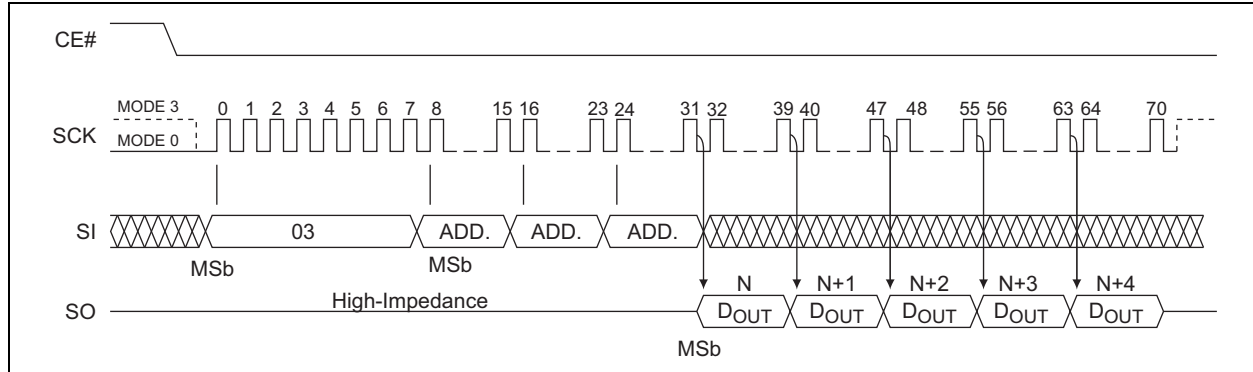
8: The instructions Release from Deep Power down and Read-ID are similar instructions (ABH). Executing Read-ID requires the ABH instruction, followed by 24 dummy address bits to retrieve the Device ID. Release from Deep Power-Down only requires the instruction ABH.

5.1 Read (25 MHz)

The Read instruction, 03H, supports up to 25 MHz Read. The device outputs a data stream starting from the specified address location. The data stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached. Once the highest memory address is reached, the address pointer automatically incre-

ments to the beginning (wrap-around) of the address space. For example, for 4 Mbit density, once the data from the address location 7FFFFH is read, the next output is from address location 000000H. The READ instruction is initiated by executing an 8-bit command, 03H, followed by address bits A23-A0. CE# must remain active low for the duration of the Read cycle. See [Figure 5-1](#) for the Read sequence.

FIGURE 5-1: READ SEQUENCE



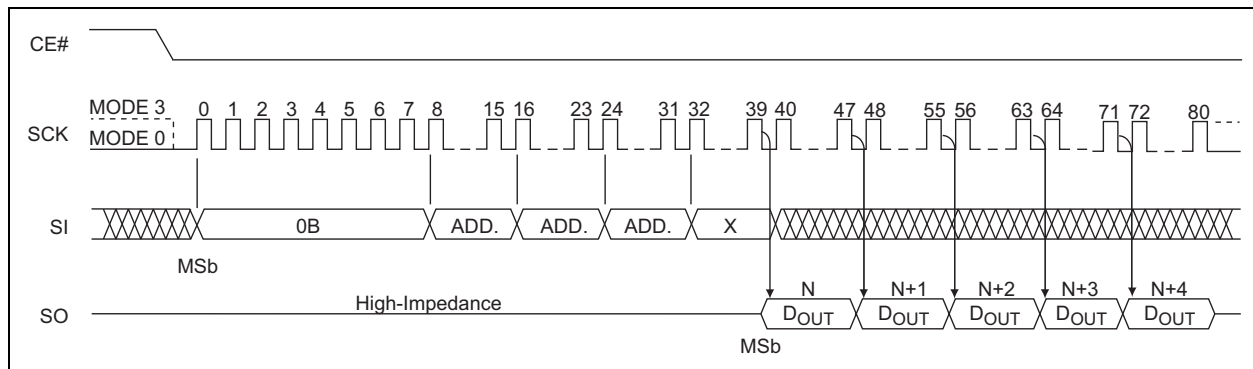
5.2 High-Speed Read (40 MHz)

The High-Speed Read instruction supporting up to 40 MHz Read is initiated by executing an 8-bit command, 0BH, followed by address bits [A23-A0] and a dummy byte. CE# must remain active low for the duration of the High-Speed Read cycle. See [Figure 5-2](#) for the High-Speed Read sequence.

through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. For example, for 4-Mbit density, once the data from address location 7FFFFH is read, the next output will be from address location 000000H.

Following a dummy cycle, the High-Speed Read instruction outputs the data starting from the specified address location. The data output stream is continuous

FIGURE 5-2: HIGH-SPEED READ SEQUENCE



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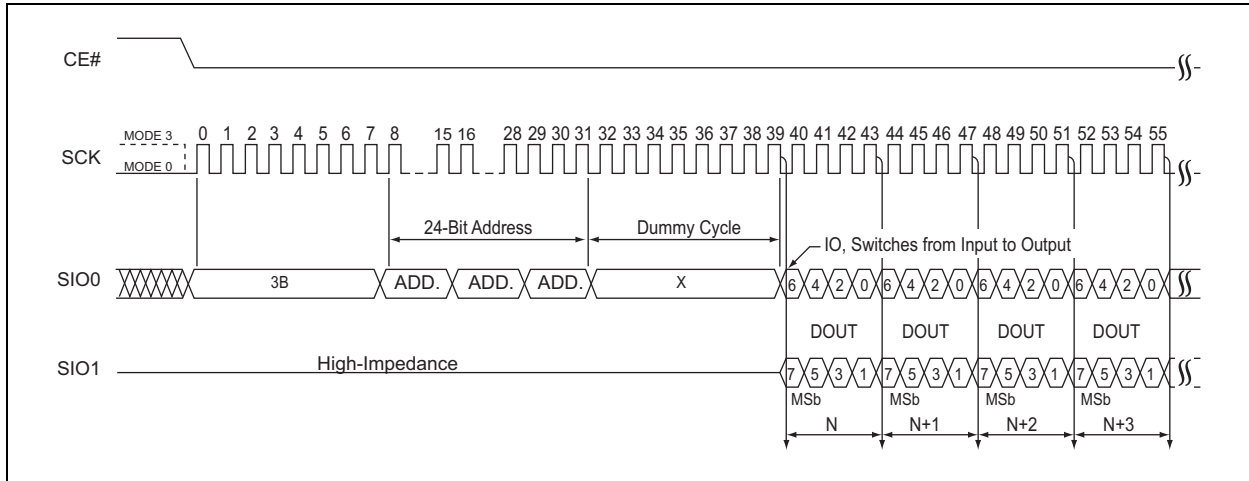
5.3 Fast-Read Dual Output (40 MHz)

The Fast-Read Dual-Output (3BH) instruction outputs data up to 40 MHz from the SIO0 and SIO1 pins. To initiate the instruction, execute an 8-bit command (3BH) followed by address bits A23-A0 and a dummy byte on SI/SIO0. Following a dummy cycle, the Fast-Read Dual-Output instruction outputs the data starting from the specified address location on the SIO1 and SIO0 lines. SIO1 outputs, per clock sequence, odd data bits D7, D5, D3, and D1; and SIO0 outputs even data bits D6, D4, D2, and D0. CE# must remain active-low for

the duration of the Fast-Read Dual-Output instruction cycle. See Figure 5-3 for the Fast-Read Dual-Output sequence.

The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer automatically increments to the beginning (wraparound) of the address space. For 4-Mbit density, once the data from address location 7FFFFH has been read the next output will be from address location 000000H.

FIGURE 5-3: FAST-READ DUAL OUTPUT SEQUENCE



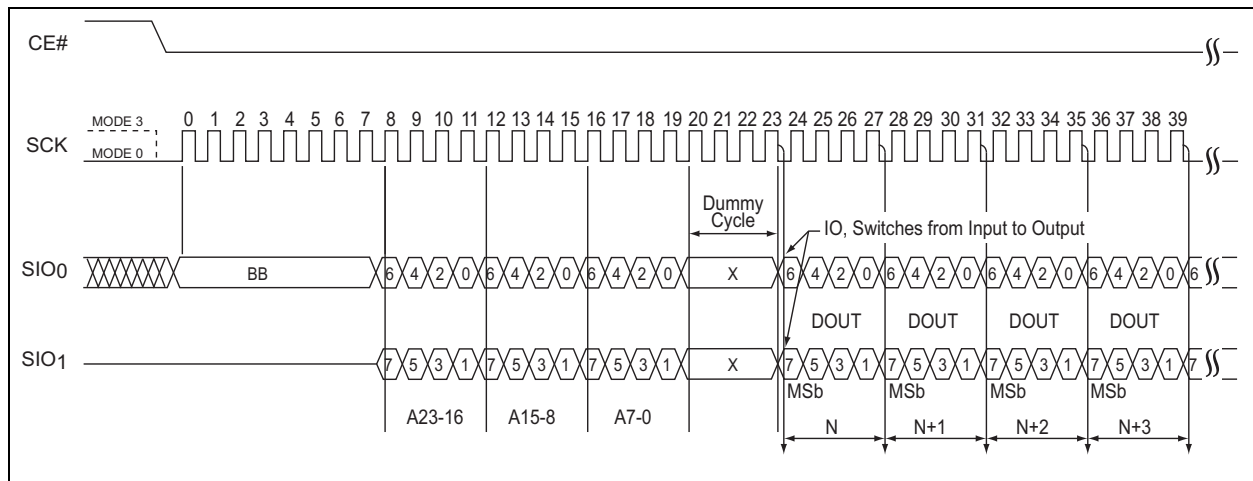
5.4 Fast-Read Dual I/O (40 MHz)

The Fast-Read Dual I/O (BBH) instruction reduces the total number of input clock cycles, which results in faster data access. The device is first selected by driving Chip Enable CE# low. Fast-Read Dual I/O is initiated by executing an 8-bit command (BBH) on SI/SIO₀, thereafter, the device accepts address bits A23-A0 and a dummy byte on SI/SIO₀ and SO/SIO₁. It offers the capability to input address bits A23-A0 at a rate of two bits per clock. Odd address bits A23 through A1 are input on SIO₁ and even address bits A22 through A0 are input on SIO₀, alternately. For example, the most significant bit is input first followed by A23/22, A21/A20, and so on. Each bit is latched at the same rising edge of the Serial Clock (SCK). The input data during the dummy clocks is “don't care”. However, the SIO₀ and SIO₁ pin must be in high-impedance prior to the falling edge of the first data output clock.

Following a dummy cycle, the Fast-Read Dual I/O instruction outputs the data starting from the specified address location on the SIO₁ and SIO₀ lines. SIO₁ outputs, per clock sequence, odd data bits D7, D5, D3, and D1; and SIO₀ outputs even data bits D6, D4, D2, and D0 per clock edge. CE# must remain active low for the duration of the Fast-Read Dual I/O instruction cycle. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer automatically increments to the beginning (wraparound) of the address space. For example, once the data from address location 7FFFFH is read, the next output is from address location 000000H. See [Figure 5-4](#) for the Fast-Read Dual I/O sequence.

FIGURE 5-4: FAST-READ DUAL I/O SEQUENCE



SST25PF040C

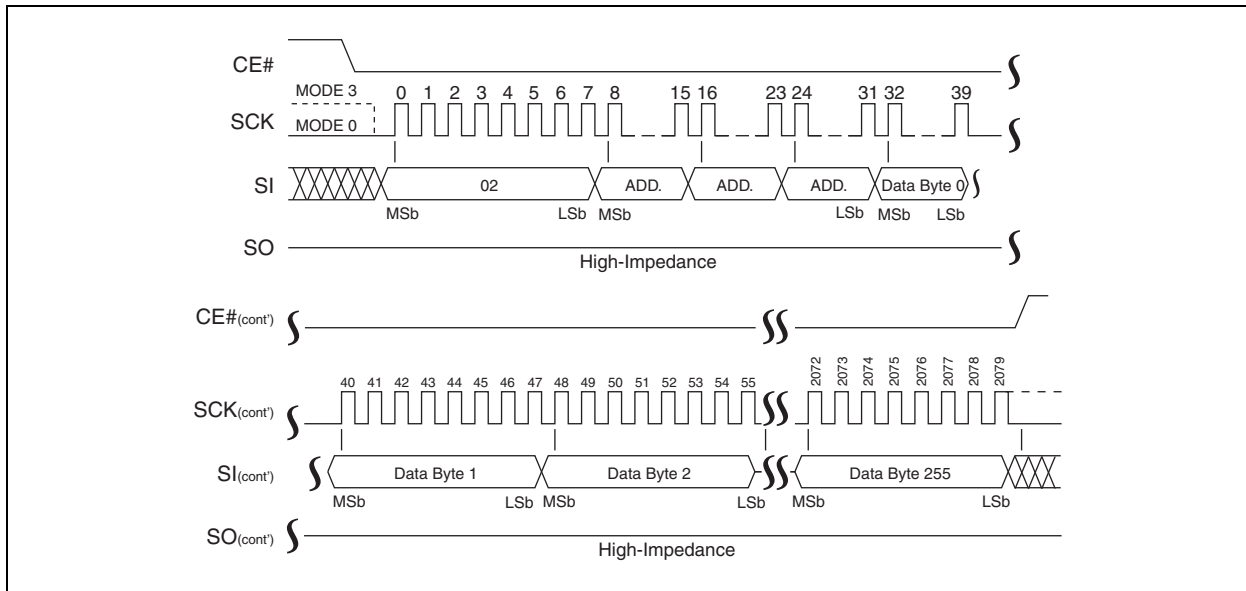
5.5 Page Program

The Page Program instruction programs up to 256 bytes of data in the memory. The data for the selected page address must be in the erased state (FFH) before initiating the Page-Program operation. A Page Program applied to a protected memory area will be ignored. Prior to the program operation, execute the WREN instruction.

To execute a Page Program operation, the host drives CE# low, then sends the Page Program command cycle (02H), three address cycles, followed by the data to be programmed, and then drives CE# high. The programmed data must be between 1 to 256 bytes and in whole byte increments; sending less than a full byte will cause the partial byte to be ignored. Poll the BUSY bit in the STATUS register, or wait TPP, for the completion of the internal, self-timed, Page Program operation. See Figure 5-5 for the Page Program sequence and Figure 6-8 for the Page Program flow chart.

When executing Page Program, the memory range for the SST25PF040C is divided into 256-byte page boundaries. The device handles the shifting of more than 256 bytes of data by maintaining the last 256 bytes as the correct data to be programmed. If the target address for the Page Program instruction is not the beginning of the page boundary (A[7:0] are not all zero), and the number of bytes of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.

FIGURE 5-5: PAGE PROGRAM SEQUENCE

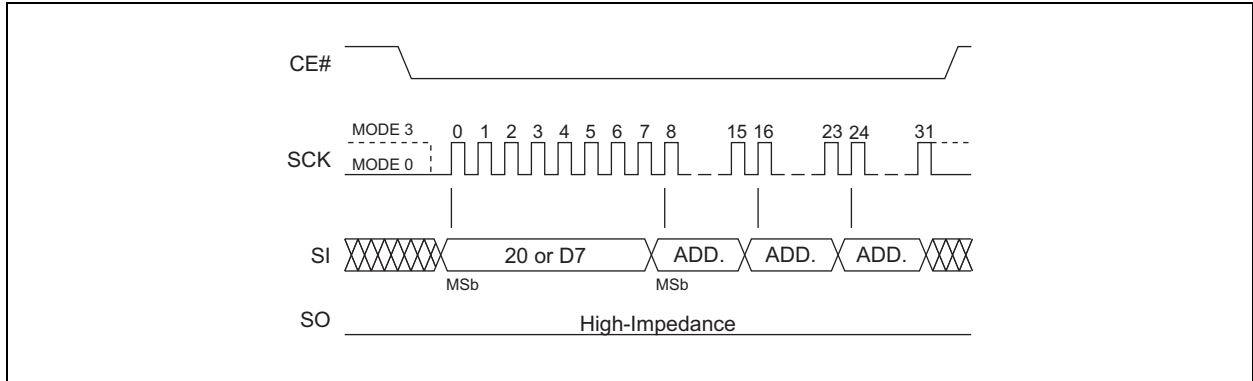


5.6 Sector Erase

The Sector-Erase instruction clears all bits in the selected 4-Kbyte sector to FFH. A Sector Erase instruction applied to a protected memory area will be ignored. Prior to any write operation, the Write Enable (\overline{WREN}) instruction must be executed. CE# must remain active low for the duration of any command sequence. The Sector Erase instruction is initiated by executing an 8-bit command, 20H or D7H, followed by address

bits [A23-A0]. Address bits [AMS-A12] (AMS = Most Significant address) are used to determine the sector address (SAX), remaining address bits can be V_{IL} or V_{IH} . CE# must be driven high before the instruction is executed. Poll the BUSY bit in the Software STATUS register, or wait T_{SE} , for the completion of the internal self-timed Sector Erase cycle. See Figure 5-6 for the Sector Erase sequence and Figure 6-9 for the flow chart.

FIGURE 5-6: SECTOR ERASE SEQUENCE



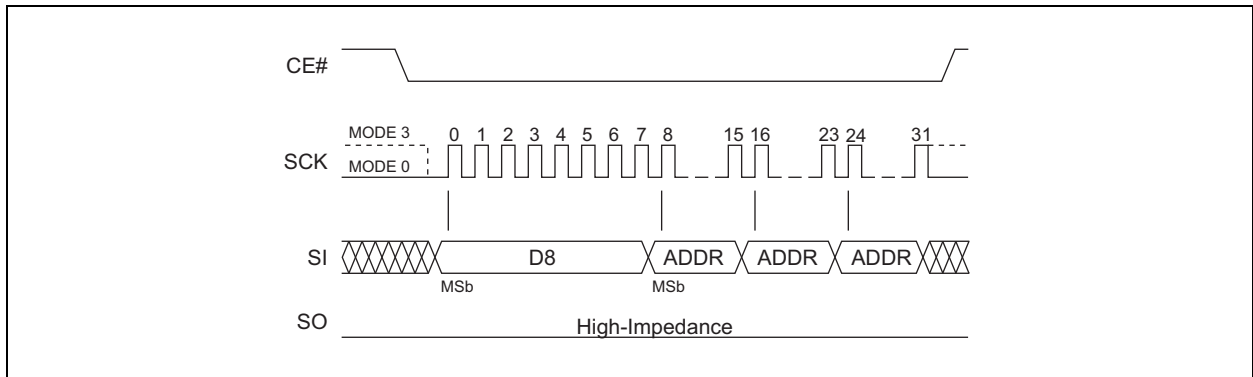
5.7 64-KByte Block Erase

The 64-Kbyte Block Erase instruction clears all bits in the selected 64-Kbyte block to FFH. Applying this instruction to a protected memory area results in the instruction being ignored. Prior to any write operation, the Write-Enable (\overline{WREN}) instruction must be executed. CE# must remain active low for the duration of any command sequence.

[A23-A0]. Address bits [AMS-A16] (AMS = Most Significant Address) determine the block address (BA_X), remaining address bits can be V_{IL} or V_{IH} . CE# must be driven high before executing the instruction. Poll the BUSY bit in the software STATUS register or wait T_{BE} for the completion of the internal self-timed Block-Erase cycle. See Figure 5-7 for the 64-Kbyte Block Erase sequences and Figure 6-9 for the flow chart.

Initiate the 64-Kbyte Block Erase instruction by executing an 8-bit command, D8H, followed by address bits

FIGURE 5-7: 64-KBYTE BLOCK ERASE SEQUENCE



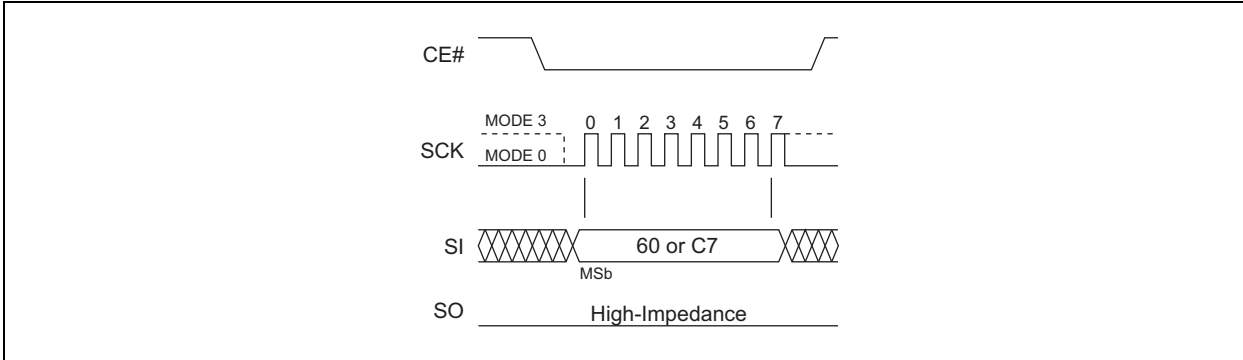
SST25PF040C

5.8 Chip Erase

The Chip Erase instruction clears all bits in the device to FFH. A Chip Erase instruction is ignored if any of the memory area is protected. Prior to any write operation, the Write Enable (*WREN*) instruction must be executed. *CE#* must remain active low for the duration of the Chip Erase instruction sequence. Initiate the Chip Erase

instruction by executing an 8-bit command, 60H or C7H. *CE#* must be driven high before the instruction is executed. Poll the *BUSY* bit in the software *STATUS* register, or wait *TSCE*, for the completion of the internal self-timed Chip Erase cycle. See [Figure 5-8](#) for the Chip Erase sequence and [Figure 6-10](#) for the flow chart.

FIGURE 5-8: CHIP ERASE SEQUENCE

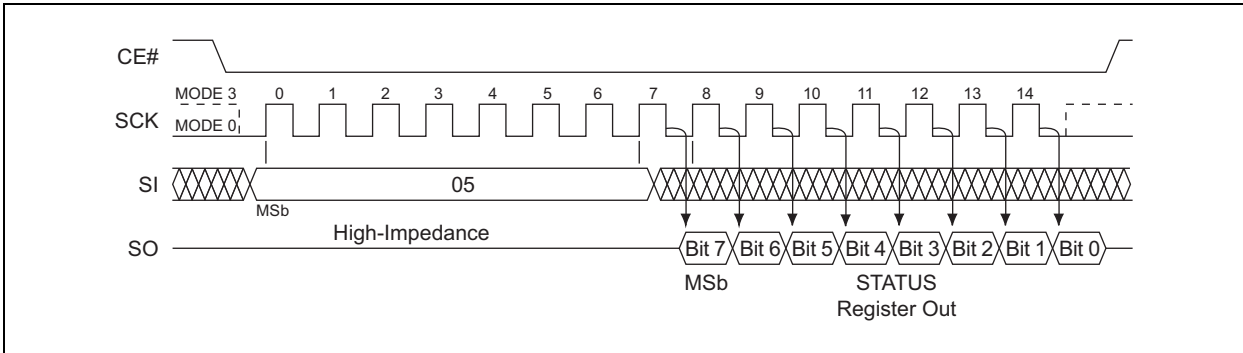


5.9 Read STATUS Register (RDSR)

The Read STATUS Register (*RDSR*) instruction, 05H, allows reading of the STATUS register. The STATUS register may be read at any time even during a Write (Program/Erase) operation. When a write operation is in progress, the *BUSY* bit may be checked before sending any new commands to assure that the new commands are properly received by the device. *CE#*

must be driven low before the *RDSR* instruction is entered and remain low until the status data is read. Read STATUS Register is continuous with ongoing clock cycles until it is terminated by a low-to-high transition of the *CE#*. See [Figure 5-9](#) for the *RDSR* instruction sequence.

FIGURE 5-9: READ STATUS REGISTER (RDSR) SEQUENCE

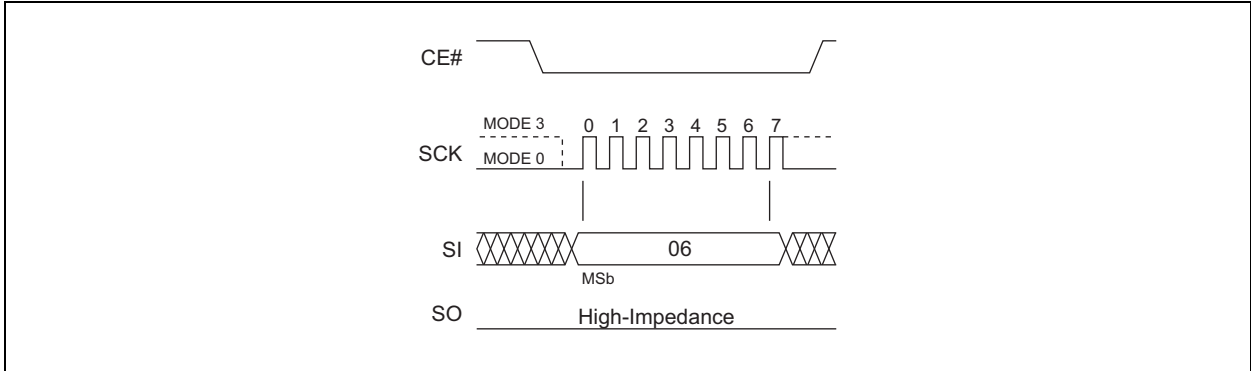


5.10 Write Enable (WREN)

The Write Enable (WREN) instruction, 06H, sets the Write Enable Latch bit in the STATUS Register to '1' allowing write operations to occur. The WREN instruction must be executed prior to any Write (Program/Erase) operation. The WREN instruction may also be used to allow execution of the Write STATUS Register (WRSR)

instruction; however, the Write Enable Latch bit in the STATUS Register will be cleared upon the rising edge CE# of the WRSR instruction. CE# must be driven low before entering the WREN instruction, and CE# must be driven high before executing the WREN instruction. See [Figure 5-10](#) for the WREN instruction sequence.

FIGURE 5-10: WRITE ENABLE (WREN) SEQUENCE

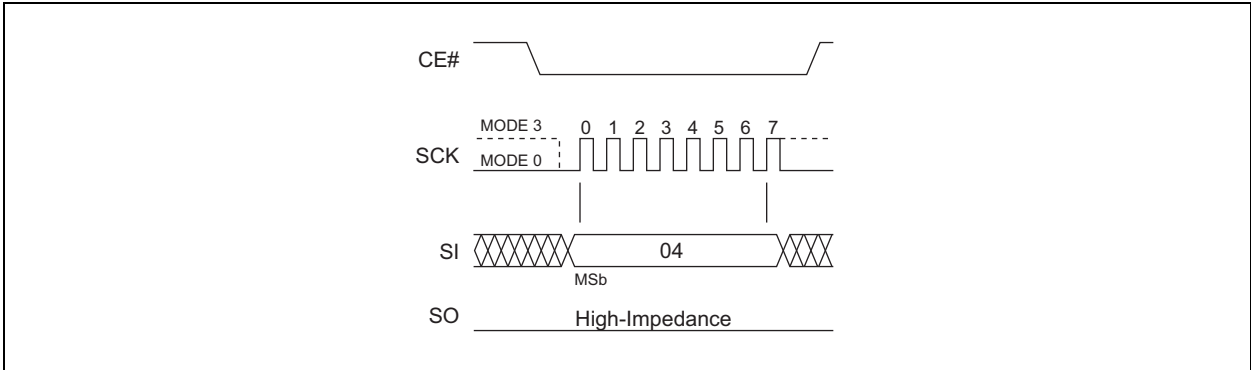


5.11 Write Disable (WRDI)

The Write Disable (WRDI) instruction, 04H, resets the Write Enable Latch bit to '0', thus preventing any new Write operations. CE# must be driven low before entering the WRDI instruction, and CE# must be driven high before executing the WRDI instruction. See [Figure 5-11](#)

for the WRDI instruction sequence.

FIGURE 5-11: WRITE DISABLE (WRDI) SEQUENCE



SST25PF040C

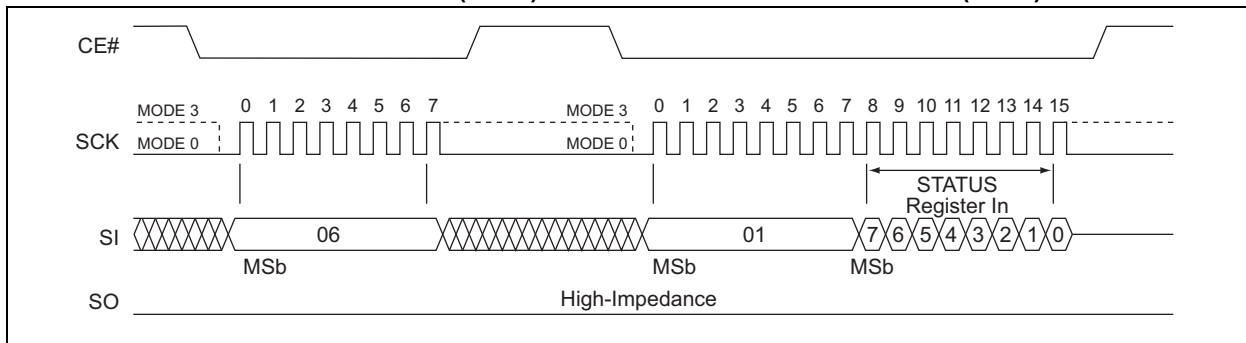
5.12 Write STATUS Register (WRSR)

The Write STATUS Register instruction writes new values to the BP0, BP1, BP2, TB, and BPL bits of the status register. CE# must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. Poll the BUSY bit in the Software STATUS register, or wait TWRSR, for the completion of the internal, self-timed Write STATUS Register cycle. See Figure 5-12 for WREN and WRSR instruction sequences and Figure 6-11 for the WRSR flow chart.

Executing the Write STATUS Register instruction will be ignored when WP# is low and BPL bit is set to '1'. When the WP# is low, the BPL bit can only be set from

'0' to '1' to lock-down the status register, but cannot be reset from '1' to '0'. When WP# is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, BP1, BP2, and TB bits in the STATUS register can all be changed. As long as BPL bit is set to '0' or WP# pin is driven high (VIH) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the bits in the status register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to '1' to lock down the status register as well as altering the BP0, BP1, BP2, and TB bits at the same time. See Table 4-1 for a summary description of WP# and BPL functions.

FIGURE 5-12: WRITE-ENABLE (WREN) AND WRITE-STATUS-REGISTER (WRSR) SEQUENCE



5.13 Power-Down

The Deep Power-Down (DPD) instruction puts the device in the lowest power consumption mode – the Deep Power-Down mode. This instruction is ignored if the device is busy with an internal write operation. While the device is in DPD mode, all instructions are ignored except for the Release Deep Power-Down instruction or Read ID.

To initiate deep power-down, input the Deep Power-Down instruction (B9H) while driving CE# low. CE# must be driven high before executing the DPD instruction. After driving CE# high, the device requires a delay

of TDPD before the standby current I_{SB} is reduced to the deep power-down current I_{DPD}. See Figure 5-13 for the DPD instruction sequence.

Exit the power-down state using the Release from Deep Power-Down or Read ID instruction. CE# must be driven low before sending the Release from Deep Power-Down command cycle (ABH), and then driving CE# high. The device will return to Standby mode and be ready for the next instruction after T_{SBR}. See Figure 5-14. for the Release from Deep Power-Down sequence.

FIGURE 5-13: DEEP POWER-DOWN SEQUENCE

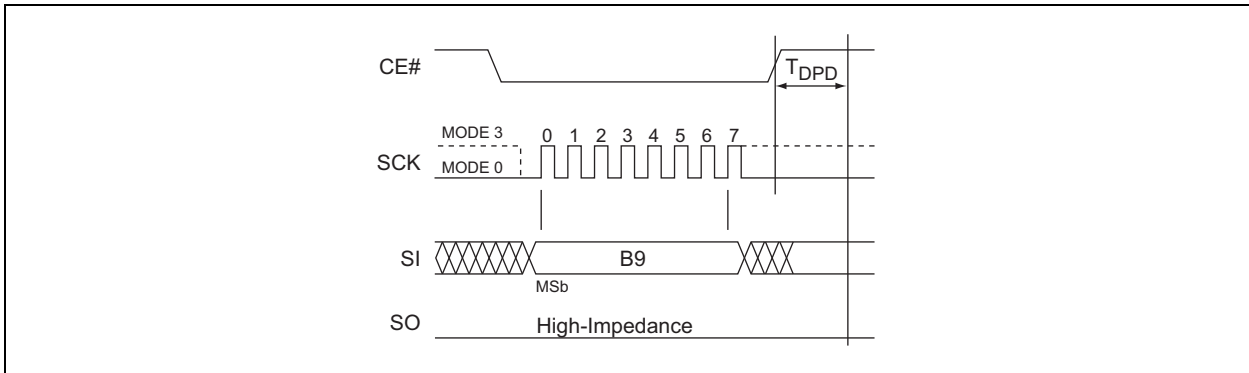
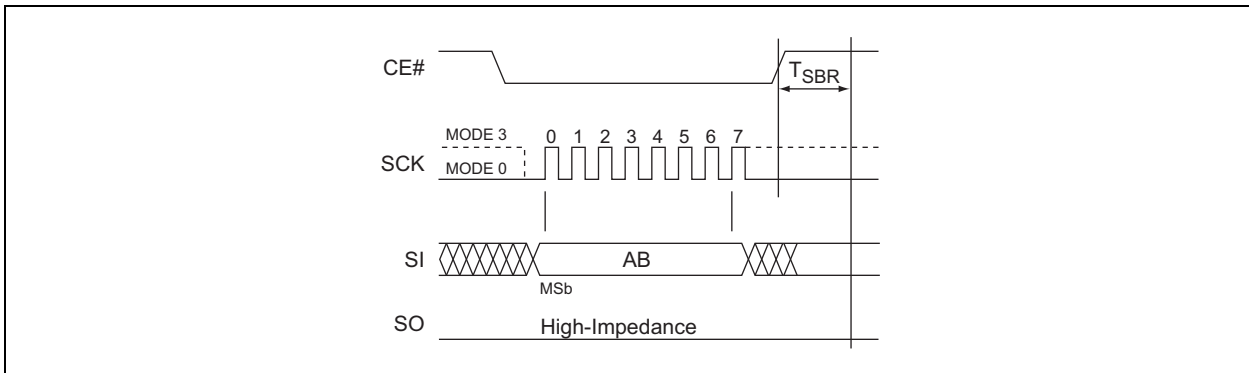


FIGURE 5-14: RELEASE FROM DEEP POWER-DOWN SEQUENCE



SST25PF040C

5.14 Read-ID

The Read-ID instruction identifies the device as SST25PF040C. Use the Read-ID instruction to identify SST25PF040C when using multiple manufacturers in the same socket. See [Table 5-2](#).

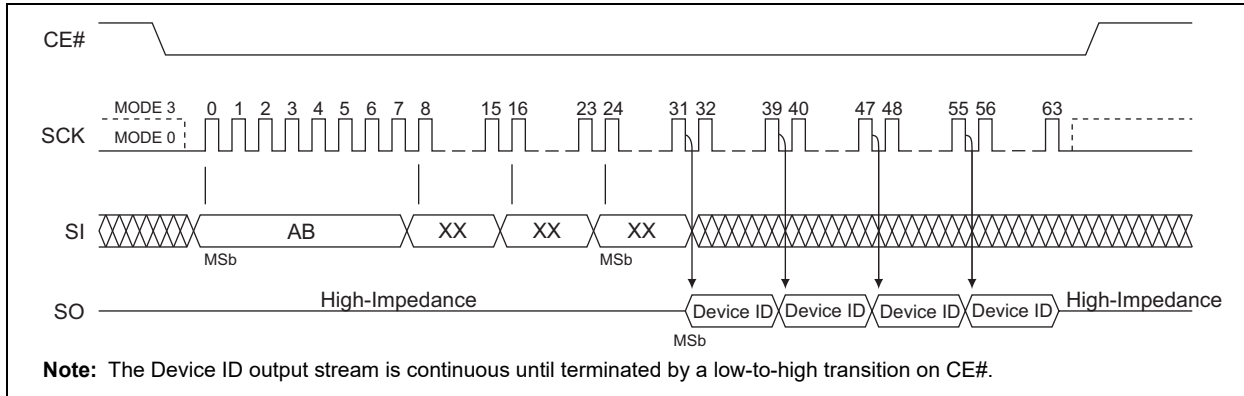
The device ID information is read by executing an 8-bit

command, ABH, followed by 24 dummy address bits. Following the Read-ID instruction, and 24 address dummy bits, the device ID continues to output with continuous clock input until terminated by a low-to-high transition on CE#.

TABLE 5-2: PRODUCT IDENTIFICATION

Device ID	Address	Data
SST25PF040C ID	XXXXXXH	6EH

FIGURE 5-15: READ-ID SEQUENCE



5.15 JEDEC Read-ID

The JEDEC Read-ID instruction identifies the device ID information of SST25PF040C. The device information can be read by executing the 8-bit command, 9FH. Following the JEDEC Read-ID instruction, 32-bit device ID information is output from the device. The Device ID information is assigned by the manufacturer and contains the Device ID 1 in the first byte, the type of mem-

ory in the second byte, the memory capacity of the device in the third byte, and a reserved code in the fourth byte. The 4-byte code outputs repeatedly with continuous clock input until a low-to-high transition on CE#. See [Figure 5-16](#) for the instruction sequence. The JEDEC Read ID instruction is terminated by a low-to-high transition on CE# at any time during data output.

FIGURE 5-16: JEDEC READ-ID SEQUENCE

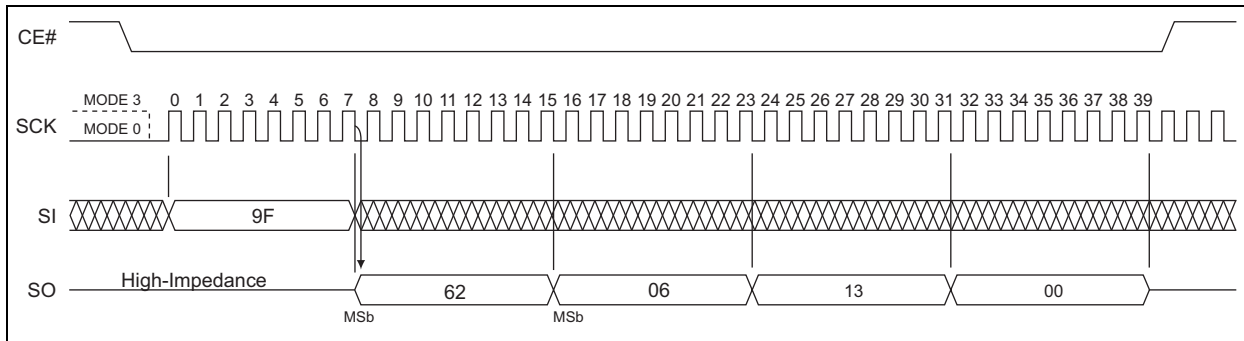


TABLE 5-3: JEDEC READ-ID DATA-OUT

Product	Device ID			
	Device ID 1 (Byte 1)	Memory Type (Byte 2)	Memory Capacity (Byte 3)	Reserved Code (Byte 4)
SST25PF040C	62H	06H	13H	00H

6.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias	-55°C to +125°C
Storage temperature	-55°C to +150°C
DC voltage on any pin to ground potential	-0.5V to V _{DD} +0.5V
Transient voltage (<20 ns) on any pin to ground potential	-2.0V to V _{DD} +2.0V
Package power dissipation capability (T _A = 25°C).....	1.0W
Surface mount solder reflow temperature	260°C for 10 seconds
Output short circuit current ⁽¹⁾	50 mA

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 6-1: OPERATING RANGE

Range	Ambient Temp	V _{DD}
Industrial	-40°C to +85°C	2.3V - 3.6V
Industrial Plus	-40°C to +105°C	2.3V - 3.6V
Extended	-40°C to +125°C	2.3V - 3.6V

6.1 Power-Up Specifications

All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3.3V in less than 330 ms). See [Table 6-3](#) and [Figure 6-2](#) for more information.

TABLE 6-2: AC CONDITIONS OF TEST

Input Rise/Fall Time	Output Load
5 ns	C _L = 30 pF

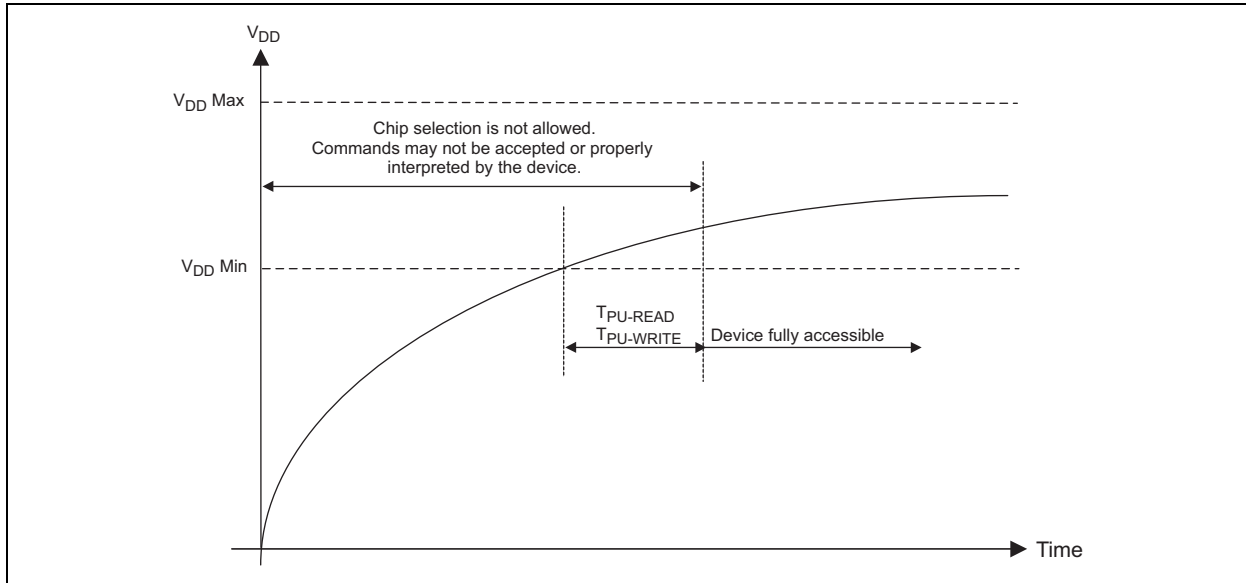
TABLE 6-3: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
TPU-READ	V _{DD} Min to Read Operation	100	µs
TPU-WRITE ⁽¹⁾	V _{DD} Min to Write Operation	100	µs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

SST25PF040C

FIGURE 6-1: POWER-UP TIMING DIAGRAM



6.2 Hardware Data Protection

SST25PF040C provides a power-up reset function. To ensure that the power reset circuit will operate correctly, the device must meet the conditions shown in [Figure 6-2](#) and [Table 6-4](#). Microchip does not guarantee the data in the event of an instantaneous power failure that occurs during a Write operation.

FIGURE 6-2: POWER-DOWN TIMING DIAGRAM

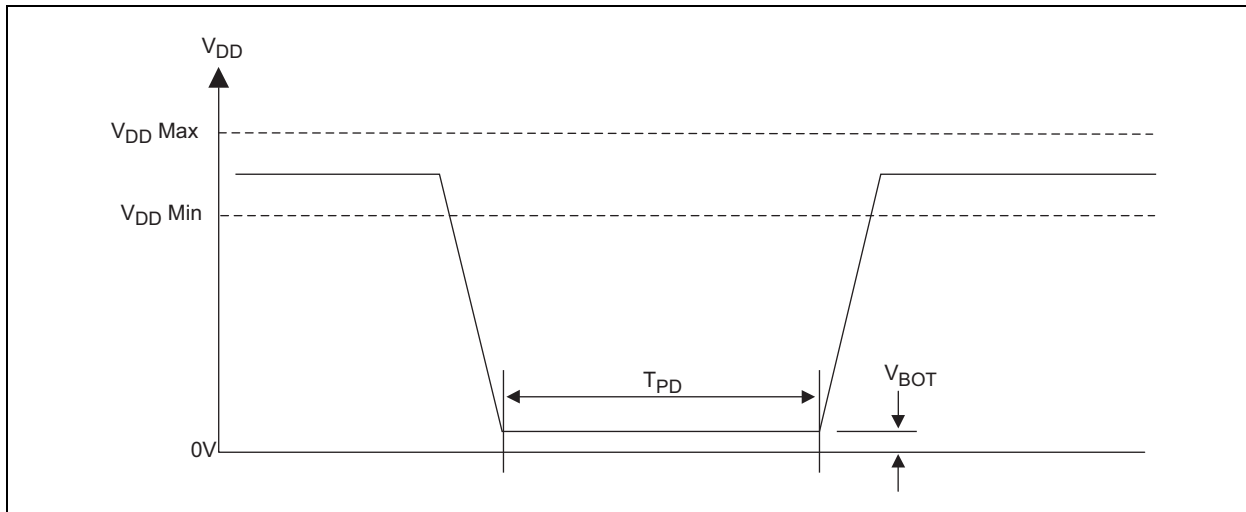


TABLE 6-4: RECOMMENDED SYSTEM POWER-DOWN TIMINGS

Symbol	Parameter	Min	Max	Units
T_{PD}	Power-down time	10	—	ms
V_{BOT}	Power-down voltage	—	0.2	V

6.3 Software Data Protection

SST25PF040C prevents unintentional operations by not recognizing commands under the following conditions:

- After inputting a write command, if the rising CE# edge timing is not in a bus cycle (8 CLK units of SCK)
- When the Page Program data is not in 1-byte increments
- If the Write STATUS Register instruction is input for two bus cycles or more.

6.4 Decoupling Capacitor

A 0.1 μ F ceramic capacitor must be provided for each device and connected between VDD and VSS to ensure that the device will operate correctly.

SST25PF040C

6.5 DC Characteristics

TABLE 6-5: DC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ. ⁽¹⁾	Max.	Units	
IDDR1	Read Current	—	—	6	mA	CE# = 0.1 VDD/0.9 VDD@25 MHz, SO = open; Single I/O
IDDR2	Read Current	—	—	10	mA	CE# = 0.1 VDD/0.9VDD@40 MHz, SO = open
IDDR3	Read Current	—	—	12	mA	CE# = 0.1 VDD/0.9VDD@40 MHz, SO = open; Dual I/O;
IDDW	Program and Erase Current	—	—	15	mA	CE# = VDD
ISB	Standby Current	—	—	50	μA	CE# = VDD, VIN = VDD or VSS
IDPD	Deep Power-Down	—	—	10	μA	CE# = VDD, VIN = VDD or VSS
ILI	Input Leakage Current	—	—	2	μA	VIN = GND to VDD, VDD = VDD Max
ILO	Output Leakage Current	—	—	2	μA	VOUT = GND to VDD, VDD = VDD Max
VIL	Input Low Voltage	-0.3	—	0.3*VDD	V	VDD = VDD Min
VIH	Input High Voltage	0.7*VDD	—	VDD+0.3	V	VDD = VDD Max
VOL	Output Low Voltage	—	—	0.2	V	IOI = 100 μA, VDD = VDD Min
VOH	Output High Voltage	VDD-0.2	—	—	V	IOH = -100 μA, VDD = VDD Min

Note 1: Value characterized, not fully tested in production.

TABLE 6-6: CAPACITANCE (TA = 25°C, F = 1 MHz, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
COUT ⁽¹⁾	Output Pin Capacitance	VOUT = 0V	12 pF
CIN ⁽¹⁾	Input Capacitance	VIN = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-7: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
NEND ⁽¹⁾	Endurance	100,000	Cycles	JEDEC Standard A117
	STATUS Register Write Cycle	100,000	Cycles	JEDEC Standard A117
TDR ⁽¹⁾	Data Retention	20	Years	JEDEC Standard A103
ILTH ⁽¹⁾	Latch Up	100 + IDD	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

6.6 AC Characteristics

TABLE 6-8: AC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits - 25 MHz			Limits - 40 MHz			Units
		Min		Max	Min		Max	
FCLK ⁽¹⁾	Serial Clock Frequency	—	—	25	—	—	40	MHz
TCKH	Serial Clock High Time	18	—	—	11.5	—	—	ns
TCKL	Serial Clock Low Time	18	—	—	11.5	—	—	ns
TCKR	Serial Clock Rise Time	—	—	5	—	—	5	ns
TCKF	Serial Clock Fall Time	—	—	5	—	—	5	ns
TCEs ⁽²⁾	CE# Active Setup Time	8	—	—	8	—	—	ns
TCEH ⁽²⁾	CE# Active Hold Time	8	—	—	8	—	—	ns
TCHS ⁽²⁾	CE# Not Active Setup Time	8	—	—	8	—	—	ns
TCHH ⁽²⁾	CE# Not Active Hold Time	8	—	—	8	—	—	ns
TCPH	CE# High Time	25	—	—	25	—	—	ns
TCHZ	CE# High to High-Z Output	—	—	8	—	—	8	ns
TCLZ	SCK Low to Low-Z Output	0	—	—	0	—	—	ns
TDS	Data In Setup Time	2	—	—	2	—	—	ns
TDH	Data In Hold Time	5	—	—	5	—	—	ns
THLS	HOLD# Low Setup Time	5	—	—	5	—	—	ns
THHS	HOLD# High Setup Time	5	—	—	5	—	—	ns
THLH	HOLD# Low Hold Time	5	—	—	5	—	—	ns
THHH	HOLD# High Hold Time	5	—	—	5	—	—	ns
THZ	HOLD# Low-to-High-Z Output	—	—	9	—	—	9	ns
TLZ	HOLD# High-to-Low-Z Output	—	—	9	—	—	9	ns
TOH	Output Hold from SCK Change	1	—	—	1	—	—	ns
TV	Output Valid from SCK	—	—	11	—	—	11	ns
TWPS	WP# Setup Time	20	—	—	20	—	—	ns
TWPH	WP# Hold Time	20	—	—	20	—	—	ns
TWRSR	STATUS Register Write Time	—	—	10	—	—	15	ms
TDPD	CE# High to Deep Power-Down	—	—	3	—	—	3	µs
TSBR	Deep Power-Down (CE# High) to Standby Mode	—	—	3	—	—	3	µs
TSE	Sector Erase	—	40	150	—	40	150	ms
TBE	Block Erase	—	80	250	—	80	250	ms
TCE	Chip Erase	—	0.25	2	—	0.25	2	s
TPP	Page Program (256 Byte)	—	4	5	—	4	5	ms

Note 1: Maximum clock frequency for Read instruction, 03H, is 25 MHz.

2: Relative to SCK.

SST25PF040C

FIGURE 6-3: SERIAL OUTPUT TIMING DIAGRAM

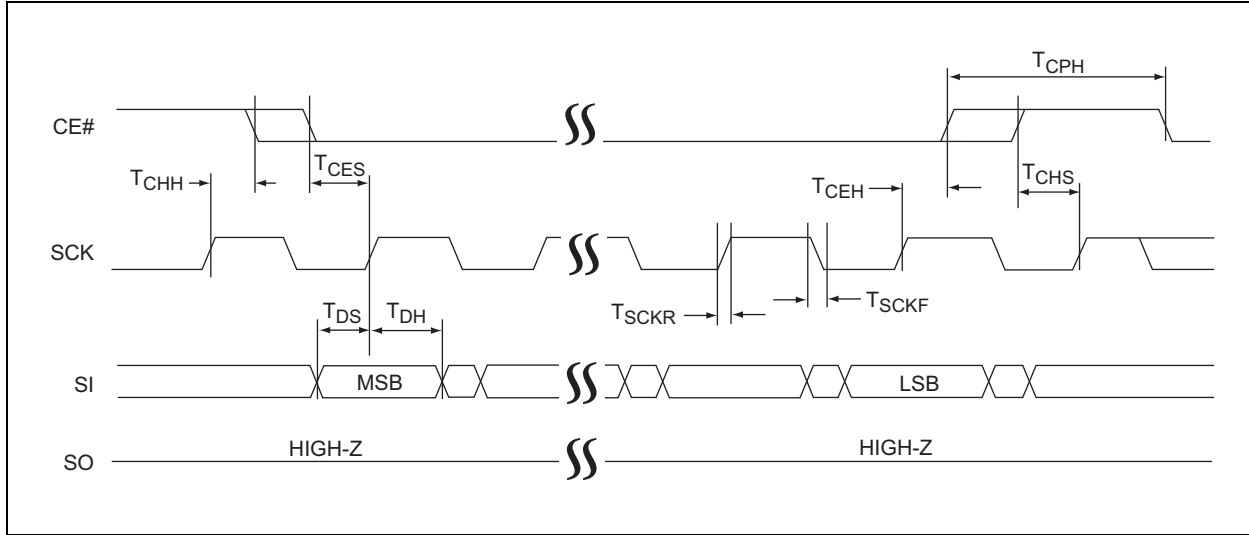


FIGURE 6-4: SERIAL INPUT TIMING DIAGRAM

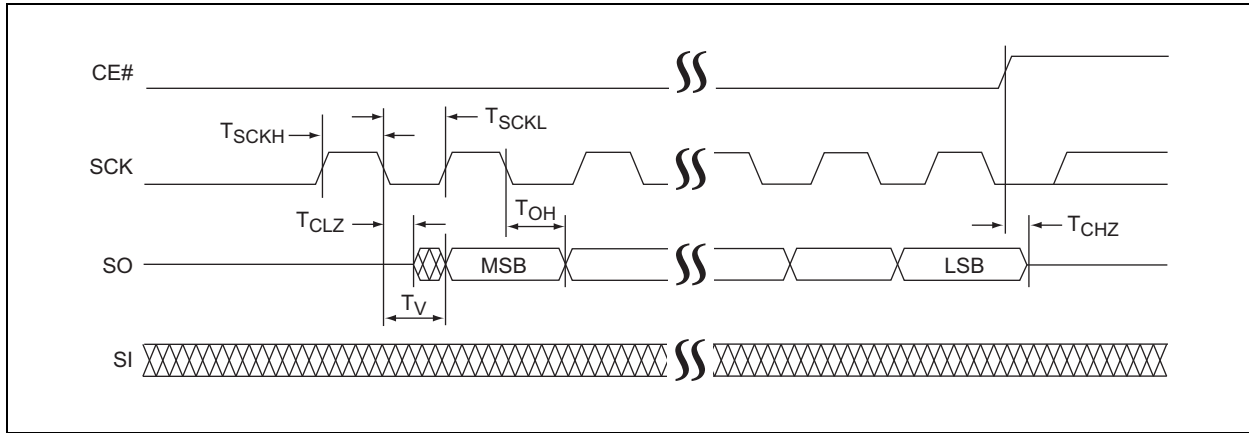


FIGURE 6-5: HOLD TIMING DIAGRAM

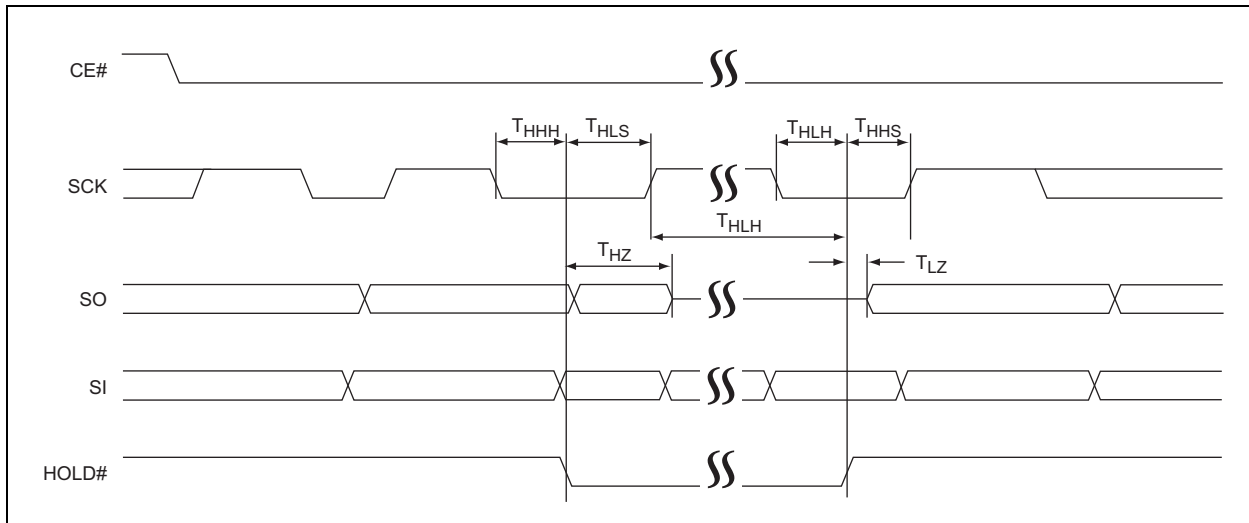


FIGURE 6-6: STATUS REGISTER WRITE TIMING

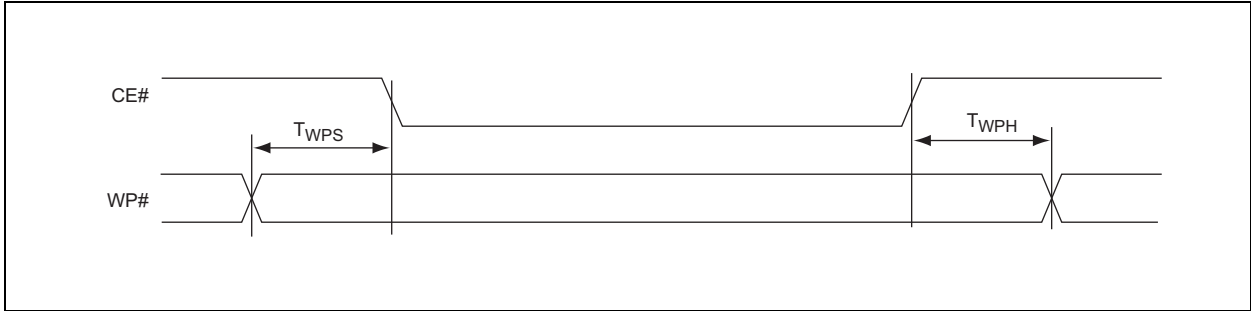
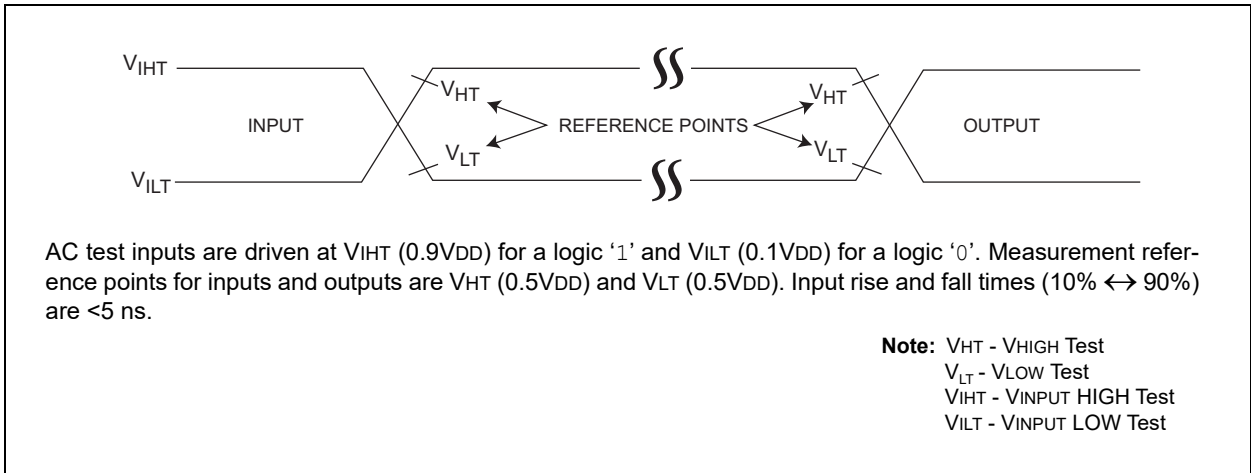


FIGURE 6-7: AC INPUT/OUTPUT REFERENCE WAVEFORMS



SST25PF040C

FIGURE 6-8: PAGE PROGRAM FLOW CHART

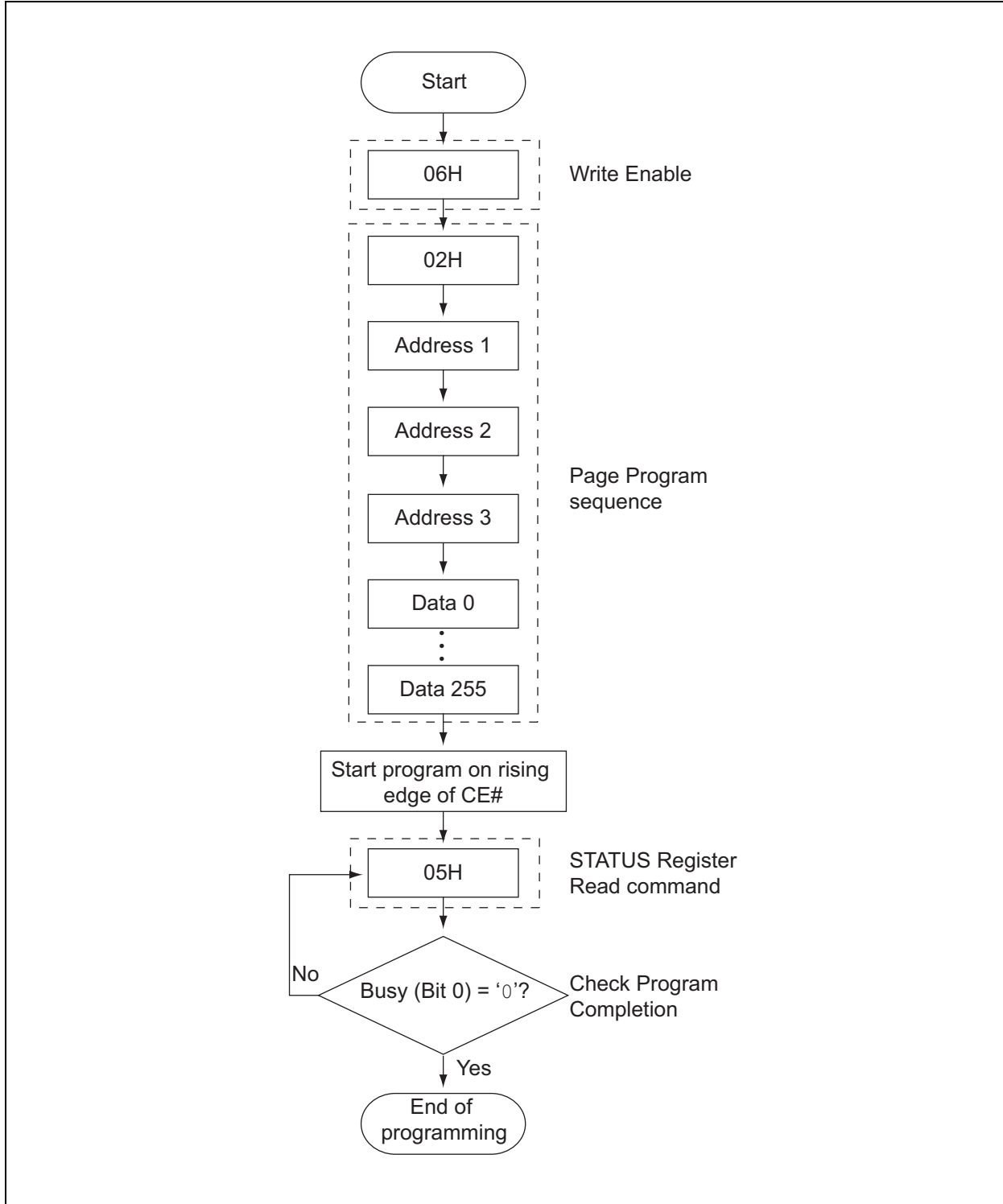
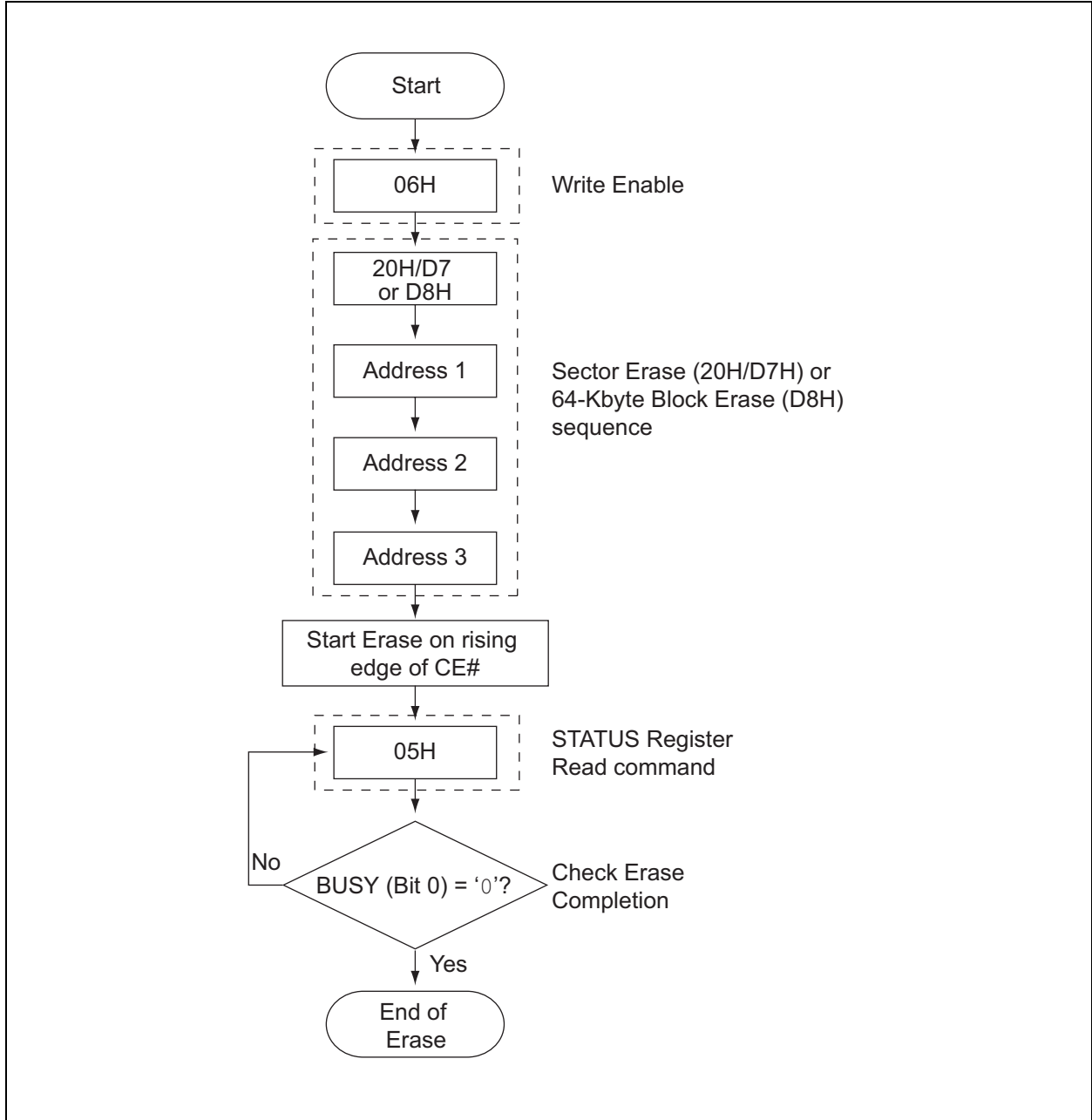


FIGURE 6-9: SECTOR ERASE OR 64-KBYTE BLOCK ERASE FLOW CHART



SST25PF040C

FIGURE 6-10: CHIP ERASE FLOW CHART

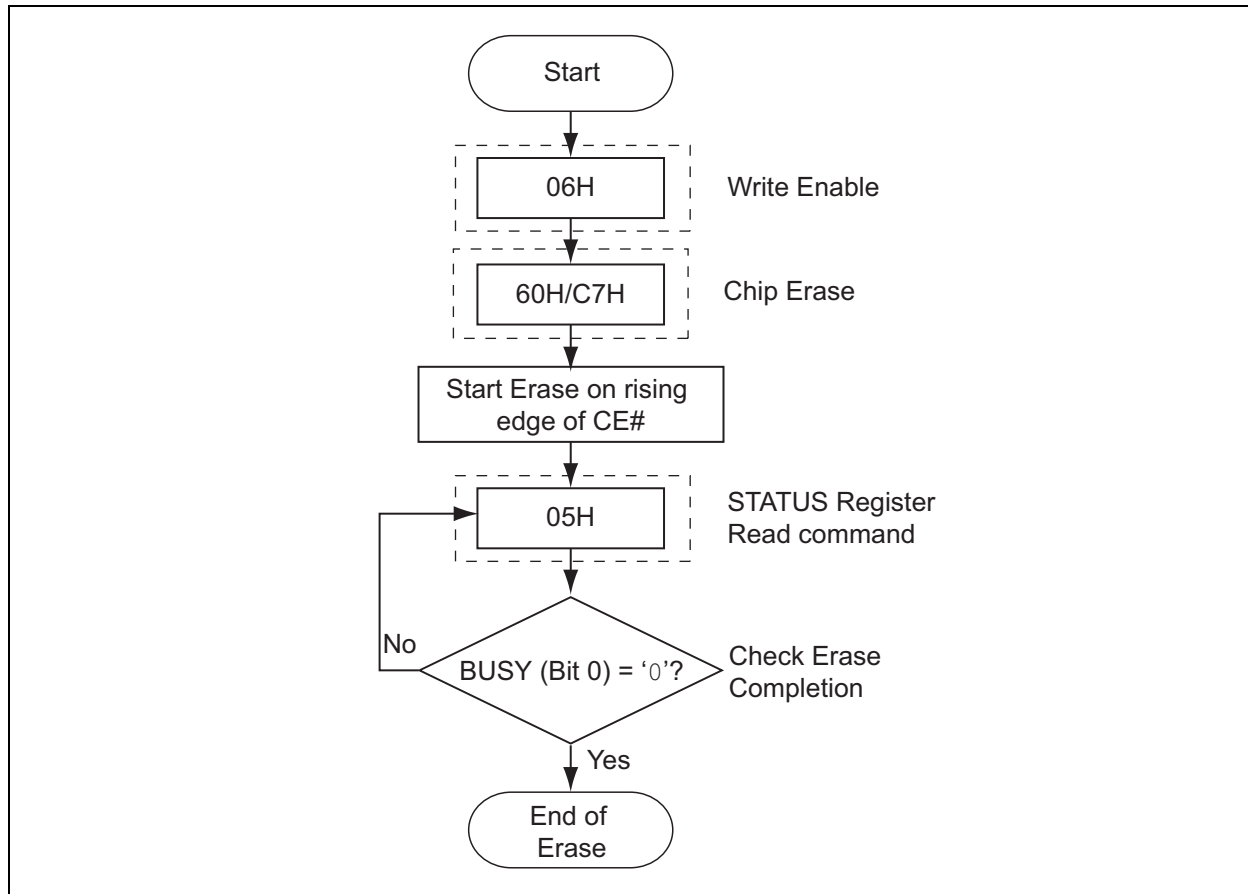
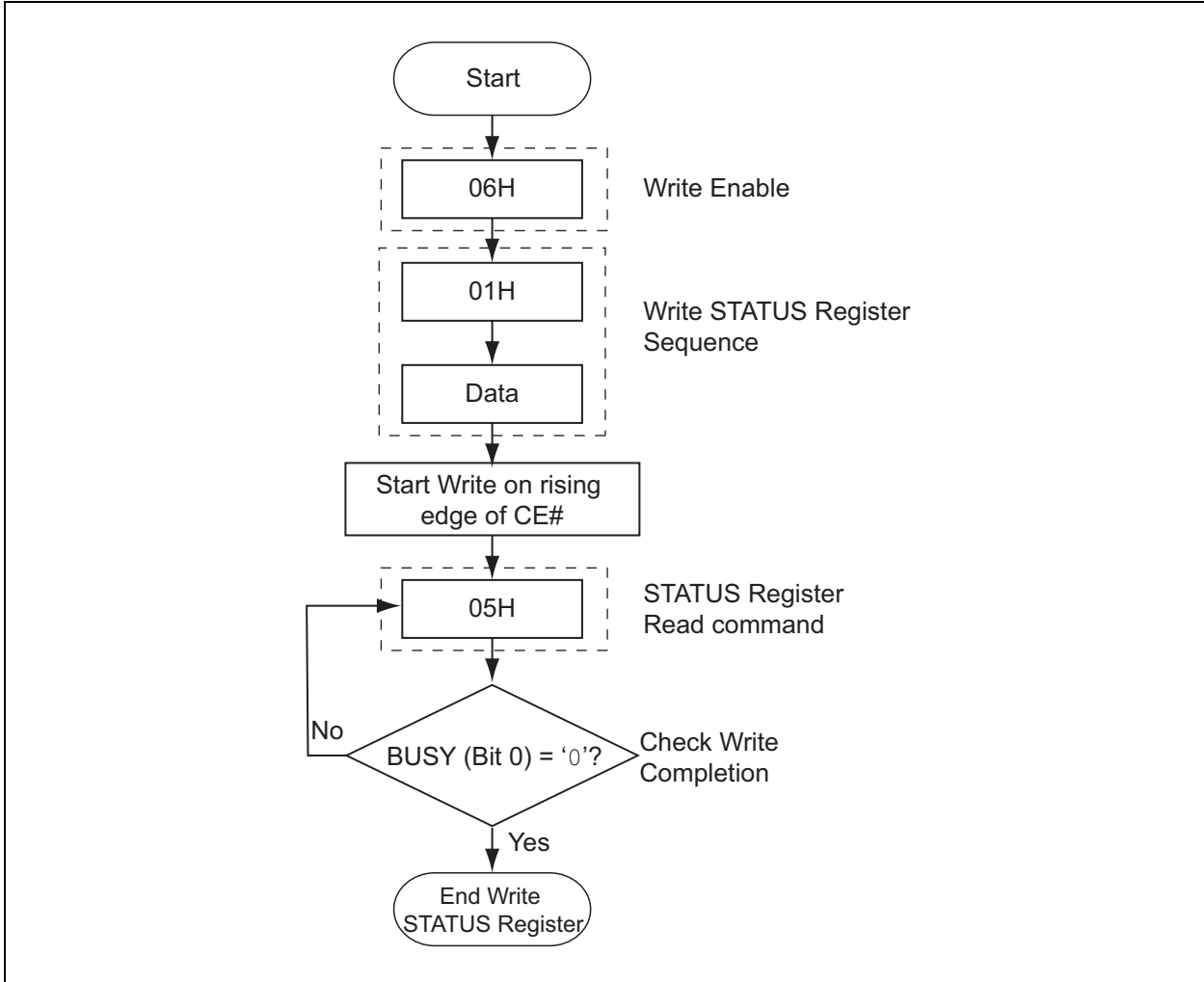


FIGURE 6-11: WRITE STATUS REGISTER (WRSR) FLOW CHART

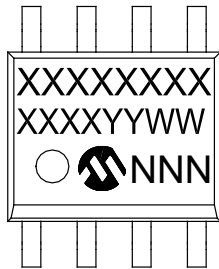


SST25PF040C

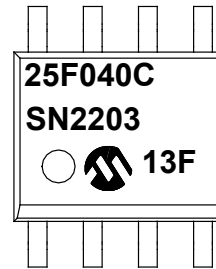
7.0 PACKAGING INFORMATION

7.1 Package Marking

8-Lead SOIC (3.90 mm)



Example



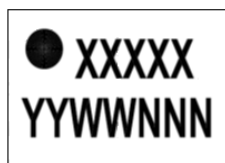
8-Lead WDFN (5x6 mm)



Example



8-Lead USON (2x3 mm)



Example



Part Number	1st Line Marking Codes		
	SOIC	WDFN	USON
SST25PF040C	25F040C	25F040C	5P040

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)

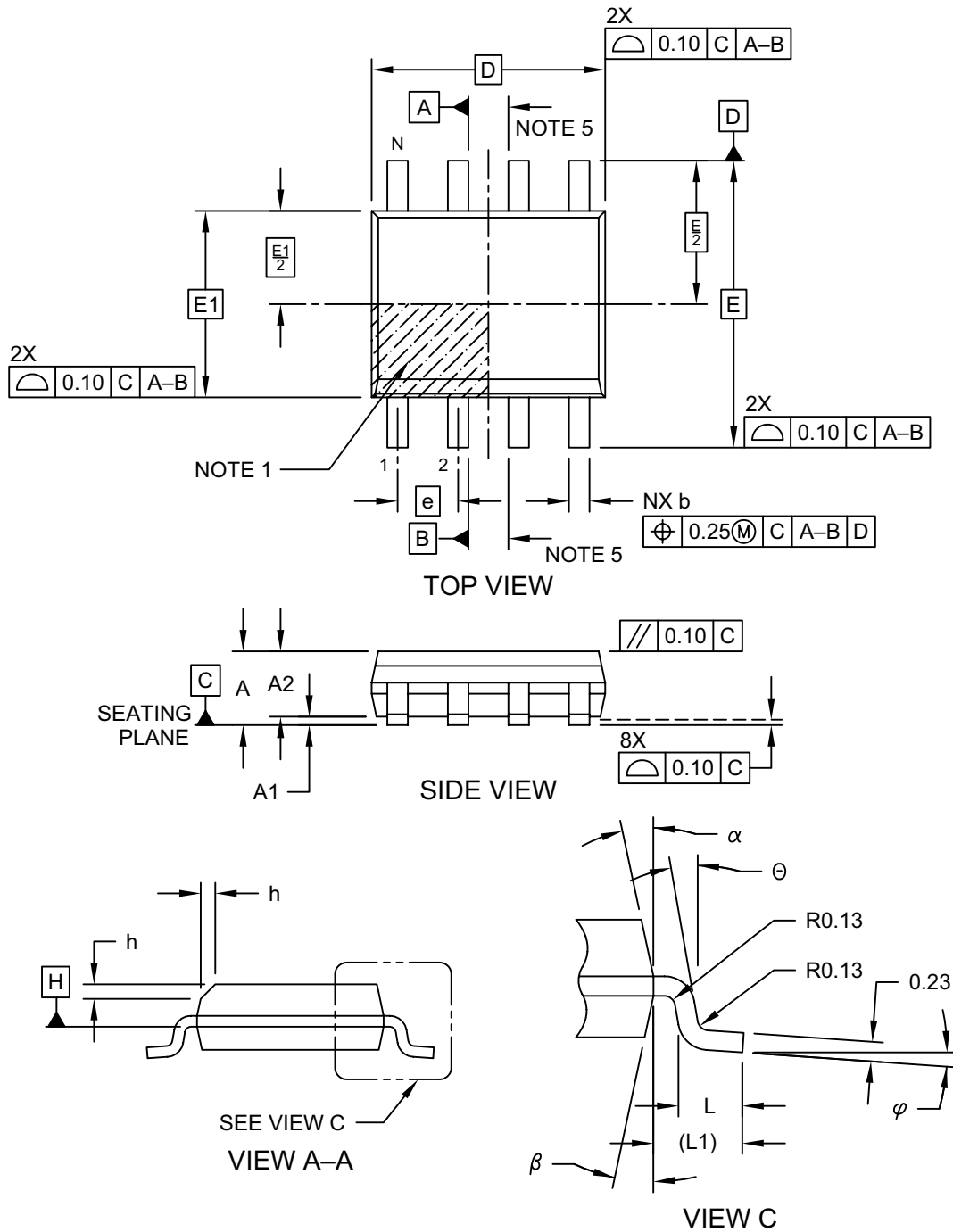
Note: For very small packages with no room for the Pb-free JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

SST25PF040C

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

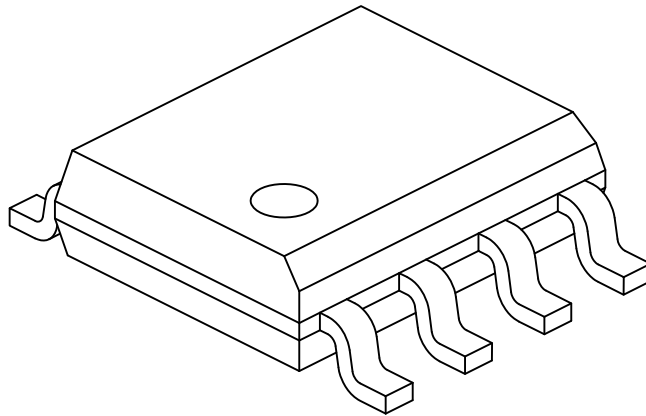


Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

SST25PF040C

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		1.27 BSC		
Overall Height	A	-	-	-	1.75
Molded Package Thickness	A2	1.25	-	-	-
Standoff §	A1	0.10	-	-	0.25
Overall Width	E		6.00 BSC		
Molded Package Width	E1		3.90 BSC		
Overall Length	D		4.90 BSC		
Chamfer (Optional)	h	0.25	-	-	0.50
Foot Length	L	0.40	-	-	1.27
Footprint	L1		1.04 REF		
Foot Angle	ϕ	0°	-	-	8°
Lead Thickness	c	0.17	-	-	0.25
Lead Width	b	0.31	-	-	0.51
Mold Draft Angle Top	α	5°	-	-	15°
Mold Draft Angle Bottom	β	5°	-	-	15°

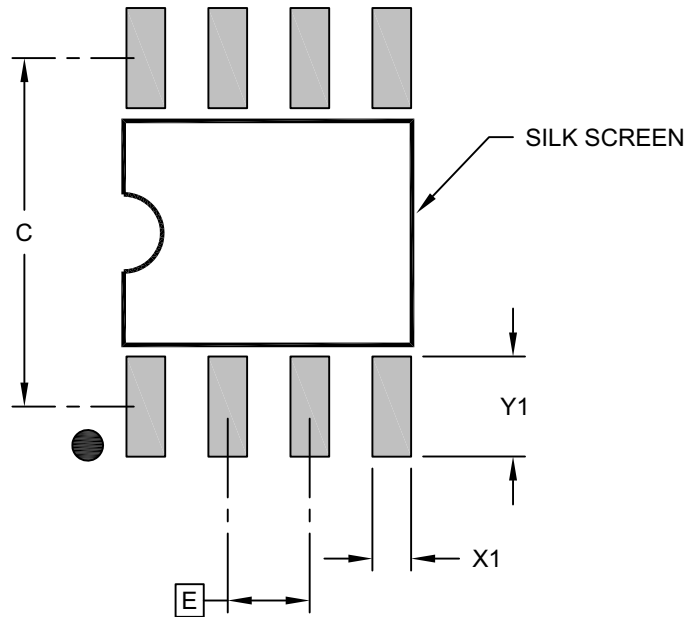
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

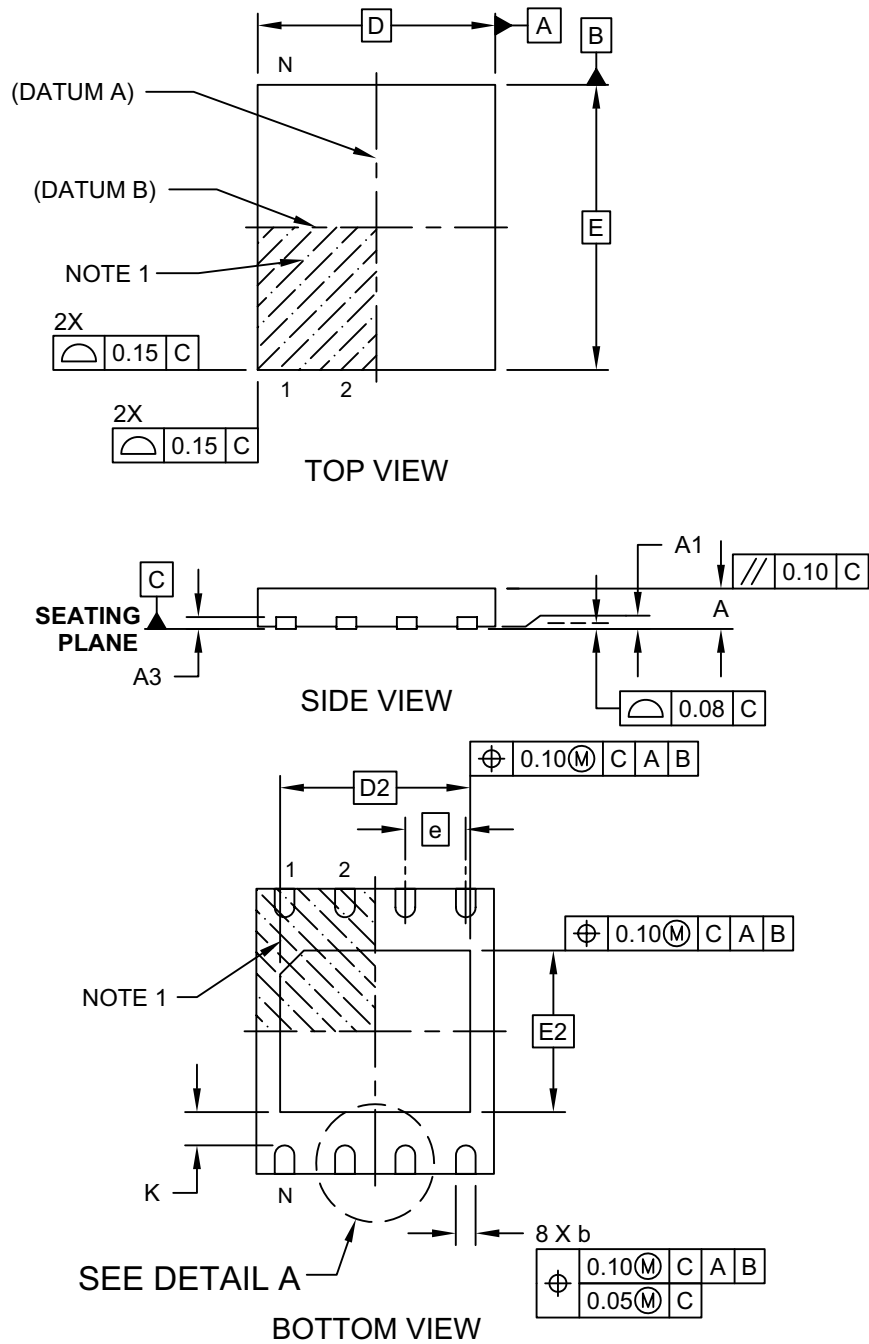
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev F

SST25PF040C

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

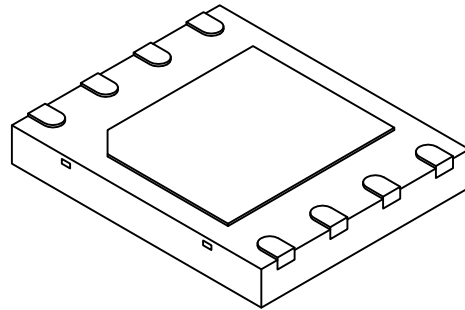
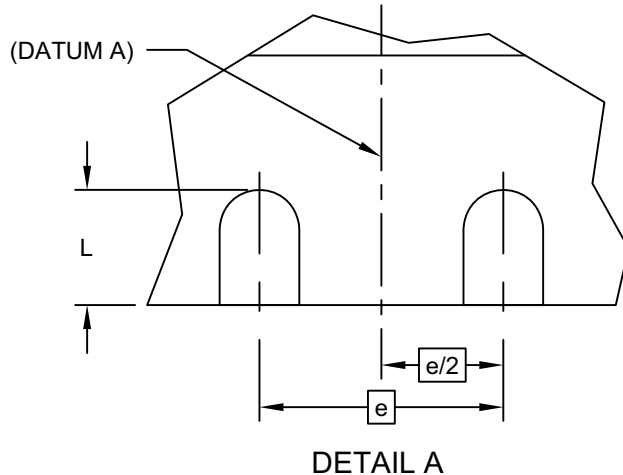


Microchip Technology Drawing C04-210B Sheet 1 of 2

SST25PF040C

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	D	5.00 BSC		
Exposed Pad Width	D2	4.00 BSC		
Overall Length	E	6.00 BSC		
Exposed Pad Length	E2	3.40 BSC		
Terminal Width	b	0.35	0.42	0.48
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

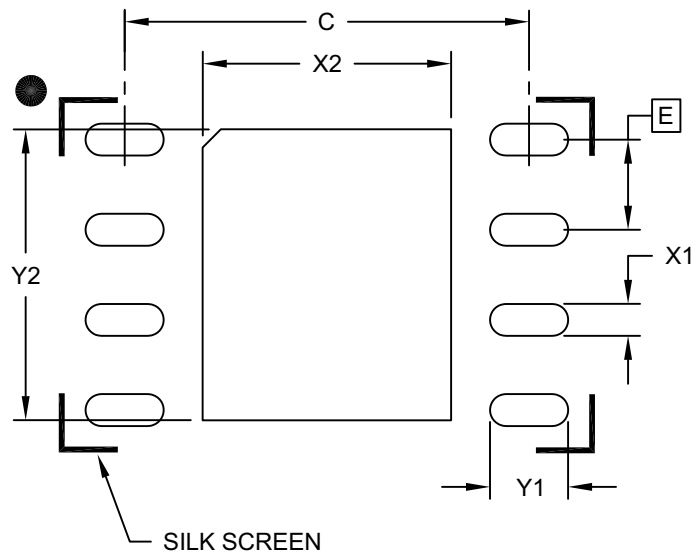
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-210B Sheet 2 of 2

SST25PF040C

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Optional Center Pad Width	X2			3.50
Optional Center Pad Length	Y2			4.10
Contact Pad Spacing	C		5.70	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.10

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

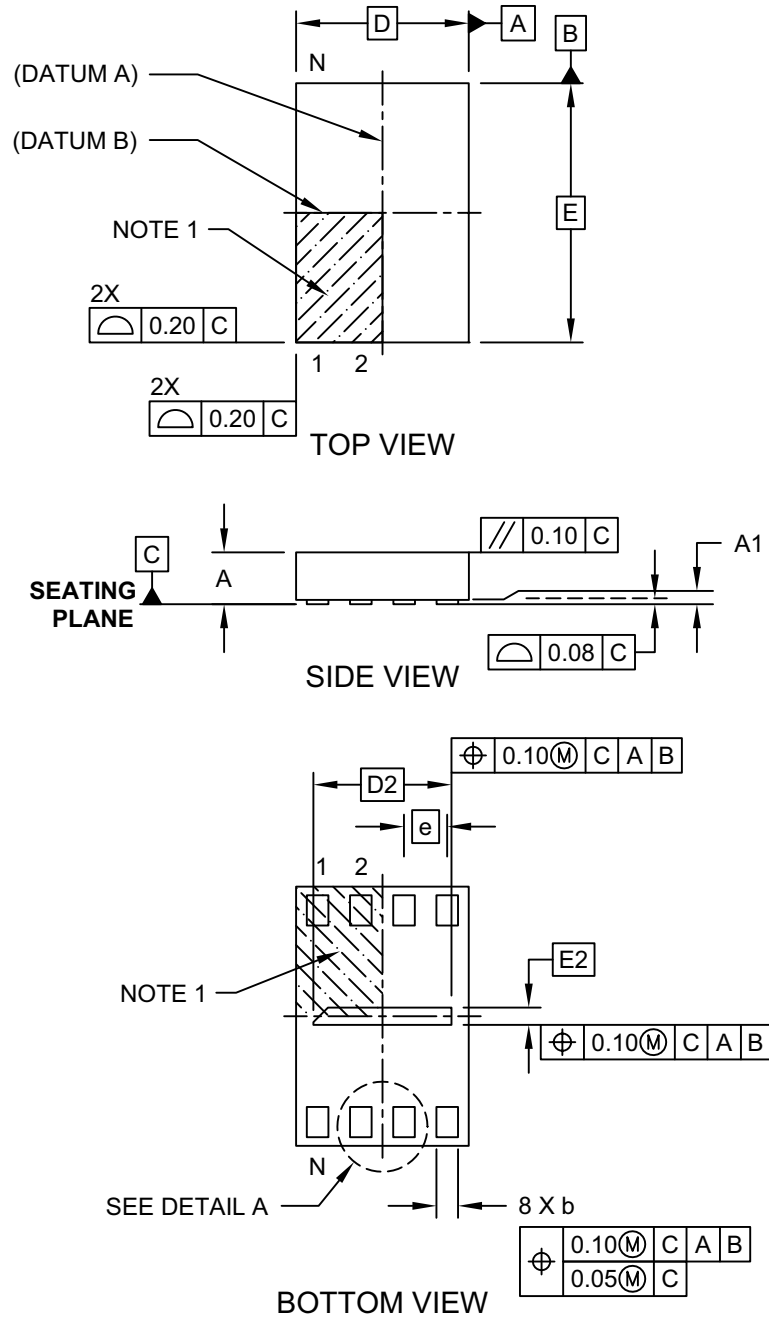
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2210A

SST25PF040C

8-Lead Plastic Ultra Thin Small Outline No Lead Package (PRX) - 2x3 mm Body [USON] [Also called UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

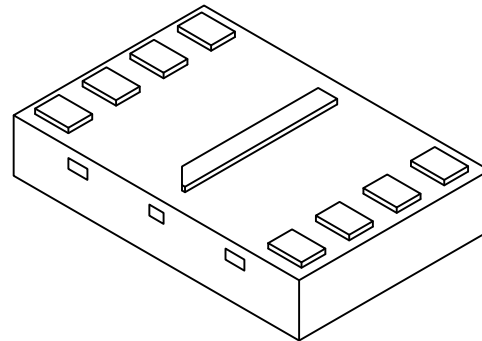
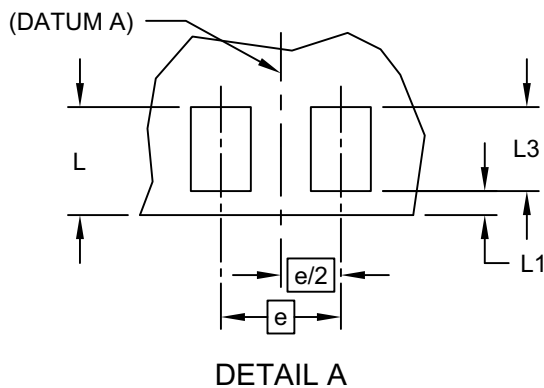


Microchip Technology Drawing C04-203C [PRX] Sheet 1 of 2

SST25PF040C

8-Lead Plastic Ultra Thin Small Outline No Lead Package (PRX) - 2x3 mm Body [USON] [Also called UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.45	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Overall Width	D	2.00 BSC		
Exposed Pad Width	D2	1.50	1.60	1.70
Overall Length	E	3.00 BSC		
Exposed Pad Length	E2	0.10	0.20	0.30
Terminal Width	b	0.20	0.25	0.30
Package Edge to Terminal Edge	L	0.40	0.45	0.50
Package Edge to Terminal Edge	L1	—	0.10	—
Terminal Length	L3	0.30	0.35	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

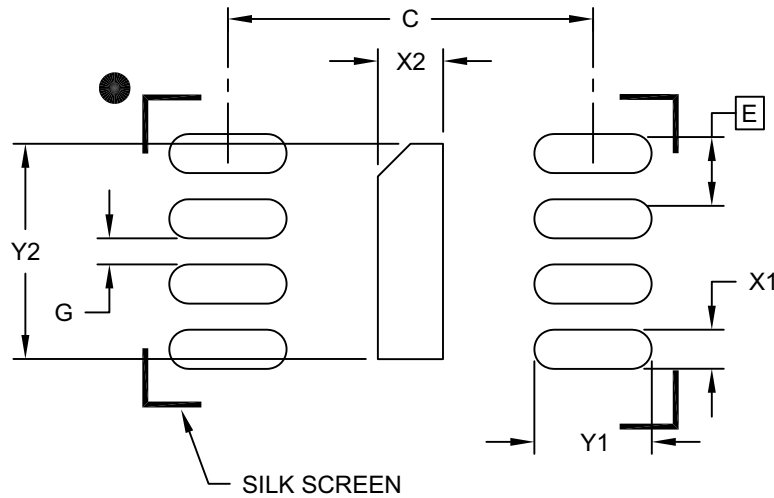
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-203C [PRX] Sheet 2 of 2

8-Lead Plastic Ultra Thin Small Outline No Lead Package (PRX) - 2x3 mm Body [USON] [Also called UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Terminal Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			0.30
Optional Center Pad Length	Y2			1.70
Terminal Pad Spacing	C		2.80	
Terminal Pad Width (X8)	X1			0.30
Terminal Pad Length (X8)	Y1			0.90
Minimum Between Terminal Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2203B [PRX]

SST25PF040C

APPENDIX A: REVISION HISTORY

Revision F (April 2022)

Replaced terminology “Master” and “Slave” with “Host” and “Client” respectively; Updated SOIC package drawings; Added Automotive Product Identification System.

Revision E (May 2019)

Added AECQ-100 Qualified information. Added Extended temperature rang.

Revision D (December 2018)

Corrected Maximum V_{IL} in [TABLE 6-5: “DC Operating Characteristics”](#).

Revision C (March 2017)

Added extended temperature range, added 2x3 USON package to the data sheet, updated [Figure 6-7](#), and updated valid ordering combinations in [Section 8.0 “Product Identification System”](#).

Revision B (November 2015)

Removed 2X3 USON package (NP) from data sheet

Revision A (October 2015)

Initial release of the document.

SST25PF040C

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SST25PF040C

PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X ⁽¹⁾	XXX	XX	XX
Device	Tape/Reel Indicator	Operating Frequency	Endurance/ Temperature	Package
Device: SST25PF040C = 4-Mbit, 2.3V-3.6V, Serial Flash Memory Tape and Reel Flag: T = Tape and Reel ⁽¹⁾ Operating Frequency: 40 = 40 MHz Temperature: I = -40°C to +85°C V = -40°C to +105°C E = -40°C to +125°C Package: SN = SOIC (3.90 mm Body), 8-lead MF = WDFN (5mm x 6mm Body), 8-contact NP = USON (2mm x 3mm Body), 8-contact	Valid Combinations: SST25PF040C-40I/SN SST25PF040CT-40I/SN SST25PF040C-40I/MF SST25PF040CT-40I/MF SST25PF040CT-40I/NP SST25PF040C-40V/SN SST25PF040CT-40V/SN SST25PF040C-40V/MF SST25PF040CT-40V/MF SST25PF040CT-40V/NP SST25PF040C-40E/SN SST25PF040CT-40E/SN SST25PF040C-40E/MF SST25PF040CT-40E/MF Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.			

SST25PF040C

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X⁽¹⁾	XXX	XX	XX	XXX^(2,3)	Valid Combinations:	
Device	Tape/Reel Indicator	Operating Frequency	Endurance/ Temperature	Package	Variant		
Device:	SST25PF040C	= 4-Mbit, 2.3-3.6V, Serial Flash Memory					SST25PF040C-40E/SN18GVAO SST25PF040C-40E/MF18GVAO SST25PF040C-40I/SN18GVAO SST25PF040C-40I/MF18GVAO SST25PF040C-40V/SN18GVAO SST25PF040C-40V/MF18GVAO SST25PF040CT-40V/SN18GVAO SST25PF040CT-40V/NP18GVAO SST25PF040CT-40V/MF18GVAO SST25PF040CT-40I/SN18GVAO SST25PF040CT-40I/NP18GVAO SST25PF040CT-40I/MF18GVAO SST25PF040CT-40E/SN18GVAO SST25PF040CT-40E/MF18GVAO
Tape and Reel Flag:	Blank T	= Standard packaging (tube or tray) = Tape and Reel ⁽¹⁾					Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. 2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications. 3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.
Operating Frequency:	40	= 40 MHz					
Temperature:	I V E	= -40°C to +85°C (AEC-Q100 Grade 3) = -40°C to +105°C (AEC-Q100 Grade 2) = -40°C to +125°C (AEC-Q100 Grade 1)					
Package:	SN MF NP	= SOIC (3.90 mm Body), 8-lead = WDFN (5mm x 6mm Body), 8-contact = USON (2mm x 3mm Body), 8-contact					
Variant^(2,3):	18GVAO 18GVXX	= Standard Automotive = Customer Specific Automotive					

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