

## Description

The AP64500 is a 5A, synchronous buck converter with a wide input voltage range of 3.8V to 40V. The device fully integrates a 45mΩ high-side power MOSFET and a 20mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The AP64500 device is easily used by minimizing the external component count due to its adoption of peak current mode control.

The AP64500 design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching. AP64500 also features Frequency Spread Spectrum (FSS) with a switching frequency jitter of  $\pm 6\%$ , which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

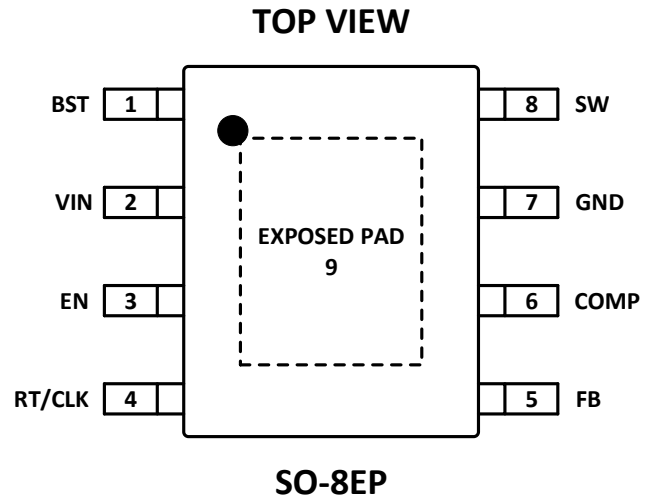
The device is available in an SO-8EP package.

## Features

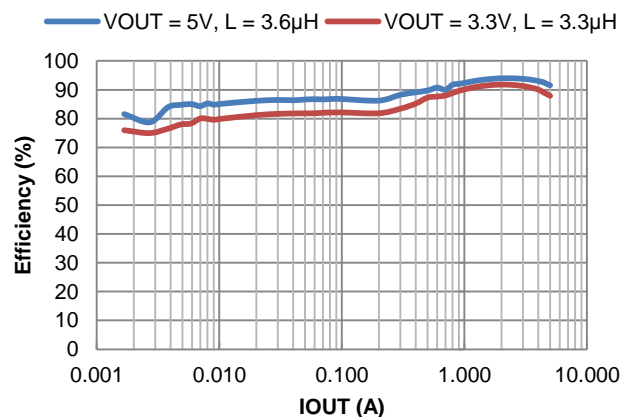
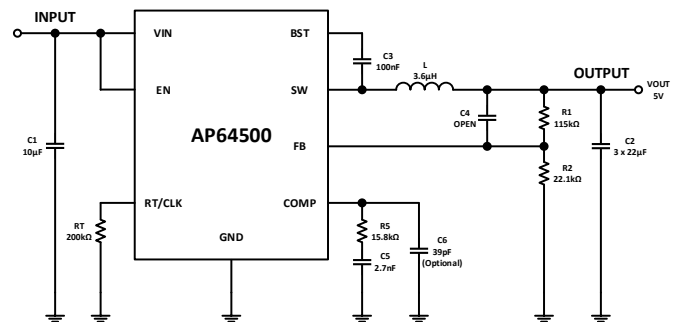
- VIN 3.8V to 40V
- 5A Continuous Output Current
- $0.8V \pm 1\%$  Reference Voltage
- 25μA Low Quiescent Current (Pulse Frequency Modulation)
- Programmable Switching Frequency: 100kHz to 2.2MHz
- External Clock Synchronization: 100kHz to 2.2MHz
- Up to 85% Efficiency at 5mA Light Load
- Proprietary Gate Driver Design for Best EMI Reduction
- Frequency Spread Spectrum (FSS) to Reduce EMI
- Low-Dropout (LDO) Mode
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Output Overvoltage Protection (OVP)
  - Cycle-by-Cycle Peak Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Assignments



## Typical Application Circuit



## Pin Descriptions

Pin Name	Pin Number	Function
BST	1	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel power MOSFET. A 100nF capacitor is recommended from BST to SW to power the high-side driver.
VIN	2	Power Input. VIN supplies the power to the IC as well as the step-down converter power MOSFETs. Drive VIN with a 3.8V to 40V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See <b>Input Capacitor</b> section for more details.
EN	3	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Connect to VIN or leave floating for automatic startup. The EN has a precision threshold of 1.18V for programming the UVLO. See <b>Enable</b> section for more details.
RT/CLK	4	Resistor Timing and External Clock. This pin can be used to control the switching frequency by setting the internal oscillator frequency or by synchronizing to an external clock. Connect a resistor from RT/CLK to GND to set the internal oscillator frequency. An external clock can be input directly to the RT/CLK pin and the internal oscillator synchronizes to the external clock frequency using a PLL. If the external clock edges stop, the operating mode automatically returns to resistor frequency programming. See <b>Programming Switching Frequency</b> section for more details.
FB	5	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See <b>Setting the Output Voltage</b> section for more details.
COMP	6	Compensation. Connect an external RC network to the COMP pin to adjust the loop response. See <b>External Loop Compensation Design</b> section for more details.
GND	7	Power Ground.
SW	8	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
EXPOSED PAD	9	Heat dissipation path of the die. The exposed thermal pad must be electrically connected to GND and must be connected to the ground plane of the PCB for proper operation and optimized thermal performance.

## Absolute Maximum Ratings (Note 4) (At $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +42.0 (DC)	V
		-0.3 to +45.0 (400ms)	
V <sub>BST</sub>	Bootstrap Pin Voltage	$V_{SW} - 0.3$ to $V_{SW} + 6.0$	V
V <sub>EN</sub>	Enable/UVLO Pin Voltage	-0.3 to +42.0	V
V <sub>RT/CLK</sub>	RT/CLK Pin Voltage	-0.3 to +6.0	V
V <sub>FB</sub>	Feedback Pin Voltage	-0.3 to +6.0	V
V <sub>COMP</sub>	Compensation Pin Voltage	-0.3 to +6.0	V
V <sub>SW</sub>	Switch Pin Voltage	-0.3 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
T <sub>ST</sub>	Storage Temperature	-65 to +150	°C
T <sub>J</sub>	Junction Temperature	+160	°C
T <sub>L</sub>	Lead Temperature	+260	°C
<b>ESD Susceptibility (Note 5)</b>			
HBM	Human Body Model	2000	V
CDM	Charged Device Model	500	V

- Notes:
- Stresses greater than the **Absolute Maximum Ratings** specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
  - Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

## Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
		SO-8EP		
$\theta_{JA}$	Junction to Ambient	SO-8EP	45	$^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Junction to Case	SO-8EP	5	$^{\circ}\text{C}/\text{W}$

Note: 6. Test condition for SO-8EP: Device mounted on FR-4 substrate, four-layer PC board, 2oz copper, with minimum recommended pad layout.

## Recommended Operating Conditions (Note 7) (At $T_A = +25^{\circ}\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	3.8	40	V
VOUT	Output Voltage	0.8	VIN	V
$T_A$	Operating Ambient Temperature Range	-40	+85	$^{\circ}\text{C}$
$T_J$	Operating Junction Temperature Range	-40	+125	$^{\circ}\text{C}$

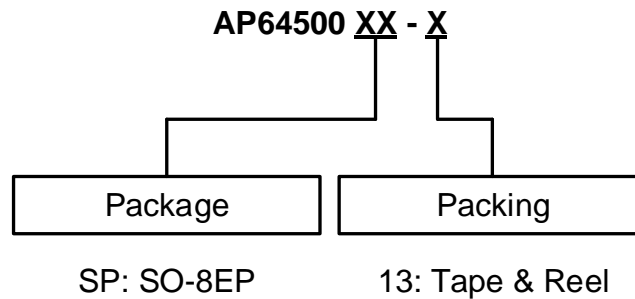
Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

## Electrical Characteristics (At $T_A = +25^{\circ}\text{C}$ , VIN = 12V, unless otherwise specified. Min/Max limits apply across the recommended ambient temperature range, $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , and input voltage range, 3.8V to 40V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{SHDN}$	Shutdown Supply Current	$V_{EN} = 0\text{V}$	—	1	3	$\mu\text{A}$
$I_Q$	Quiescent Supply Current	$V_{EN} = \text{Floating}, V_{FB} = 1.0\text{V}$	—	25	—	$\mu\text{A}$
UVLO	VIN Undervoltage Rising Threshold	—	—	3.5	3.7	V
	VIN Undervoltage Hysteresis	—	—	400	—	mV
$R_{DS(ON)1}$	High-Side Power MOSFET On-Resistance (Note 8)	—	—	45	—	$\text{m}\Omega$
$R_{DS(ON)2}$	Low-Side Power MOSFET On-Resistance (Note 8)	—	—	20	—	$\text{m}\Omega$
$I_{PEAK\_LIMIT}$	HS Peak Current Limit (Note 8)	—	6.8	8	9.2	A
$I_{VALLEY\_LIMIT}$	LS Valley Current Limit (Note 8)	—	—	9	—	A
$I_{PFMPK}$	PFM Peak Current Limit	—	—	950	—	mA
$I_{ZC}$	Zero Cross Current Threshold	—	—	0	—	mA
$f_{RANGE\_RT}$	Frequency Range Using RT	—	100	—	2200	kHz
$f_{SW}$	Oscillator Frequency	$RT = 200\text{k}\Omega (\pm 1\%)$	450	500	550	kHz
$f_{RANGE\_CLK}$	Frequency Range Using External CLK	—	100	—	2200	kHz
$t_{ON\_MIN}$	Minimum On-Time	—	—	100	—	ns
$V_{FB}$	Feedback Voltage	CCM	792	800	808	mV
$V_{EN\_H}$	EN Logic High Threshold	—	—	1.18	1.25	V
$V_{EN\_L}$	EN Logic Low Threshold	—	1.03	1.09	—	V
$I_{EN}$	EN Input Current	$V_{EN} = 1.5\text{V}$	—	5.5	—	$\mu\text{A}$
		$V_{EN} = 1\text{V}$	1	1.5	2	$\mu\text{A}$
$t_{SS}$	Soft-Start Time	—	—	4	—	ms
$T_{SD}$	Thermal Shutdown (Note 8)	—	—	160	—	$^{\circ}\text{C}$
$T_{Hys}$	Thermal Shutdown Hysteresis (Note 8)	—	—	25	—	$^{\circ}\text{C}$

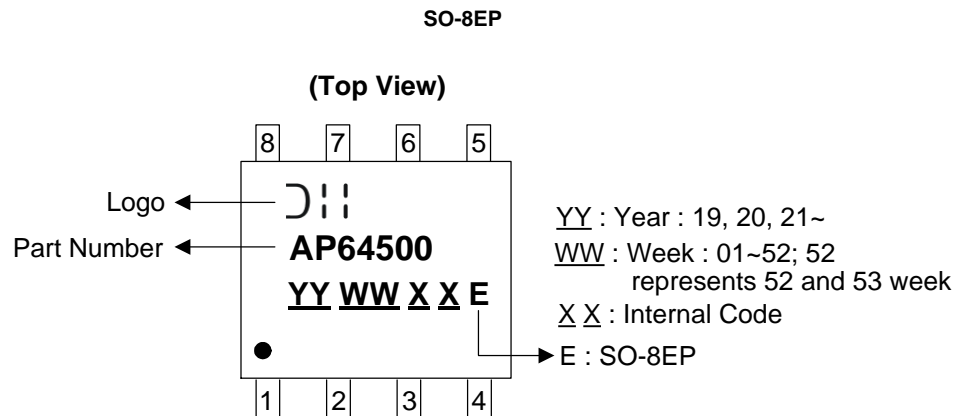
Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

## Ordering Information



Orderable Device	Package Code	Tape and Reel	
		Quantity	Part Number Suffix
AP64500SP-13	SP	4000	-13

## Marking Information



## Device Comparison Table

Part Name	VIN (V)	VOUT (V)	Output Current (A)	HS / LS R <sub>DS(ON)</sub> (mΩ)	Switching Frequency (kHz)	I <sub>q</sub> (μA)	Key Features	Ambient Temperature (°C)	Package
AP64350	3.8 to 40	0.8 to VIN	3.5	75 / 45	100 to 2200	22	Prog. Fsw, Ext. Sync, Ext. Comp	-40 to +85	SO-8EP
AP64351	3.8 to 40	0.8 to VIN	3.5	75 / 45	570	22	Prog. SS, Ext. Comp	-40 to +85	SO-8EP
AP64352	3.8 to 40	0.8 to VIN	3.5	75 / 45	100 to 2200	22	Prog. Fsw, Ext. Sync, Ext. SS	-40 to +85	SO-8EP
AP64500	3.8 to 40	0.8 to VIN	5.0	45 / 20	100 to 2200	25	Prog. Fsw, Ext. Sync, Ext. Comp	-40 to +85	SO-8EP
AP64501	3.8 to 40	0.8 to VIN	5.0	45 / 20	570	25	Prog. SS, Ext. Comp	-40 to +85	SO-8EP

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