

# CCB032M12FM3

## 1200 V, 32 mΩ All-Silicon Carbide Six-Pack Module

|              |               |
|--------------|---------------|
| $V_{DS}$     | <b>1200 V</b> |
| $R_{DS(on)}$ | <b>32 mΩ</b>  |

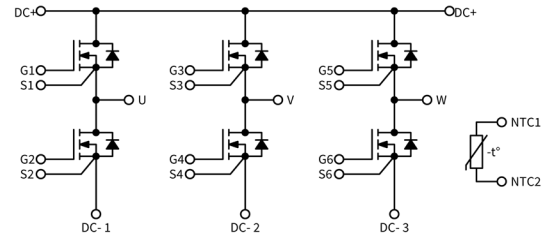
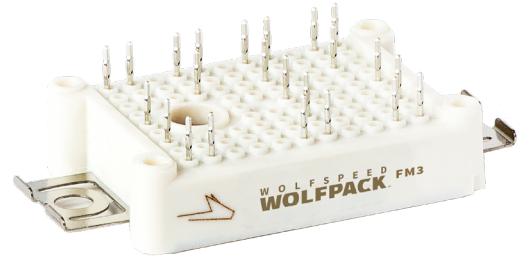
### Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation

### Applications

- EV Chargers
- Solar
- High-Efficiency Converters / Inverters
- Motor & Traction Drives
- Smart-Grid / Grid-Tied Distributed Generation

### Package



### System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

### Maximum Parameters (Verified by Design)

| Symbol            | Parameter   | Min. | Typ. | Max. | Unit             | Test Conditions   | Note              |
|-------------------|---|------|------|------|------------------|---|-------------------|
| $V_{DS\ max}$     | Drain-Source Voltage  |      |      | 1200 | V                |   |                   |
| $V_{GS\ max}$     | Gate-Source Voltage, Maximum Value                                | -8   |      | +19  |                  | Transient, <100 ns  | Fig. 33           |
| $V_{GS\ op}$      | Gate-Source Voltage, Recommended Op. Value                        | -4   |      | +15  |                  | Static  |                   |
| $I_D$             | DC Continuous Drain Current ( $T_{VJ} \leq 150\ ^\circ\text{C}$ ) |      | 40   |      | A                | $V_{GS} = 15\ \text{V}, T_H = 50\ ^\circ\text{C}, T_{VJ} \leq 150\ ^\circ\text{C}$    | Fig. 20<br>Note 1 |
|                   | DC Continuous Drain Current ( $T_{VJ} \leq 175\ ^\circ\text{C}$ ) |      | 42   |      |                  | $V_{GS} = 15\ \text{V}, T_H = 50\ ^\circ\text{C}, T_{VJ} \leq 175\ ^\circ\text{C}$    |                   |
| $I_{SD\ BD}$      | DC Source-Drain Current (Body Diode)                              |      | 24   |      |                  | $V_{GS} = -4\ \text{V}, T_H = 50\ ^\circ\text{C}, T_{VJ} \leq 175\ ^\circ\text{C}$    |                   |
| $I_{D\ (pulsed)}$ | Maximum Pulsed Drain Current                                      |      |      | 84   |                  | $t_{Pmax}$ limited by $T_{Jmax}$<br>$V_{GS} = 15\ \text{V}, T_H = 50\ ^\circ\text{C}$ |                   |
| $T_{VJ\ op}$      | Maximum Virtual Junction Temperature under Switching Conditions   | -40  |      | 150  | $^\circ\text{C}$ | Operation   |                   |
|                   |   | -40  |      | 175  | $^\circ\text{C}$ | Intermittent with Reduced Life  |                   |

Note 1. DC continuous drain current rating,  $I_D$ , limited to 30 A by the press-fit pins.

**MOSFET Characteristics (Per Position)** ( $T_{vj} = 25^\circ\text{C}$  unless otherwise specified)

| Symbol        | Parameter   | Min. | Typ.                    | Max. | Unit                      | Test Conditions   | Note               |
|---------------|---|------|-------------------------|------|---------------------------|---|--------------------|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage  | 1200 |                         |      | V                         | $V_{GS} = 0\text{ V}, T_{vj} = -40^\circ\text{C}$   |                    |
| $V_{GS(th)}$  | Gate Threshold Voltage  | 1.8  | 2.5                     | 3.6  |                           | $V_{DS} = V_{GS}, I_D = 11.5\text{ mA}$   |                    |
| $I_{DSS}$     | Zero Gate Voltage Drain Current   |      | 1                       | 19   | $\mu\text{A}$             | $V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$   |                    |
| $I_{GSS}$     | Gate-Source Leakage Current   |      | 10                      | 250  | nA                        | $V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$   |                    |
| $R_{DS(on)}$  | Drain-Source On-State Resistance (Devices Only)   |      | 32.0                    | 42.6 | m $\Omega$                | $V_{GS} = 15\text{ V}, I_D = 30\text{ A}$   | Fig. 2<br>Fig. 3   |
|               |   |      | 51.2                    |      |                           | $V_{GS} = 15\text{ V}, I_D = 30\text{ A}, T_{vj} = 150^\circ\text{C}$   |                    |
|               |   |      | 57.6                    |      |                           | $V_{GS} = 15\text{ V}, I_D = 30\text{ A}, T_{vj} = 175^\circ\text{C}$   |                    |
| $g_{fs}$      | Transconductance  |      | 21.3                    |      | S                         | $V_{DS} = 20\text{ V}, I_{DS} = 30\text{ A}$  | Fig. 4             |
|               |   |      | 20.1                    |      |                           | $V_{DS} = 20\text{ V}, I_{DS} = 30\text{ A}, T_{vj} = 150^\circ\text{C}$  |                    |
| $E_{On}$      | Turn-On Switching Energy, $T_J = 25^\circ\text{C}$<br>$T_{vj} = 125^\circ\text{C}$<br>$T_{vj} = 150^\circ\text{C}$  |      | 0.41<br>0.80<br>0.95    |      | mJ                        | $V_{DS} = 600\text{ V},$<br>$I_D = 30\text{ A},$<br>$V_{GS} = -4\text{ V}/15\text{ V},$<br>$R_{G(OFF)} = 1.0\ \Omega, R_{G(ON)} = 1.0\ \Omega$<br>$L = 45.1\ \mu\text{H}$ | Fig. 11<br>Fig. 13 |
| $E_{Off}$     | Turn-Off Switching Energy, $T_J = 25^\circ\text{C}$<br>$T_{vj} = 125^\circ\text{C}$<br>$T_{vj} = 150^\circ\text{C}$ |      | 0.005<br>0.006<br>0.007 |      |                           |   |                    |
| $R_{G(int)}$  | Internal Gate Resistance  |      | 1.7                     |      | $\Omega$                  | $T_{vj} = 25^\circ\text{C}, f = 100\text{ kHz}, V_{AC} = 25\text{ mV}$  |                    |
| $C_{iss}$     | Input Capacitance   |      | 3.4                     |      | nF                        | $V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V},$<br>$V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$  | Fig. 9             |
| $C_{oss}$     | Output Capacitance  |      | 144                     |      |                           |   |                    |
| $C_{rss}$     | Reverse Transfer Capacitance  |      | 14                      |      |                           |   |                    |
| $Q_{GS}$      | Gate to Source Charge   |      | 40                      |      | nC                        | $V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$<br>$I_D = 40\text{ A}$<br>Per IEC60747-8-4 pg 21  |                    |
| $Q_{GD}$      | Gate to Drain Charge  |      | 34                      |      |                           |   |                    |
| $Q_G$         | Total Gate Charge   |      | 118                     |      |                           |   |                    |
| $R_{thJH}$    | FET Thermal Resistance, Junction to Heatsink  |      | 1.24                    |      | $^\circ\text{C}/\text{W}$ |   | Fig. 17            |



### Diode Characteristics (Per Position) ( $T_{vj} = 25^\circ\text{C}$ unless otherwise specified)

| Symbol    | Parameter  | Min. | Typ. | Max. | Unit          | Test Conditions   | Note    |
|-----------|--|------|------|------|---------------|---|---------|
| $V_{SD}$  | Body Diode Forward Voltage   |      | 4.6  |      | V             | $V_{GS} = -4\text{ V}, I_{SD} = 30\text{ A}$  | Fig. 7  |
|           |  |      | 4.4  |      |               | $V_{GS} = -4\text{ V}, I_{SD} = 30\text{ A}, T_{vj} = 150^\circ\text{C}$  |         |
| $t_{rr}$  | Reverse Recovery Time  |      | 17   |      | ns            | $V_{GS} = -4\text{ V}, I_{SD} = 30\text{ A}, V_R = 600\text{ V}$<br>$di/dt = 15\text{ A/ns}, R_{G(ON)} = 1.0\ \Omega,$<br>$T_J = 150^\circ\text{C}$ | Fig. 32 |
| $Q_{RR}$  | Reverse Recovery Charge  |      | 1.2  |      | $\mu\text{C}$ |   |         |
| $I_{RRM}$ | Peak Reverse Recovery Current  |      | 115  |      | A             |   |         |
| $E_{RR}$  | Reverse Recovery Energy $T_J = 25^\circ\text{C}$<br>$T_J = 125^\circ\text{C}$<br>$T_J = 150^\circ\text{C}$ |      | 0.13 |      | mJ            | $V_{DS} = 600\text{ V}, I_D = 30\text{ A},$<br>$V_{GS} = -4\text{ V}/15\text{ V}, R_{G(ON)} = 1.0\ \Omega,$<br>$L = 45.1\ \mu\text{H}$              | Fig. 14 |
|           |  |      | 0.26 |      |               |   |         |
|           |  |      | 0.31 |      |               |   |         |

### Module Physical Characteristics

| Symbol      | Parameter                                  | Min. | Typ. | Max. | Unit             | Test Conditions   |
|-------------|--|------|------|------|------------------|---|
| $R_{HS}$    | Package Resistance, M1, M3, M5 (High-Side) |      | 5.3  |      | m $\Omega$       | $T_c = 25^\circ\text{C}, I_D = 30\text{ A}, \text{Note 2}$  |
|             |  |      | 5.9  |      |                  | $T_c = 125^\circ\text{C}, I_D = 30\text{ A}, \text{Note 2}$ |
| $R_{LS}$    | Package Resistance, M2, M4, M6 (Low-Side)  |      | 7.4  |      |                  | $T_c = 25^\circ\text{C}, I_D = 30\text{ A}, \text{Note 2}$  |
|             |  |      | 8.1  |      |                  | $T_c = 125^\circ\text{C}, I_D = 30\text{ A}, \text{Note 2}$ |
| $L_{Stray}$ | Stray Inductance                           |      | 17.4 |      | nH               | Between Terminals DC+ and DC-                               |
| $T_c$       | Case Temperature                           | -40  |      | 125  | $^\circ\text{C}$ |   |
| W           | Weight                                     |      | 21   |      | g                |   |
| $M_s$       | Mounting Torque                            |      | 2.0  | 2.3  | N-m              | M4 bolts  |
| $V_{isol}$  | Case Isolation Voltage                     |      | 3    |      | kV               | AC, 50 Hz, 1 min  |
| CTI         | Comparative Tracking Index                 | 200  |      |      |                  |   |
|             | Clearance Distance                         |      | 5.0  |      | mm               | Terminal to Terminal  |
|             |  |      | 10.0 |      |                  | Terminal to Heatsink  |
|             | Creepage Distance                          |      | 6.3  |      |                  | Terminal to Terminal  |
|             |  |      | 11.5 |      |                  | Terminal to Heatsink  |

Note 2. Total Effective Resistance (Per Switch Position) = MOSFET  $R_{DS(on)}$  + Switch Position Package Resistance.

### NTC Thermistor Characterization

| Symbol           | Parameter                                  | Min. | Typ. | Max. | Unit       | Test Conditions              | Note    |
|------------------|--|------|------|------|------------|------------------------------|---------|
| $R_{NTC}$        | Rated Resistance                           |      | 5.0  |      | k $\Omega$ | $T_{NTC} = 25^\circ\text{C}$ | Fig. 23 |
| $\Delta R/R$     | Resistance Tolerance at $25^\circ\text{C}$ | -5   |      | 5    | %          |                              |         |
| $\beta_{25/50}$  | Beta Value ( $T_2 = 50^\circ\text{C}$ )    |      | 3380 |      | K          |                              |         |
| $\beta_{25/80}$  | Beta Value ( $T_2 = 80^\circ\text{C}$ )    |      | 3468 |      | K          |                              |         |
| $\beta_{25/100}$ | Beta Value ( $T_2 = 100^\circ\text{C}$ )   |      | 3523 |      | K          |                              |         |
| $P_{Max}$        | Power Dissipation                          |      |      | 10   | mW         | $T_{NTC} = 25^\circ\text{C}$ |         |



## Typical Performance

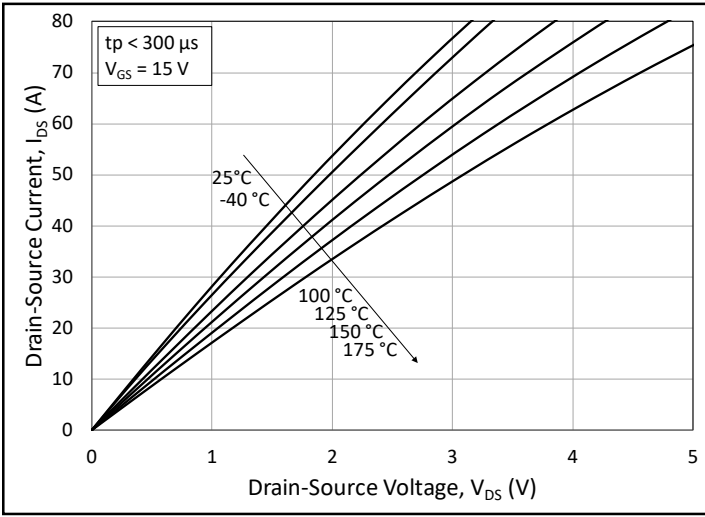


Figure 1. Output Characteristics for Various Junction Temperatures

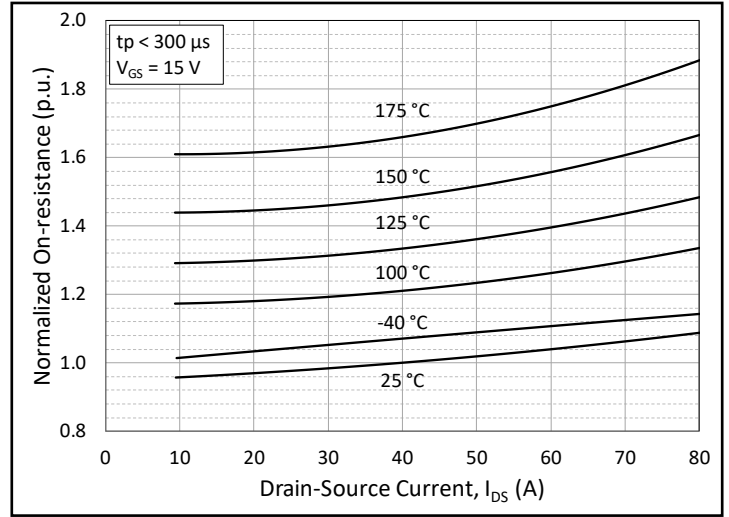


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

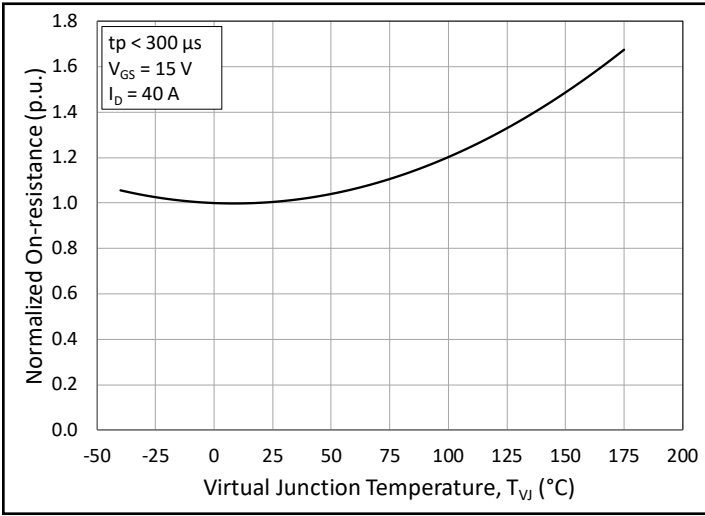


Figure 3. Normalized On-State Resistance vs. Junction Temperature

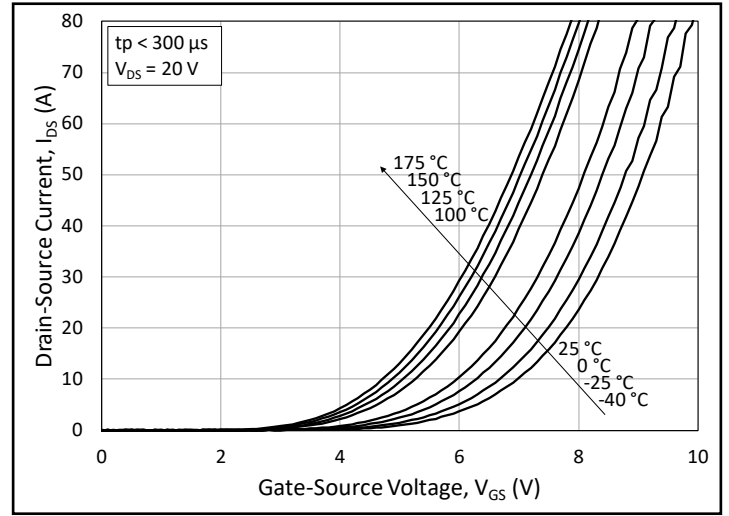


Figure 4. Transfer Characteristic for Various Junction Temperatures

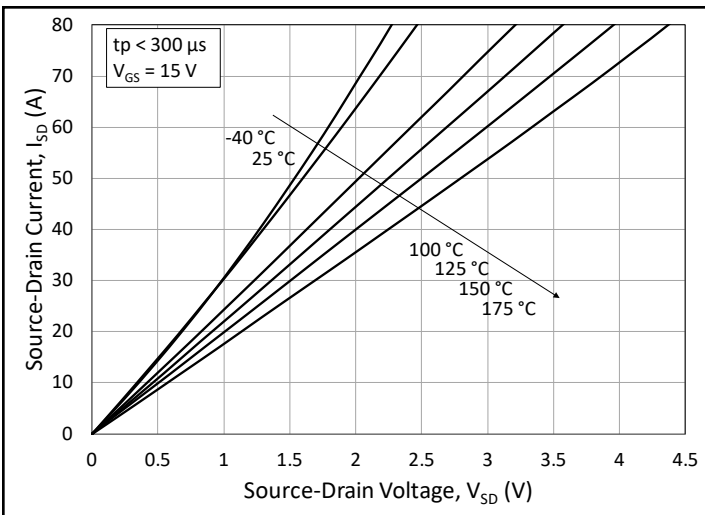


Figure 5. 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = 15\text{ V}$

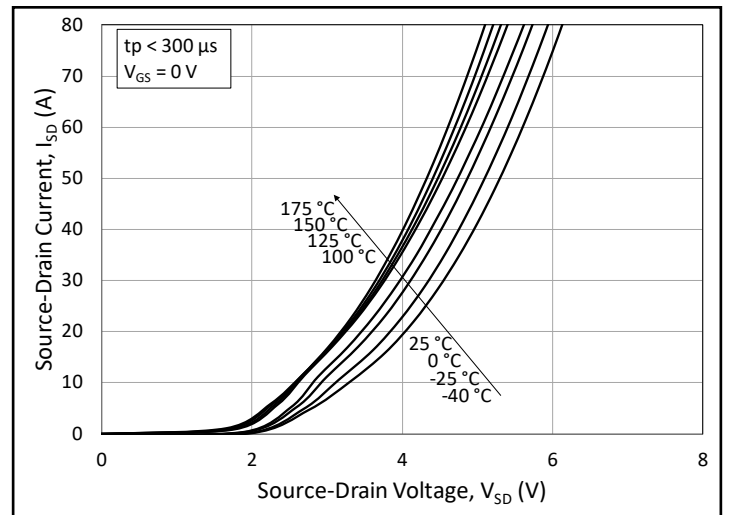


Figure 6. 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = 0\text{ V}$  (Body Diode)

**Typical Performance**

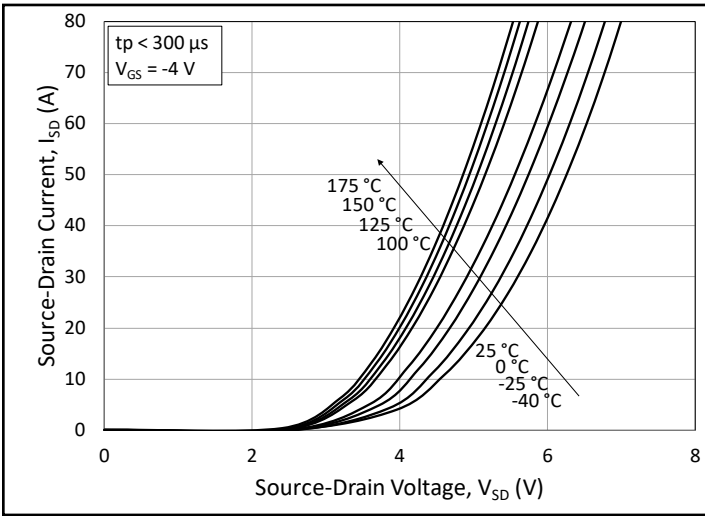


Figure 7. 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = -4\text{ V}$  (Body Diode)

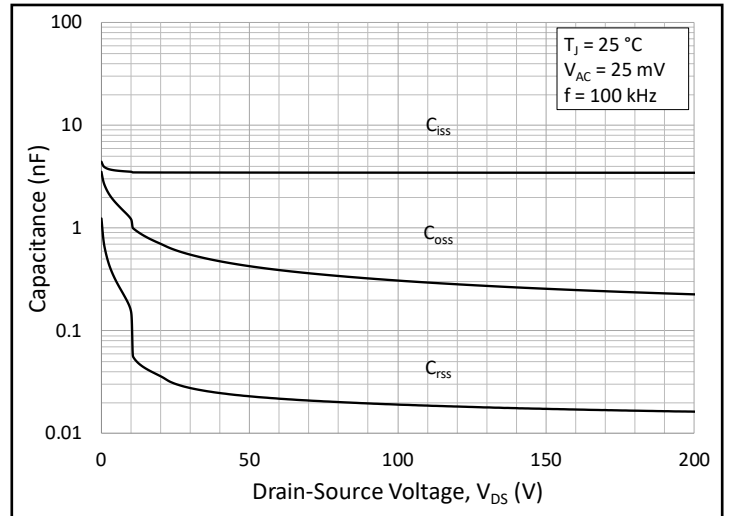


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

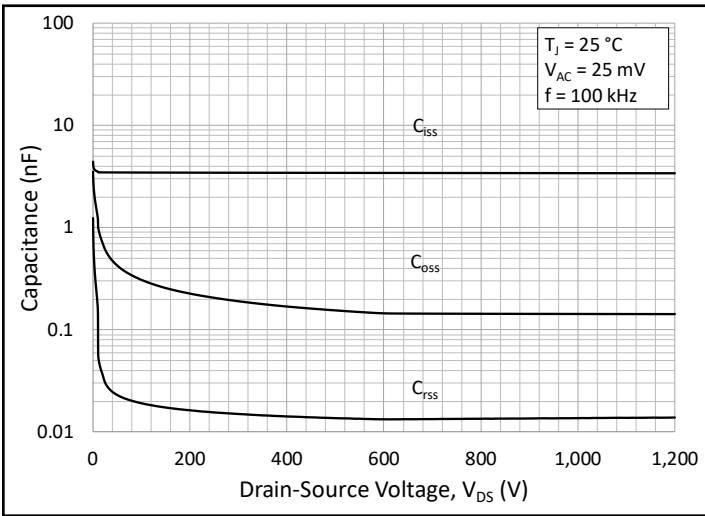


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

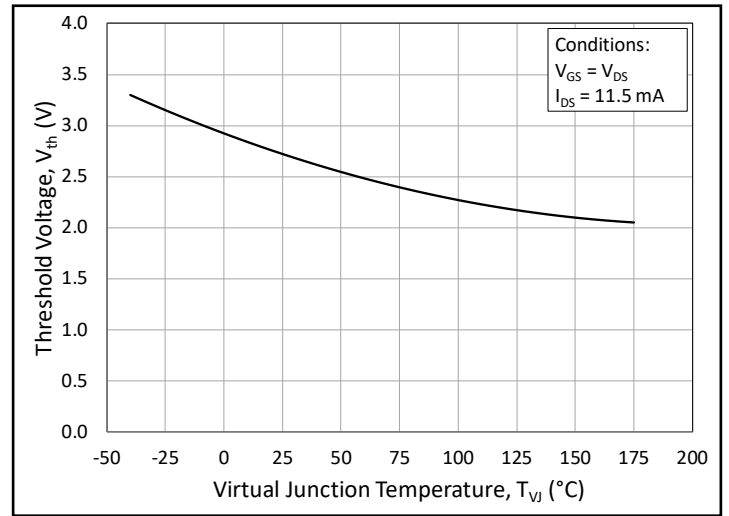


Figure 10. Threshold Voltage vs. Junction Temperature

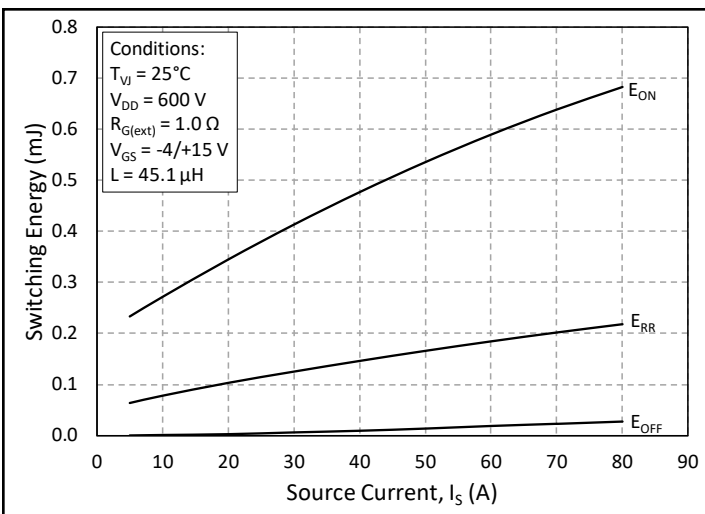


Figure 11. Switching Energy vs. Drain Current ( $V_{DS} = 600\text{ V}$ )

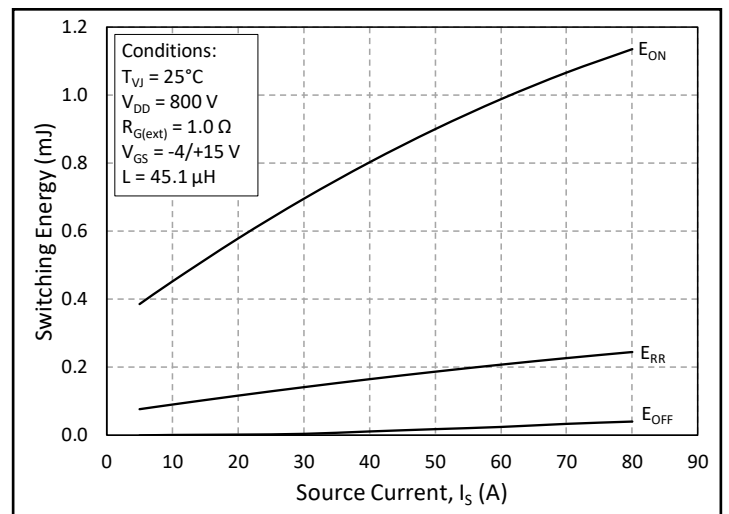


Figure 12. Switching Energy vs. Drain Current ( $V_{DS} = 800\text{ V}$ )

**Typical Performance**

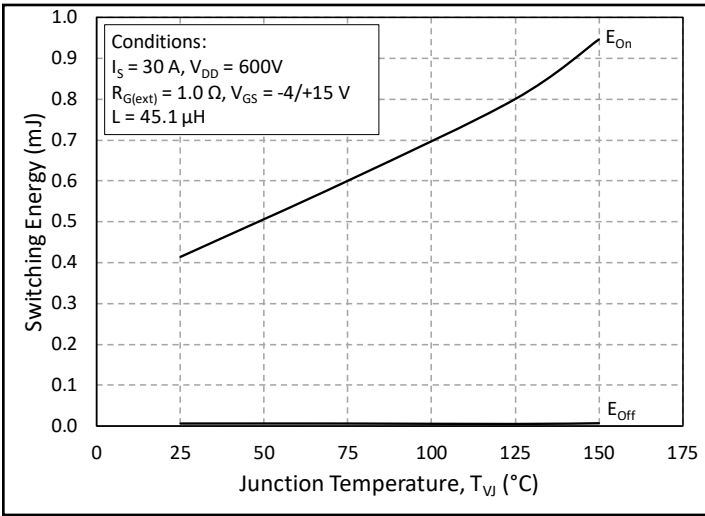


Figure 13. MOSFET Switching Energy vs. Junction Temperature

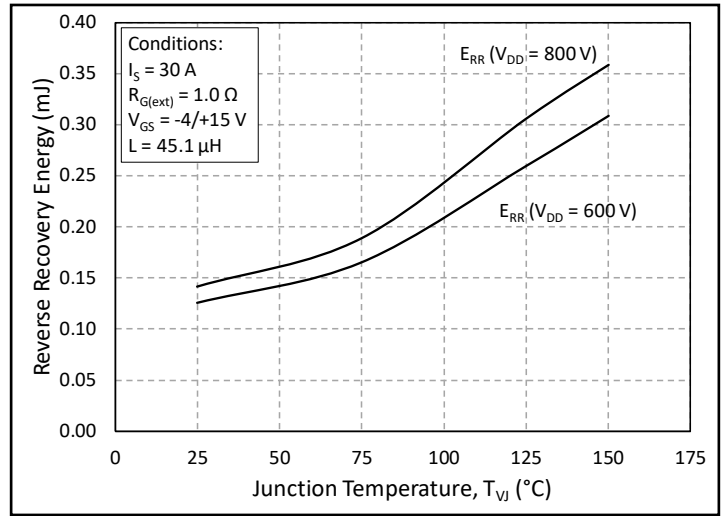


Figure 14. Reverse Recovery Energy vs. Junction Temperature

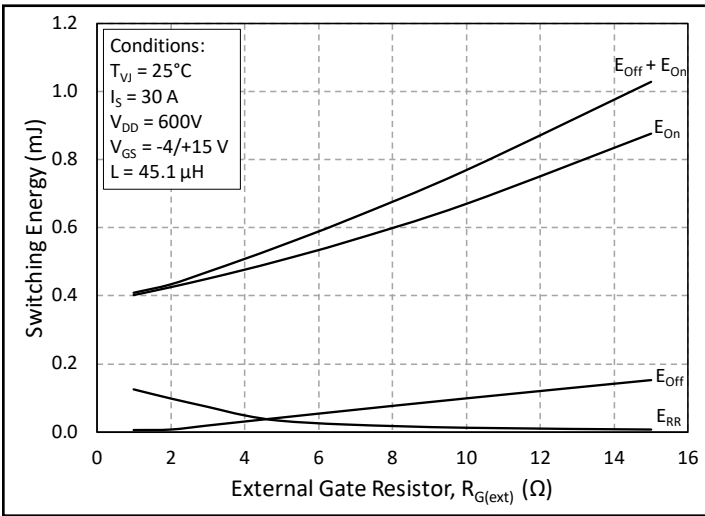


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

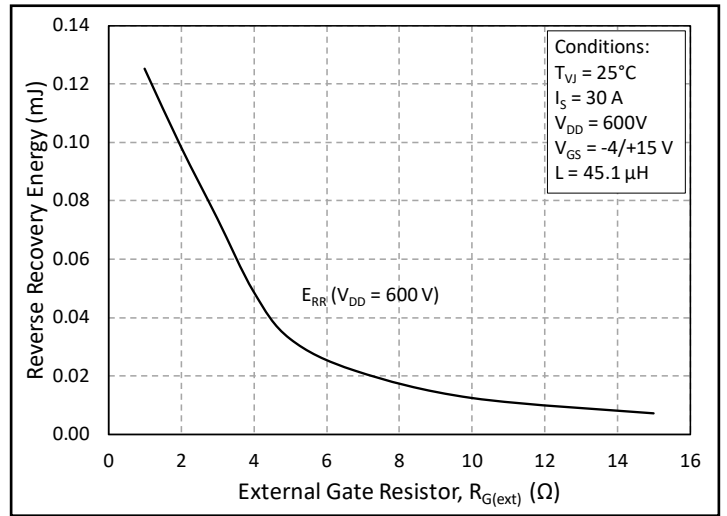


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

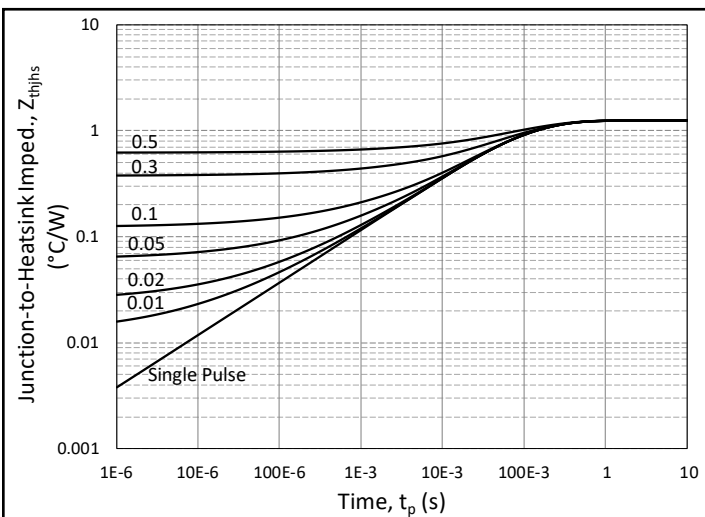


Figure 17. MOSFET Junction to Case Transient Thermal Impedance,  $Z_{thJC}$  (°C/W)

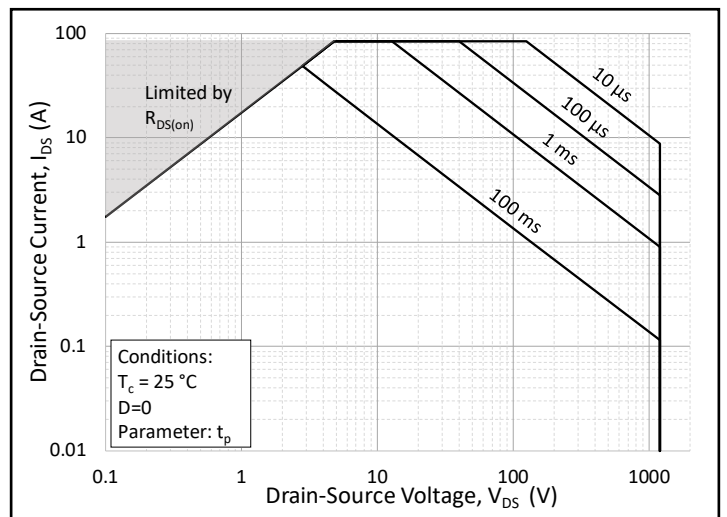


Figure 18. Forward Bias Safe Operating Area (FBSOA)

**Typical Performance**

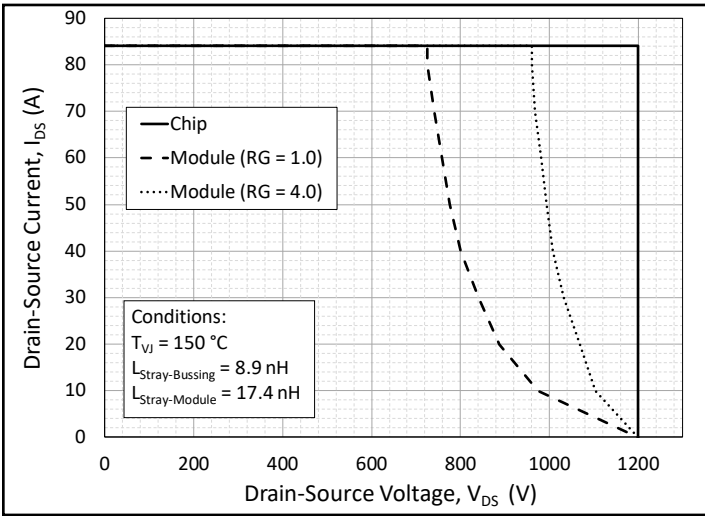


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

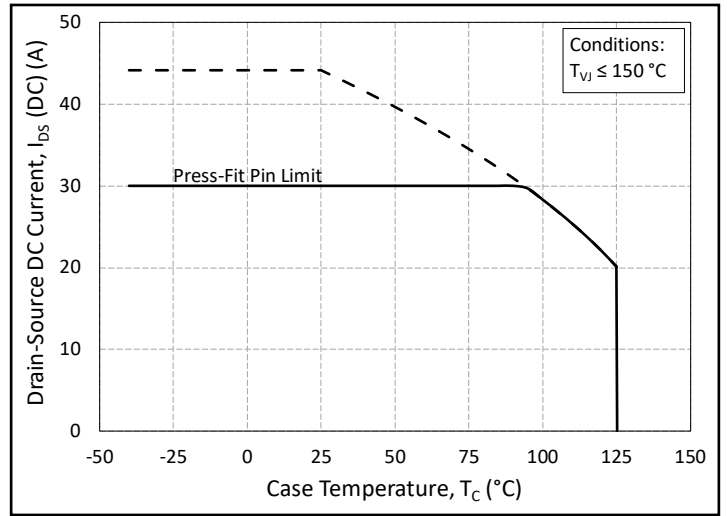


Figure 20. Continuous Drain Current Derating vs. Case Temperature

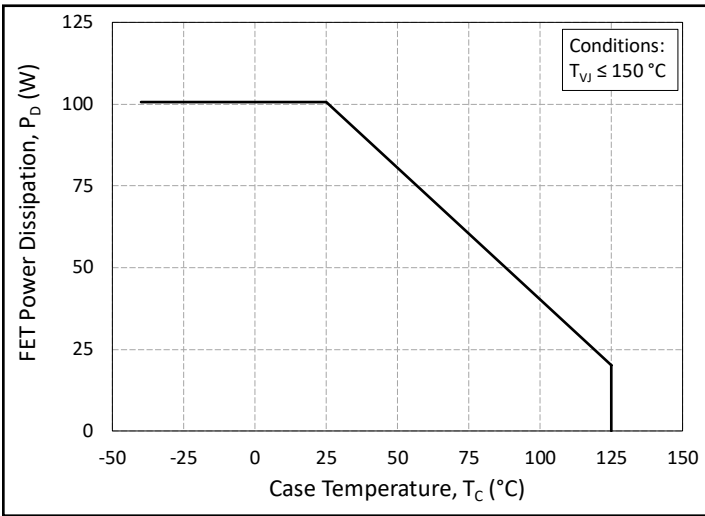


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

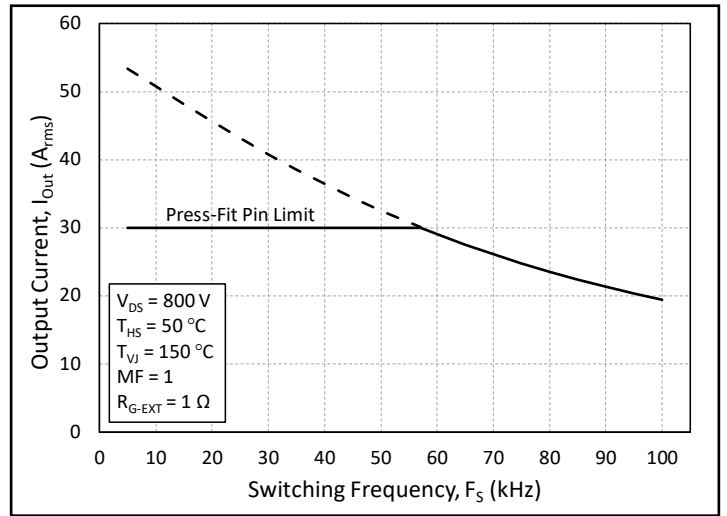


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

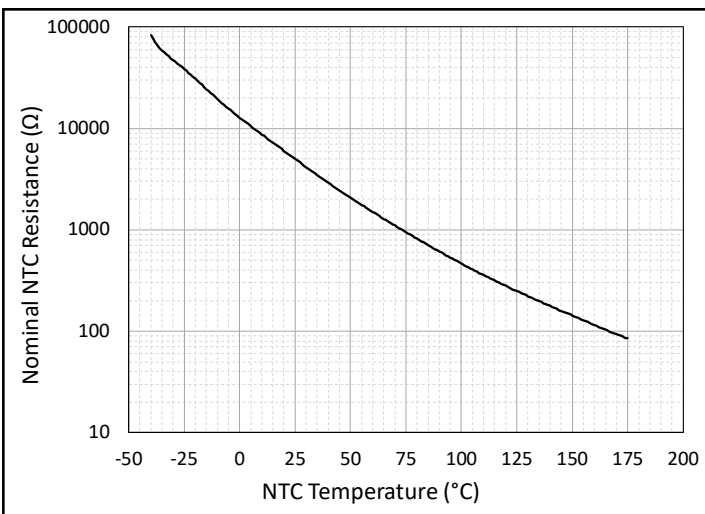


Figure 23. Nominal NTC Resistance vs. NTC Temperature



**Timing Characteristics**

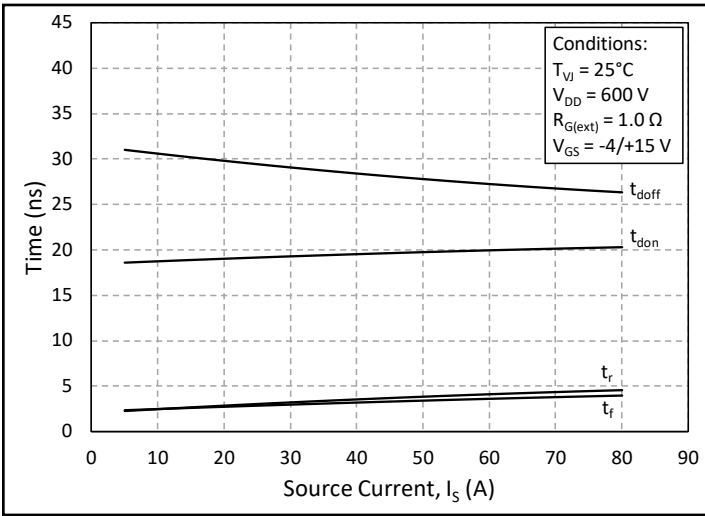


Figure 24. Timing vs. Source Current

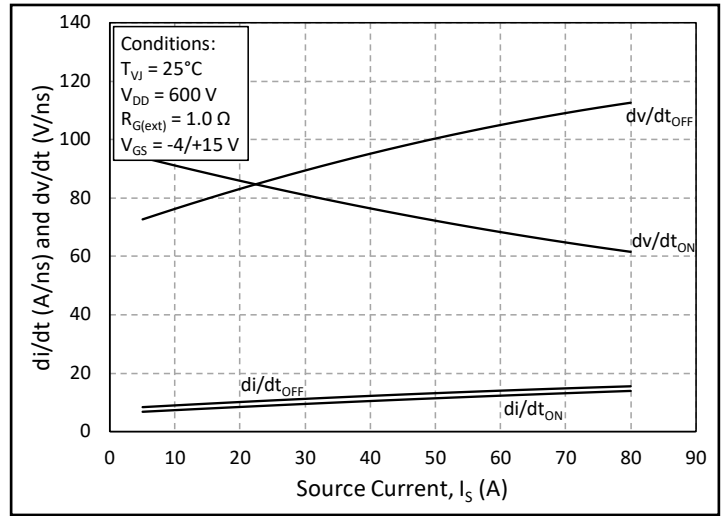


Figure 25. dv/dt and di/dt vs. Source Current

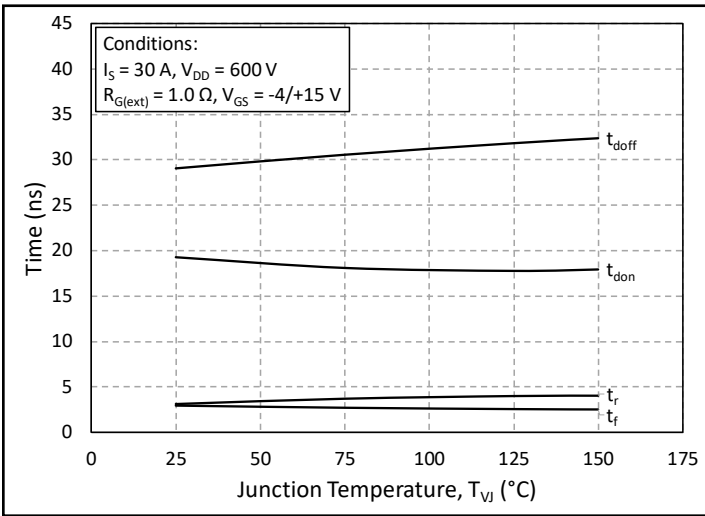


Figure 26. Timing vs. Junction Temperature

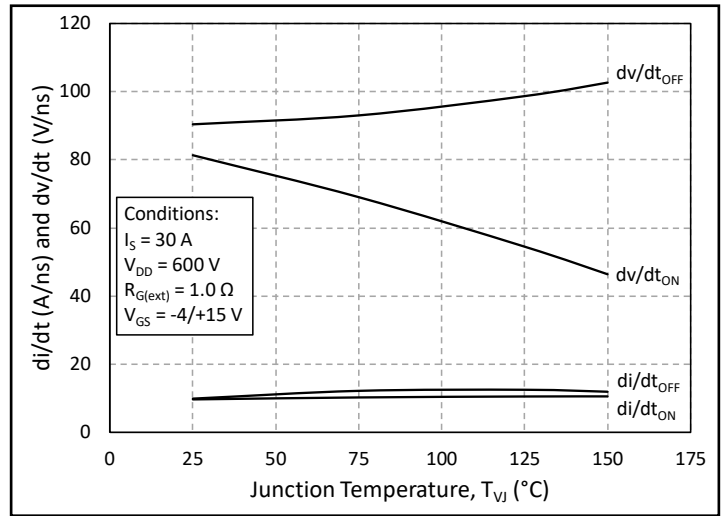


Figure 27. dv/dt and di/dt vs. Junction Temperature

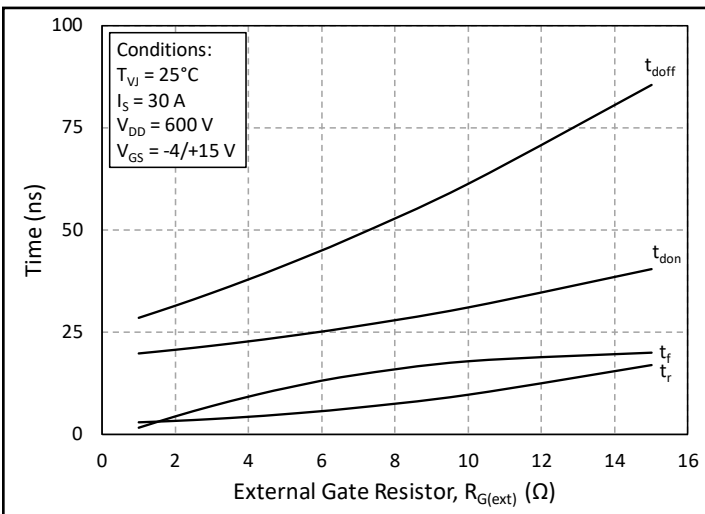


Figure 28. Timing vs. External Gate Resistance

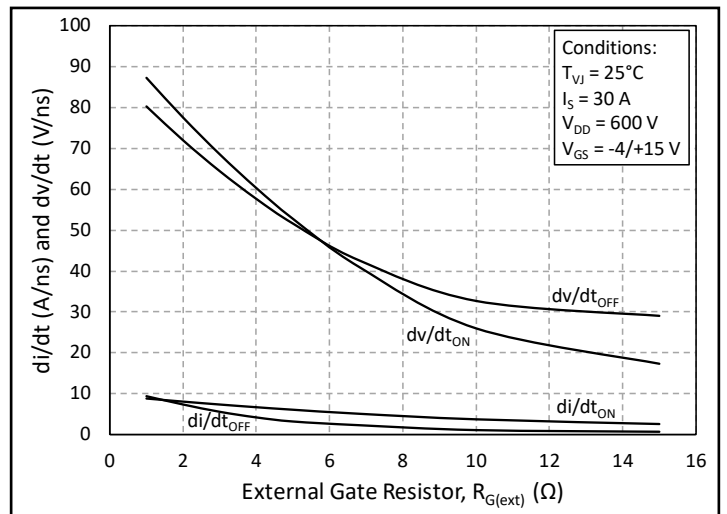


Figure 29. dv/dt and di/dt vs. External Gate Resistance





**Definitions**

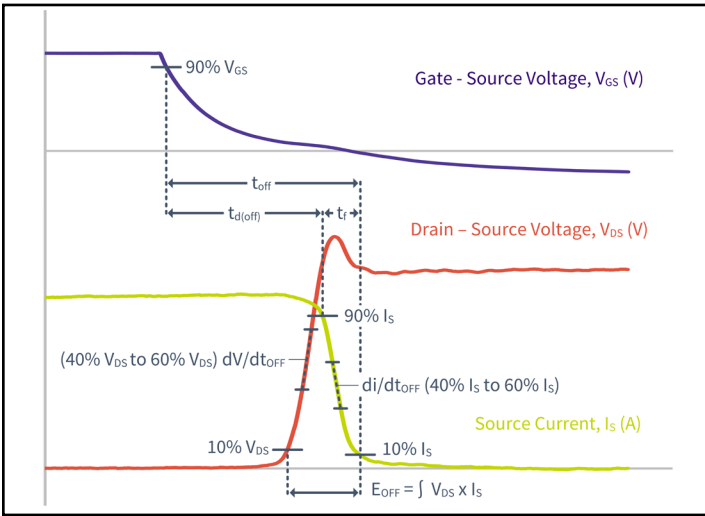


Figure 30. Turn-off Transient Definitions

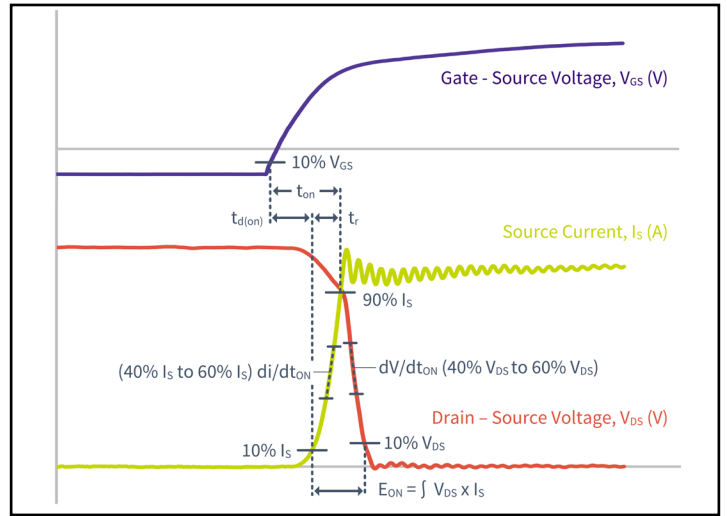


Figure 31. Turn-on Transient Definitions

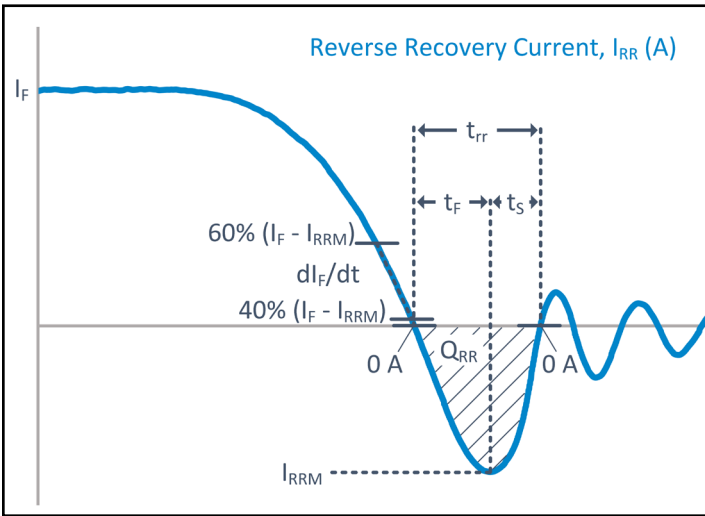


Figure 32. Reverse Recovery Definitions

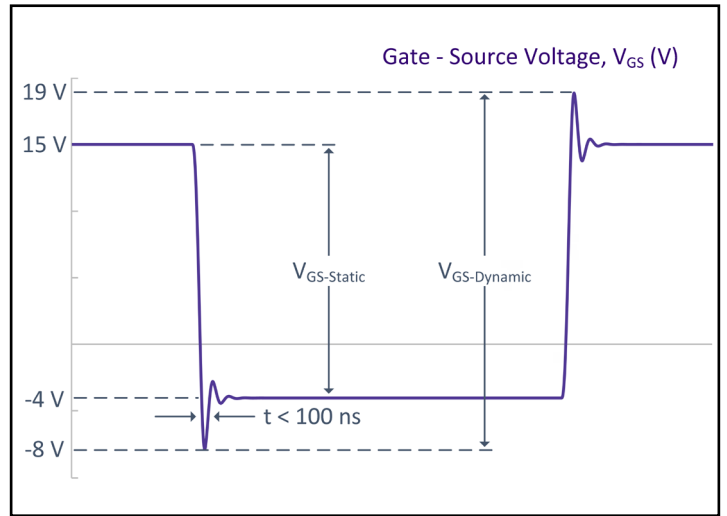
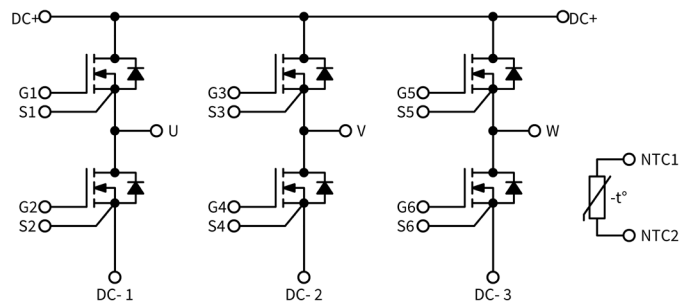
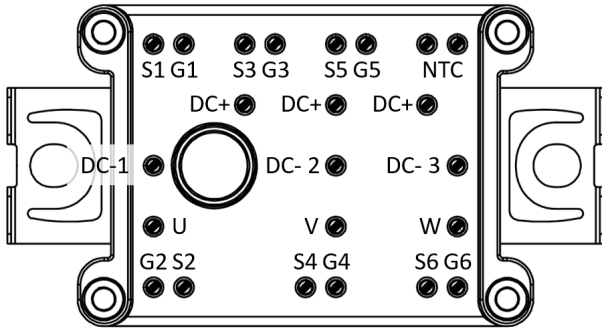


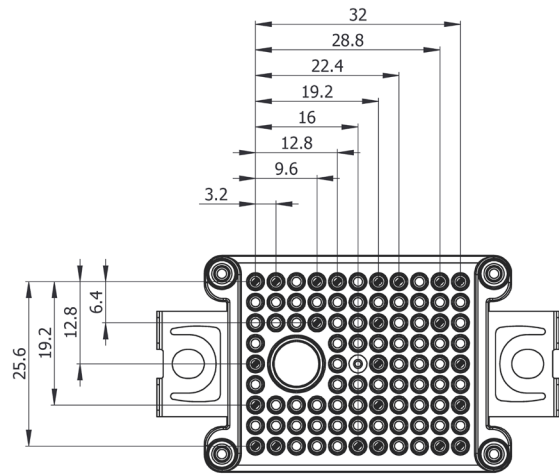
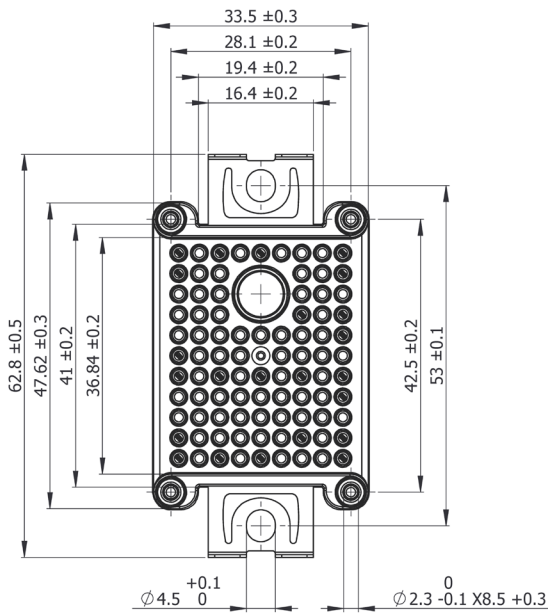
Figure 33.  $V_{GS}$  Transient Definitions



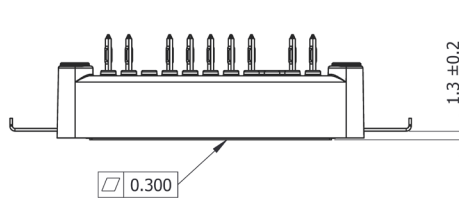
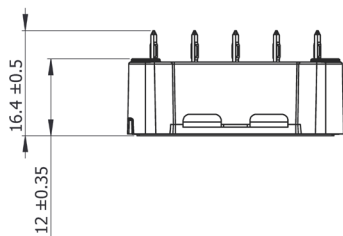
## Schematic and Pin Out



## Package Dimension (mm)



(1) Pin Positions Tolerance  $\oplus \ominus \phi 0.4$



## Supporting Documents & Tools

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### Evaluation Tools

- [KIT-CRD-CIL12N-FMA: Dynamic Evaluation Board for Half-Bridge FM3 Modules](#)
- [KIT-CRD-CIL12N-FMC: Dynamic Evaluation Board for Six-Pack FM3 Modules](#)
- [CRD25AD12N-FMC: 25 kW SiC Active Front End \(AFE\)](#)
- [CCB032M12FM3 PLECS Model](#)
- [SpeedFit 2.0 Design Simulator™](#)

### Dual-Channel Companion Gate Driver Boards

- [EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board](#)
- [Si823H-AxWA-KIT: Silicon Labs® Gate Driver Board](#)
- [CGD1700HB2M-UNA: Wolfspeed Gate Driver Board](#)
- [CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers](#)

### Application Notes

- [CPWR-AN41: Mounting Instructions and PCB Requirements](#)
- [CPWR-AN42: Thermal Interface Material Application Note](#)
- [CPWR-AN45: Dynamic Performance Application Note](#)

## Notes

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- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.
- The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.



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