TJA1081B

FlexRay node transceiver

Rev. 1 — 4 June 2012 Product data sheet

1. General description

The TJA1081B is a FlexRay node transceiver that is fully compliant with the FlexRay electrical physical layer specification V3.0.1 (see Ref. 1). In order to meet the JASPAR-specific requirements, it implements the 'Bus driver increased voltage amplitude transmitter' functional class. It is primarily intended for communication systems from 2.5 Mbit/s to 10 Mbit/s and provides an advanced interface between the protocol controller and the physical bus in a FlexRay network.

The TJA1081B features enhanced low-power modes, optimized for ECUs that are permanently connected to the battery.

The TJA1081B provides differential transmit capability to the network and differential receive capability to the FlexRay controller. It offers excellent EMC performance as well as effective ESD protection.

The TJA1081B actively monitors system performance using dedicated error and status information (that can be read by any microcontroller), along with internal voltage and temperature monitoring.

The TJA1081B supports mode control as used in the TJA1080A (see Ref. 3) and is fully function and footprint compatible with the TJA1081 (see Ref. 2).

2. Features and benefits

2.1 Optimized for time triggered communication systems

- Compliant with FlexRay electrical physical layer specification V3.0.1 (see Ref. 1)
- Meets JASPAR requirements as described in the 'Bus driver increased voltage amplitude transmitter' functional class
- Automotive product qualification in accordance with AEC-Q100
- Data transfer rates from 2.5 Mbit/s to 10 Mbit/s
- Supports 60 ns minimum bit time at 400 mV differential input voltage
- Very low ElectroMagnetic Emissions (EME) to support unshielded cable, meeting latest industry standards
- Differential receiver with wide common-mode range for high ElectroMagnetic Immunity (EMI), meeting latest industry standards
- Auto I/O level adaptation to host controller supply voltage V_{IO}
- Can be used in 14 V, 24 V and 48 V powered systems
- Instant transmitter shut-down interface (via BGE pin)
- Independent power supply ramp-up for V_{BAT}, V_{CC} and V_{IO}

2.2 Low-power management

- Low-power management including inhibit switch
- Very low current in Sleep and Standby modes
- V_{BAT} operating range: 4.75 V to 60 V
- Gap-free specification
- Local and remote wake-up
- Supports remote wake-up via dedicated data frames
- Wake-up source recognition

2.3 Diagnosis (detection and signaling)

- Enhanced supply monitoring of V_{BAT}, V_{CC} and V_{IO}
- Overtemperature detection
- Short-circuit detection on bus lines
- V_{BAT} power-on flag (first battery connection and cold start)
- Clamping diagnosis on pin TXEN
- BGE status feedback

2.4 Protection

- Bus pins protected against ±6 kV ESD pulses according to IEC61000-4-2 and HBM
- Pins V_{BAT} and WAKE protected against ±6 kV ESD pulses according to IEC61000-4-2
- Bus pins protected against transients in automotive environment (according to ISO 7637 class C)
- Bus pins short-circuit proof to battery voltage (14 V, 24 V and 48 V) and ground
- Fail-silent behavior in the event of an undervoltage on pins V_{BAT}, V_{CC} or V_{IO}
- Passive behavior of bus lines while the transceiver is not powered
- No reverse currents from the digital input pins to V_{IO} or V_{CC} when the transceiver is not powered

2.5 Functional classes according to FlexRay electrical physical layer specification (see Ref. 1)

- Bus driver voltage regulator control
- Bus driver - bus guardian interface
- Bus driver logic level adaptation
- Bus driver remote wake-up
- Bus driver increased voltage amplitude transmitter (JASPAR)

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1081BTS	SSOP16	SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1

4. Block diagram

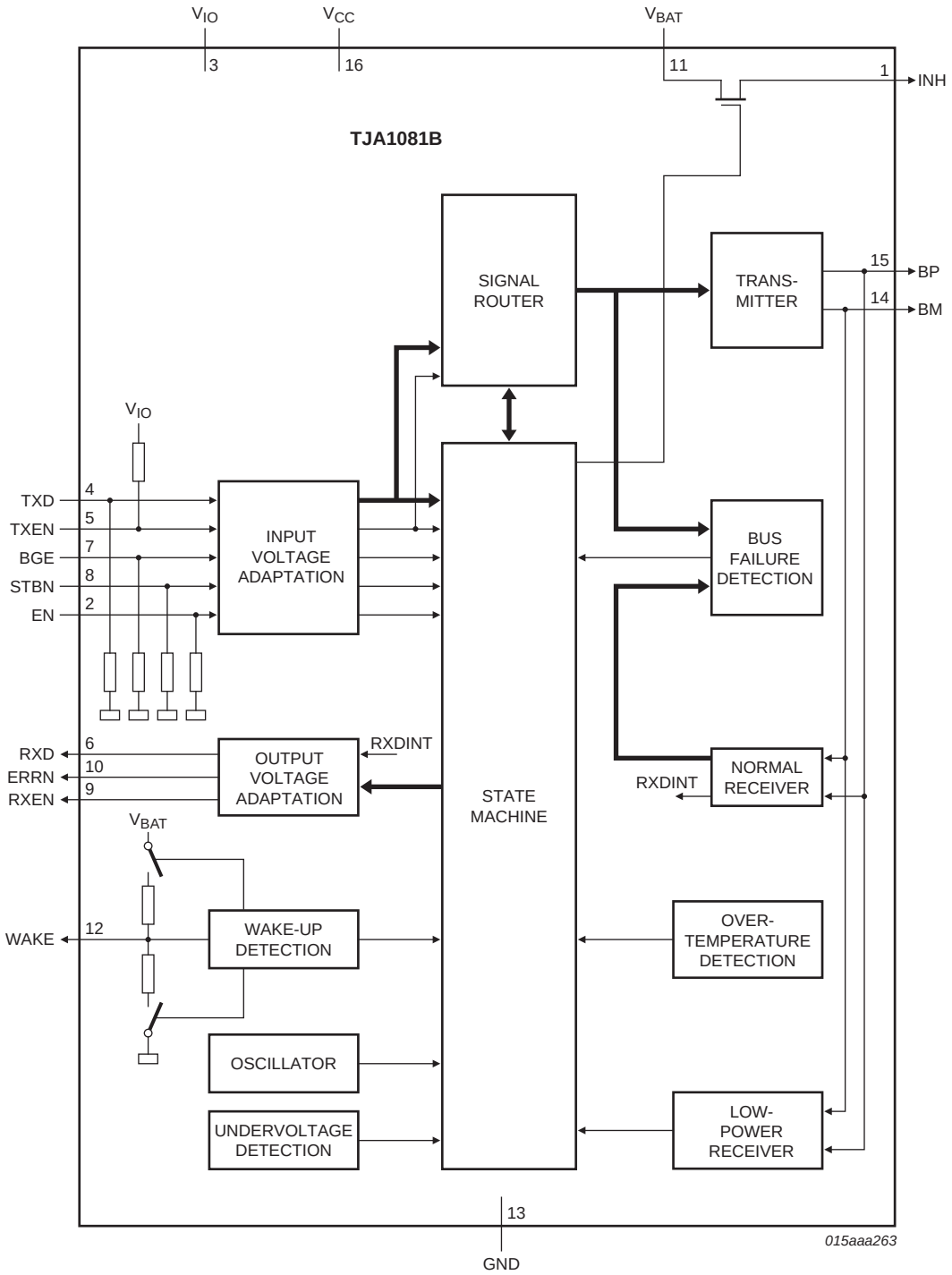


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

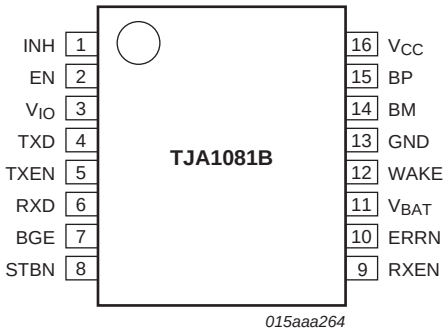


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
INH	1	O	inhibit output for switching external voltage regulator
EN	2	I	enable input; enabled when HIGH; internal pull-down
V_{IO}	3	P	supply voltage for V_{IO} voltage level adaptation
TXD	4	I	transmit data input; internal pull-down
TXEN	5	I	transmitter enable input; when HIGH transmitter disabled; internal pull-up
RXD	6	O	receive data output
BGE	7	I	bus guardian enable input; when LOW transmitter disabled; internal pull-down
STBN	8	I	standby input; low-power mode when LOW; internal pull-down
RXEN	9	O	receive data enable output; when LOW bus activity detected
ERRN	10	O	error diagnoses output; when LOW error detected
V_{BAT}	11	P	battery supply voltage
WAKE	12	I	local wake-up input; internal pull-up or pull-down (depends on voltage at pin WAKE)
GND	13	P	ground
BM	14	I/O	bus line minus
BP	15	I/O	bus line plus
V_{CC}	16	P	supply voltage (+5 V)

6. Functional description

The block diagram of the transceiver is shown in Figure 1.

6.1 Operating modes

The TJA1081B supports the following operating modes:

- Normal (normal-power mode)
- Receive-only (normal-power mode)
- Standby (low-power mode)
- Go-to-sleep (low-power mode)
- Sleep (low-power mode)
- PowerOff

6.1.1 Bus activity and idle detection

The following mechanisms for activity and idle detection are valid in normal-power modes:

- If the absolute differential voltage on the bus lines is higher than $|V_{i(dif)det(act)}|$ for $t_{det(act)(bus)}$, activity is detected on the bus lines; pin RXEN is switched LOW, releasing pin RXD:
  - if, after activity has been detected on the bus, the differential voltage on the bus lines is lower than $V_{IL(dif)}$, pin RXD will go LOW
  - if, after activity has been detected on the bus, the differential voltage on the bus lines is higher than $V_{IH(dif)}$, pin RXD will go HIGH
- If the absolute differential voltage on the bus lines is lower than $|V_{i(dif)det(act)}|$ for $t_{det(idle)(bus)}$, idle is detected on the bus lines; pin RXEN is switched HIGH, blocking pin RXD (pin RXD is switched HIGH or remains HIGH)

6.1.2 Signaling on pin ERRN

Pin ERRN provides either error information or wake-up information. The behavior of ERRN is determined by the host (via pins STBN and EN) and not by the operating mode.

If STBN is LOW, pin ERRN is configured to signal a wake-up event; when STBN and EN are both HIGH, pin ERRN is configured to provide an error alert. Signaling on pin ERRN is described in Table 3.

If pin ERRN goes LOW in Standby or Sleep mode to signal a wake-up event, the host can switch the TJA1081B to Receive only mode (STBN → H) to determine if the wake-up is local or remote. A LOW level on ERRN in Receive only mode (provided the transition to Receive only mode was not triggered by EN going LOW) indicates a remote wake-up was detected; a HIGH signals a local wake-up.

If EN was forced HIGH (to switch the TJA1081B to Normal mode) after an earlier wake-up event, then ERRN will always indicate the error detection status (in both Normal and Receive only modes).

Table 3. Signaling on pin ERRN

STBN	EN	Conditions	ERRN
Normal mode active			
H	H	no error detected	HIGH
H	H	error detected	LOW
Receive only mode active			
H	L	a wake-up was detected (ERRN went LOW in Standby/Sleep mode; EN was not HIGH) before the TJA1081B was switched to Receive only mode	
		local wake-up detected	HIGH
		remote wake-up detected	LOW
H	L	EN was forced HIGH previously in response to an earlier wake-up event before the transition to Receive only mode	
		no error detected	HIGH
		error detected	LOW
Standby or Sleep modes active			
L	X	no local or remote wake-up detected	HIGH
L	X	local or remote wake-up detected	LOW

ERRN is in a high-impedance state in PowerOff mode.

6.1.3 Signaling on pins RXEN and RXD

Signaling on pins RXEN and RXD is determined by the TJA1081B operating mode, as detailed in Table 4.

Table 4. RXEN and RXD signaling

Operating mode	RXEN		RXD		Tx	INH
	LOW	HIGH	LOW	HIGH		
Normal	bus active	bus idle	DATA_0	DATA_1 or idle	enabled	HIGH
Receive-only					disabled	
Go-to-Sleep	local or remote wake-up detected[1]	no local or remote wake-up detected	local or remote wake-up detected[1]	no local or remote wake-up detected		
Standby						
Sleep						floating
PowerOff	high impedance		HIGH			

[1] Valid if V_{IO} and (V_{CC} or V_{BAT}) are present.

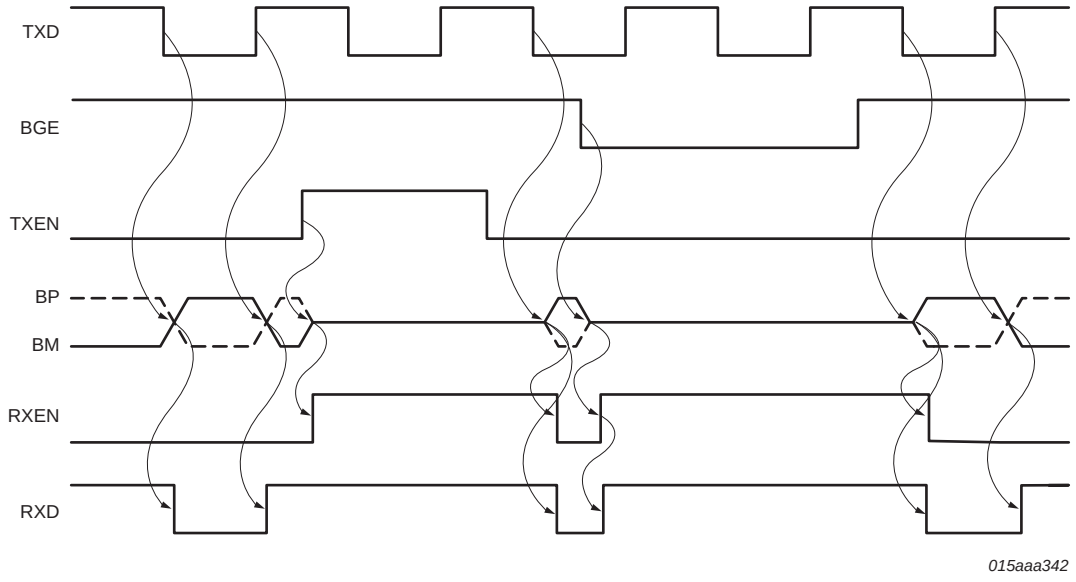


Fig 3. Timing diagram in Normal mode

6.1.4 Operating mode transitions

State transitions are summarized in the state transition diagram in Figure 4 and detailed in Table 5 to Table 8. Numbers are used to represent the state transitions. The numbers in the diagram correspond to the numbers in the third column in the tables.

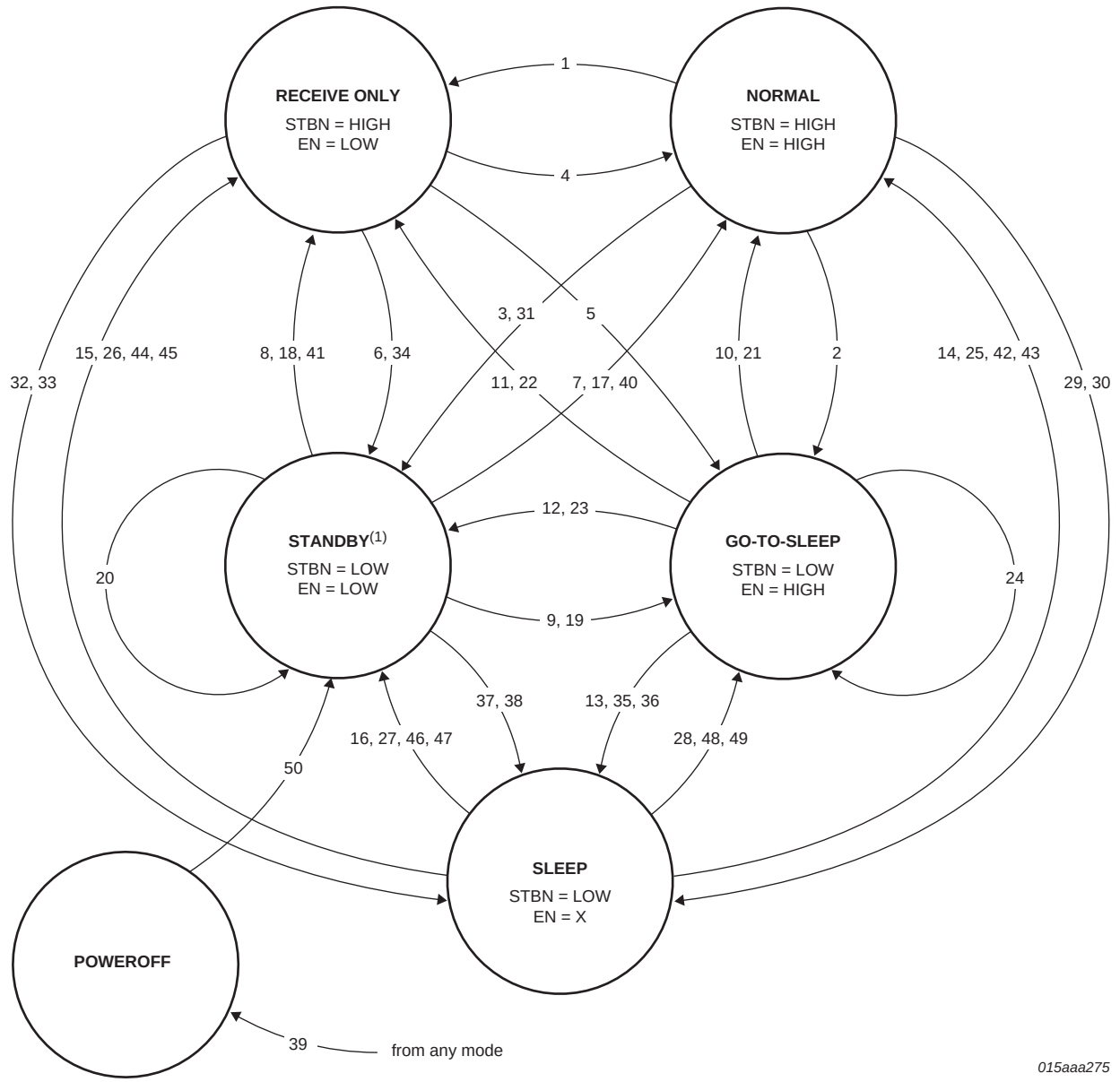


Fig 4. State diagram

Table 5. State transitions forced by EN and STBN

→ indicates the action that initiates a transaction; 1→ and 2 → indicated the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Pin		Flag					Notes
			STBN	EN	UV_{VIO}	UV_{VBAT}	UV_{VCC}	PWON	Wake	
Normal	Receive-only	1	H	→ L	cleared	cleared	cleared	cleared	X	
	Go-to-sleep	2	→ L	H	cleared	cleared	cleared	cleared	X	
	Standby	3	→ L	→ L	cleared	cleared	cleared	cleared	X	
Receive-only	Normal	4	H	→ H	cleared	cleared	cleared	X	X	
	Go-to-sleep	5	→ L	→ H	cleared	cleared	cleared	X	X	
	Standby	6	→ L	L	cleared	cleared	cleared	X	X	
Standby	Normal	7	→ H	→ H	cleared	cleared	cleared	X	X	
	Receive-only	8	→ H	L	cleared	cleared	cleared	X	X	
	Go-to-sleep	9	L	→ H	cleared	cleared	X	X	X	
Go-to-sleep	Normal	10	→ H	H	cleared	cleared	cleared	X	X	[1]
	Receive-only	11	→ H	→ L	cleared	cleared	cleared	X	X	[1]
	Standby	12	L	→ L	cleared	cleared	X	X	X	[1]
	Sleep	13	L	H	cleared	cleared	X	X	cleared	[2]
Sleep	Normal	14	→ H	H	cleared	cleared	cleared	X	X	
	Receive-only	15	→ H	L	cleared	cleared	cleared	X	X	
	Standby	16	→ H	X	cleared	cleared	X	X	X	[3]

[1] Hold time of go-to-sleep is less than $t_{h(gotosleep)}$.

[2] Hold time of go-to-sleep becomes greater than $t_{h(gotosleep)}$.

[3] Transition to a non-low-power mode is blocked when the voltage on pin V_{CC} is below $V_{uvd(VCC)}$ for longer than $t_{det(uv)(VCC)}$.

Table 6. State transitions forced by a wake-up

→ indicates the action that initiates a transaction; 1→ and 2 → indicated the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Pin		Flag					Note
			STBN	EN	UV_{VIO}	UV_{VBAT}	UV_{VCC}	PWON	Wake	
Standby	Normal	17	H	H	cleared	cleared	1 → cleared	X	→ set	[1]
	Receive-only	18	H	L	cleared	cleared	1 → cleared	X	→ set	[1]
	Go-to-sleep	19	L	H	cleared	cleared	1 → cleared	X	→ set	[1]
	Standby	20	L	L	cleared	cleared	1 → cleared	X	→ set	[1]
Go-to-sleep	Normal	21	H	H	cleared	cleared	1 → cleared	X	→ set	[1]
	Receive-only	22	H	L	cleared	cleared	1 → cleared	X	→ set	[1]
	Standby	23	L	L	cleared	cleared	1 → cleared	X	→ set	[1]
	Go-to-sleep	24	L	H	cleared	cleared	1 → cleared	X	→ set	[1]
Sleep	Normal	25	H	H	1 → cleared	1 → cleared	1 → cleared	X	→ set	[1][2]
	Receive-only	26	H	L	1 → cleared	1 → cleared	1 → cleared	X	→ set	[1][2]
	Standby	27	L	L	1 → cleared	1 → cleared	1 → cleared	X	→ set	[1]
	Go-to-sleep	28	L	H	1 → cleared	1 → cleared	1 → cleared	X	→ set	[1][2]

[1] Setting the wake flag clears the UV_{VIO}, UV_{VBAT} and UV_{VCC} flags.

[2] Transition via Standby mode.

Table 7. State transitions forced by an undervoltage condition

→ indicates the action that initiates a transaction; 1→ and 2 → indicated the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Flag					Note
			UV_{VIO}	UV_{VBAT}	UV_{VCC}	PWON	Wake	
Normal	Sleep	29	→ set	cleared	cleared	cleared	1 → cleared	[1]
	Sleep	30	cleared	→ set	cleared	cleared	1 → cleared	[1]
	Standby	31	cleared	cleared	→ set	cleared	1 → cleared	[1][2]
Receive-only	Sleep	32	→ set	cleared	cleared	X	1 → cleared	[1]
	Sleep	33	cleared	→ set	cleared	X	1 → cleared	[1]
	Standby	34	cleared	cleared	→ set	X	1 → cleared	[1][2]
Go-to-sleep	Sleep	35	→ set	cleared	cleared	X	1 → cleared	[1]
	Sleep	36	cleared	→ set	cleared	X	1 → cleared	[1]
Standby	Sleep	37	→ set	cleared	X	X	1 → cleared	[1][3]
	Sleep	38	cleared	→ set	X	X	1 → cleared	[1][4]
X	PowerOff	39	X	X	X	X	X	[5]

[1] UV_{VIO}, UV_{VBAT} or UV_{VCC} detected clears the wake flag.

[2] Transition already completed when the voltage on pin V_{CC} is below $V_{uvd(VCC)}$ for longer than $t_{det(uv)(VCC)}$.

[3] UV_{VIO} overrules UV_{VCC}.

[4] UV_{VBAT} overrules UV_{VCC}.

[5] V_{DIG} (the internal digital supply voltage to the state machine) < $V_{th(det)POR}$.

Table 8. State transitions forced by an undervoltage recovery

→ indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

Transition from mode	Direction to mode	Transition number	Pin		Flag					Note
			STBN	EN	UV_{VIO}	UV_{VBAT}	UV_{VCC}	PWON	Wake	
Standby	Normal	40	H	H	cleared	cleared	→ cleared	X	X	[1]
	Receive-only	41	H	L	cleared	cleared	→ cleared	X	X	[1]
Sleep	Normal	42	H	H	cleared	→ cleared	cleared	X	X	
	Normal	43	H	H	→ cleared	cleared	cleared	X	X	
	Receive-only	44	H	L	cleared	→ cleared	cleared	X	X	
	Receive-only	45	H	L	→ cleared	cleared	cleared	X	X	
	Standby	46	L	L	cleared	→ cleared	cleared	X	X	
	Standby	47	L	L	→ cleared	cleared	cleared	X	X	
	Go-to-sleep	48	L	H	cleared	→ cleared	cleared	X	X	
	Go-to-sleep	49	L	H	→ cleared	cleared	cleared	X	X	
PowerOff	Standby	50	X	X	X	X	X	→ set	X	[2]

[1] Transition already completed when the voltage on pin V_{CC} is above $V_{uvr(VCC)}$ for longer than $t_{rec(uv)(VCC)}$.

[2] The voltage on pin V_{BAT} is above $V_{uvr(VBAT)}$ for longer than $t_{rec(uv)(VBAT)}$ AND V_{DIG} (the internal digital supply voltage to the state machine) > $V_{th(rec)POR}$.

6.1.5 Normal mode

In Normal mode, the transceiver is able to transmit and receive data via bus lines BP and BM. The output of the normal receiver is connected directly to pin RXD.

Transmitter behavior in Normal mode, with no TXEN time-out (see Section 6.4.7) and the temperature flag not set (TEMP HIGH = 0; see Table 10), is detailed in Table 9.

In this mode, pin INH is set HIGH.

Table 9. Transmitter function table

BGE	TXEN	TXD	Transmitter
L	X	X	transmitter is disabled
X	H	X	transmitter is disabled
H	L	H	transmitter is enabled; the bus lines are actively driven; BP is driven HIGH and BM is driven LOW
H	L	L	transmitter is enabled; the bus lines are actively driven; BP is driven LOW and BM is driven HIGH

The transmitter is activated by the first LOW level detected on pin TXD when pin BGE HIGH and pin TXEN is LOW.

6.1.6 Receive-only mode

In Receive-only mode, the transceiver can only receive data. The transmitter is disabled, regardless of the voltage levels on pins BGE and TXEN.

In this mode, pin INH is set HIGH.

6.1.7 Standby mode

Standby mode is a low-power mode featuring very low current consumption. In this mode, the transceiver cannot transmit or receive data. The low-power receiver is activated to monitor the bus for wake-up patterns.

A transition to Standby mode can be triggered by applying the appropriate levels on pins EN and STBN (see Figure 4 and Table 5) or if an undervoltage is detected on pin V_{CC} (see Figure 4 and Section 6.1.9).

In this mode, pin INH is set HIGH.

If the wake flag is set, pins RXEN and RXD are driven LOW; otherwise pins RXEN and RXD are set HIGH (see Section 6.2).

6.1.8 Go-to-sleep mode

In this mode, the transceiver behaves as in Standby mode. If Go-to-sleep mode remains active longer than the go-to-sleep hold time ($t_{h(gotosleep)}$) and the wake flag has been cleared previously, the transceiver switches to Sleep mode regardless of the voltage on pin EN.

6.1.9 Sleep mode

Sleep mode is a low-power mode. The only difference between Sleep mode and Standby mode is that pin INH is set floating in Sleep mode. A transition to Sleep mode is triggered from all other modes when the UV_{VIO} flag or the UV_{VBAT} flag is set (see Table 7).

When the wake flag is set, the undervoltage flags are reset and the transceiver switches from Sleep mode to the mode indicated by the levels on pins EN and STBN (see Table 7), provided V_{IO} is valid.

6.2 Wake-up mechanism

From Sleep mode (pin INH floating), the transceiver enters Standby mode if the wake flag is set. Consequently, pin INH is switched on (HIGH).

If an undervoltage is not detected on pins V_{IO}, V_{CC} or V_{BAT}, the transceiver switches immediately to the mode indicated by the levels on pins EN and STBN.

In Standby, Go-to-sleep and Sleep modes, pins RXD, RXEN and ERRN are driven LOW if the wake flag is set.

6.2.1 Remote wake-up

6.2.1.1 Bus wake-up via wake-up pattern

A valid wake-up pattern on the bus triggers a remote wake-up. A valid remote wake-up pattern consists of a DATA_0, DATA_1 or idle, DATA_0, DATA_1 or idle sequence. The DATA_0 phases must last at least $t_{det(wake)DATA\_0}$ and the DATA_1 or idle phases at least $t_{det(wake)idle}$. The entire sequence must be completed within $t_{det(wake)tot}$.

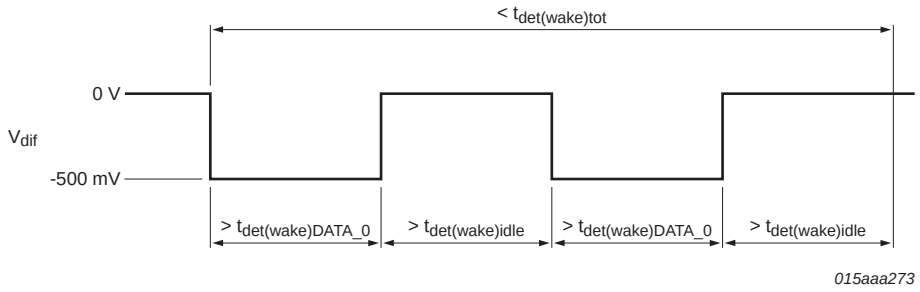


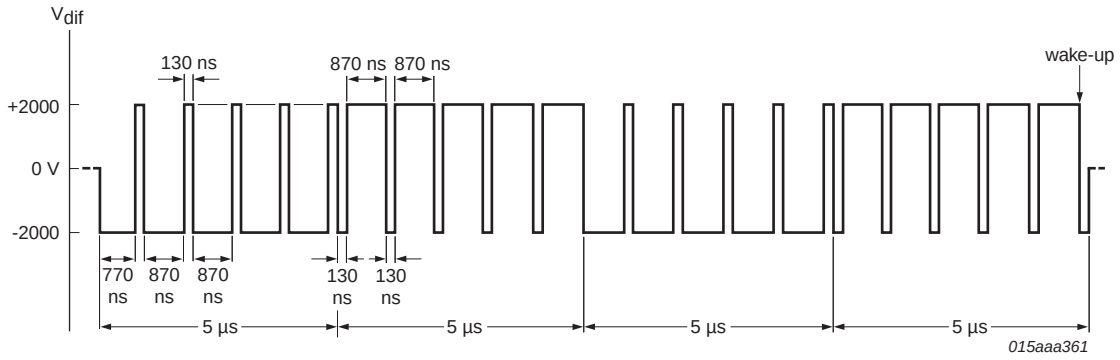
Fig 5. Bus wake-up timing

6.2.1.2 Bus wake-up via dedicated FlexRay data frame

If the TJA1081B receives a dedicated data frame that emulates a valid wake-up pattern as detailed Figure 6, the remote wake-up source flag is set.

Due to the Byte Start Sequence (BSS) preceding each byte, the DATA_0 and DATA_1 phases for the wake-up symbol are interrupted every 1 μs. For 10 Mbit/s the maximum interruption time is 130 ns. Such interruptions do not prevent the transceiver from recognizing the wake-up pattern in the payload of a data frame.

The remote wake-up source flag is not set if an invalid wake-up pattern is received.



Each interruption is 130 ns.

The transition time from DATA_0 to DATA_1 and from DATA_1 to DATA_0 is about 20 ns.

The TJA1081B remote wake-up source flag is set by the following pattern:

FFh, FFh, FFh, FFh, FFh, 00h, 00h, 00h, 00h, 00h,

FFh, FFh, FFh, FFh, FFh, 00h, 00h, 00h, 00h, 00h,

FFh, FFh, FFh, FFh, FFh, 00h, 00h, 00h, 00h, 00h,

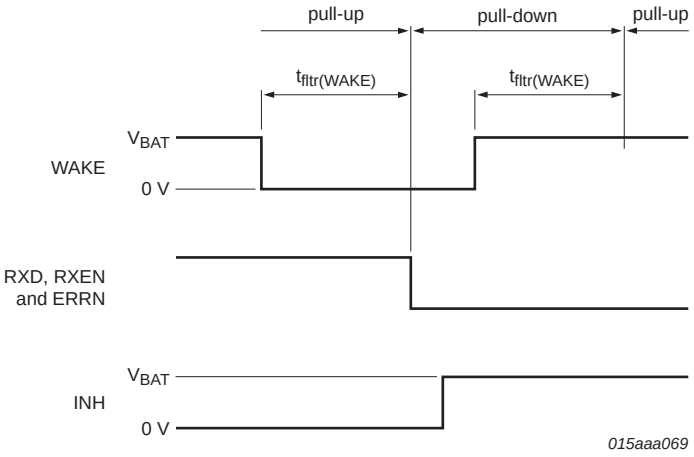
FFh, FFh, FFh, FFh, FFh, FFh

Fig 6. Minimum bus pattern for bus wake-up

6.2.2 Local wake-up via pin WAKE

If the voltage on pin WAKE is lower than $V_{th(det)(WAKE)}$ for longer than $t_{fltr(WAKE)}$ (falling edge on pin WAKE) a local wake-up event on pin WAKE is detected. At the same time, the biasing of this pin is switched to pull-down.

If the voltage on pin WAKE is higher than $V_{th(det)(WAKE)}$ for longer than $t_{fltr(WAKE)}$, the biasing of this pin is switched to pull-up, and a local wake-up is not detected.



Sleep mode: V_{IO} and (V_{BAT} or V_{CC}) still provided.

Fig 7. Local wake-up timing via pin WAKE

6.3 Fail-silent behavior

To ensure fail-silent behavior, a reset mechanism for the digital state machine has been implemented along with undervoltage detection.

If an undervoltage is detected on pins V_{CC}, V_{IO} and/or V_{BAT}, the transceiver switches to a low-power mode. This action ensures that the transmitter and receiver are passive when an undervoltage is detected and that their behavior is defined.

The digital state machine is supplied by V_{CC}, V_{IO} or V_{BAT}, depending on which voltage is available. Therefore, the digital state machine will be properly supplied as long as the voltage on pin V_{CC}, V_{IO} or V_{BAT} remains above 4.5 V.

If the voltage on all pins (i.e. V_{CC}, V_{IO} and V_{BAT}) breaks down, a reset signal is transmitted to the digital state machine. The reset signal is transmitted as soon as the internal supply voltage to the digital state machine is no longer high enough to guarantee proper operation. This ensures that the digital state machine is passive, and its behavior defined, when an undervoltage is detected.

6.3.1 V_{BAT} undervoltage

If the UV_{VBAT} flag is set, the transceiver enters Sleep mode (pin INH is switched off) regardless of the voltage levels on pins EN and STBN. If the undervoltage recovers, the transceiver switches to the mode determined by the voltages on pins EN and STBN.

6.3.2 V_{CC} undervoltage

If the UV_{VCC} flag is set, the transceiver switches to Standby mode regardless of the voltage levels on pins EN and STBN. If the undervoltage recovers or the wake flag is set, mode switching via pins EN and STBN is again enabled.

6.3.3 V_{IO} undervoltage

If the voltage on pin V_{IO} is lower than $V_{uvd(VIO)}$ for longer than $t_{det(uv)(VIO)}$ (even if the UV_{VIO} flag is reset) pins EN, STBN, TXD and BGE are set LOW (internally) and pin TXEN is set HIGH (internally). If the UV_{VIO} flag is set, the transceiver enters Sleep mode (pin INH is switched off). If the undervoltage recovers or the wake flag is set, mode switching via pins EN and STBN is again enabled.

6.4 Flags

6.4.1 Local wake-up source flag

The local wake-up source flag can only be set in a low-power mode. When a wake-up event is detected on pin WAKE (see Section 6.2.2), the local wake-up source flag is set. The local wake-up source flag is reset by entering a low-power mode.

6.4.2 Remote wake-up source flag

The remote wake-up source flag can only be set in a low-power mode if pin V_{BAT} is within its operating range. When a remote wake-up event is detected on the bus lines (see Section 6.2.1), the remote wake-up source flag is set. The remote wake-up source flag is reset by entering a low-power mode.

6.4.3 Wake flag

The wake flag is set if the local or remote wake-up source flag is set. The wake flag is reset by entering a low-power mode or by setting one of the undervoltage flags.

6.4.4 Power-on flag

If the internal supply voltage to the digital section rises above the minimum operating level, the PWON power-on flag is set. The PWON flag is reset when the TJA1081B enters Normal mode.

6.4.5 Temperature medium flag

If the junction temperature exceeds $T_{j(warn)(medium)}$ in a normal-power mode, the temperature medium flag is set. The temperature medium flag is reset when the junction temperature drops below $T_{j(warn)(medium)}$ (in a normal-power mode or after the status register has been read in a low-power mode). No action is taken when this flag is set.

6.4.6 Temperature high flag

If the junction temperature exceeds $T_{j(dis)(high)}$ in a normal-power mode, the temperature high flag is set. If a negative edge is applied to pin TXEN while the junction temperature is below $T_{j(dis)(high)}$ in a normal-power mode, the temperature high flag is reset.

The transmitter is disabled when the temperature high flag is set.

6.4.7 TXEN clamped flag

The TXEN clamped flag is set if pin TXEN is LOW for longer than $t_{detCL(TXEN)}$. The TXEN clamped flag is reset if pin TXEN is HIGH. If the TXEN clamped flag is set, the transmitter is disabled.

6.4.8 Bus error flag

The bus error flag is set if pin TXEN is LOW, pin BGE is HIGH and the data received on the bus lines (pins BP and BM) is different to that received on pin TXD. The transmission of any valid communication element, including a wake-up pattern, will not be detected as a bus error.

The bus error flag is reset if the data on the bus lines (pins BP and BM) is the same as on pin TXD or if the transmitter is disabled. No action is taken when the bus error flag is set.

6.4.9 UV_{VBAT} flag

The UV_{VBAT} flag is set if the voltage on pin V_{BAT} is lower than $V_{uvd(VBAT)}$ for longer than $t_{det(uv)(VBAT)}$. The UV_{VBAT} flag is reset if the voltage is higher than $V_{uvr(VBAT)}$ for longer than $t_{to(uvr)(VBAT)}$ or by setting the wake flag; see Section 6.3.1.

6.4.10 UV_{VCC} flag

In a non-low-power mode, the UV_{VCC} flag is set if the voltage on pin V_{CC} is lower than $V_{uvd(VCC)}$ for longer than $t_{det(uv)(VCC)}$. In a low-power mode, the UV_{VCC} flag is set if the voltage on pin V_{CC} is lower than $V_{uvd(VCC)}$ for longer than $t_{to(uvd)(VCC)}$. The UV_{VCC} flag is reset if the voltage on pin V_{CC} is higher than $V_{uvr(VCC)}$ for longer than $t_{to(uvr)(VCC)}$ or the wake flag is set; see Section 6.3.2.

6.4.11 UV_{VIO} flag

The UV_{VIO} flag is set if the voltage on pin V_{IO} is lower than $V_{uvd(VIO)}$ for longer than $t_{to(uvd)(VIO)}$. The flag is reset if the voltage on pin V_{IO} is higher than $V_{uvr(VIO)}$ for longer than $t_{to(uvr)(VIO)}$ or the wake flag is set; see Section 6.3.3.

6.5 Status register

Pin ERRN goes LOW when one or more of status bits S4 to S10 is set. The contents of the status register (Table 10) can be read out on pin ERRN using the input signal on pin EN as a clock. The timing diagram is shown in Figure 8.

The status register is accessible if:

- UV_{VIO} flag is not set and the voltage on pin V_{IO} is between 4.75 V and 5.25 V
- UV_{VCC} flag is not set and the voltage on pin V_{IO} is between 2.8 V and 4.75 V

After reading the status register, if an edge is not detected on pin EN for $t_{det(EN)}$, status bits S4 to S10 are cleared provided the corresponding flags have been reset.

Table 10. Status bits

Bit number	Status bit	Description
S0	LOCAL WAKEUP	local wake-up source flag is redirected to this bit
S1	REMOTE WAKEUP	remote wake-up source flag is redirected to this bit
S2	-	not used; always set
S3	PWON	status bit set means PWON flag has been set previously
S4	BUS ERROR	status bit set means bus error flag has been set previously
S5	TEMP HIGH	status bit set means temperature high flag has been set previously
S6	TEMP MEDIUM	status bit set means temperature medium flag has been set previously
S7	TXEN CLAMPED	status bit set means TXEN clamped flag has been set previously
S8	UVVBAT	status bit set means UV_{VBAT} flag has been set previously
S9	UVVCC	status bit set means UV_{VCC} flag has been set previously
S10	UVVIO	status bit set means UV_{VIO} flag has been set previously
S11	BGE FEEDBACK	BGE feedback (status bit reset if pin BGE LOW; status bit set if pin BGE HIGH)
S12	-	not used; always reset

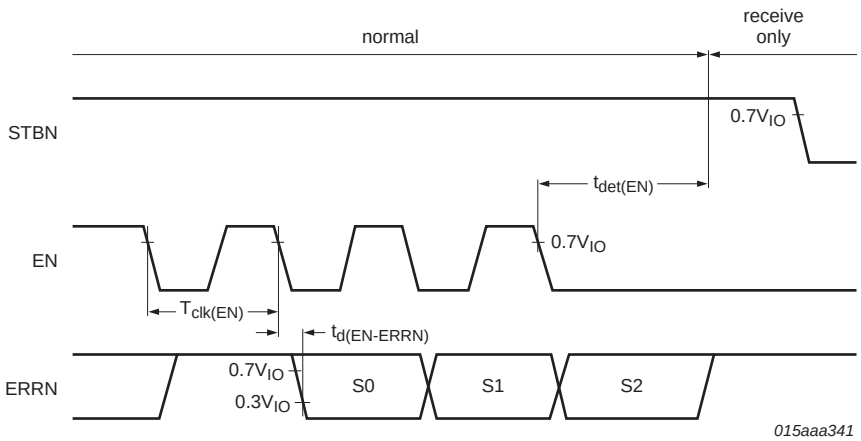


Fig 8. Timing diagram for status bits

7. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to ground.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{BAT}	battery supply voltage	no time limit		–0.3	+60	V
		operating range		4.75	60	V
V_{CC}	supply voltage	no time limit		–0.3	+5.5	V
		operating range		4.75	5.25	V
V_{IO}	supply voltage on pin V_{IO}	no time limit		–0.3	+5.5	V
		operating range		2.8	5.25	V
V_{INH}	voltage on pin INH			–0.3	V_{BAT} + 0.3	V
$I_{O(INH)}$	output current on pin INH	no time limit		–1	-	mA
V_{WAKE}	voltage on pin WAKE			–0.3	V_{BAT} + 0.3	V
$I_{o(WAKE)}$	output current on pin WAKE	pin GND not connected		–15	-	mA
V_{BGE}	voltage on pin BGE	no time limit		–0.3	+5.5	V
V_{TXEN}	voltage on pin TXEN	no time limit		–0.3	+5.5	V
V_{TXD}	voltage on pin TXD	no time limit		–0.3	+5.5	V
V_{ERRN}	voltage on pin ERRN	no time limit		–0.3	V_{IO} + 0.3	V
V_{RXD}	voltage on pin RXD	no time limit		–0.3	V_{IO} + 0.3	V
V_{RXEN}	voltage on pin RXEN	no time limit		–0.3	V_{IO} + 0.3	V
V_{EN}	voltage on pin EN	no time limit		–0.3	+5.5	V
V_{STBN}	voltage on pin STBN	no time limit		–0.3	+5.5	V
V_{BP}	voltage on pin BP	no time limit; with resect to pins BM, V_{BAT}, WAKE, INH and GND		–60	+60	V
V_{BM}	voltage on pin BM	no time limit; with resect to pins BP, V_{BAT}, WAKE, INH and GND		–60	+60	V
V_{trt}	transient voltage	on pins BM and BP	[1]	–100	-	V
			[2]	-	75	V
			[3]	–150	-	V
			[4]	-	100	V
T_{stg}	storage temperature			–55	+150	°C
T_{vj}	virtual junction temperature		[5]	–40	+150	°C
T_{amb}	ambient temperature			–40	+125	°C
V_{ESD}	electrostatic discharge voltage	HBM on pins BP and BM to ground	[6]	–6.0	+6.0	kV
		HBM on pins V_{BAT} and WAKE to ground	[6]	–4.0	+4.0	kV
		HBM at all other pins	[6]	–2.0	+2.0	kV
		MM on all pins	[7]	–100	+100	V
		CDM on corner pins	[8]	–750	+750	V
		CDM on all other pins	[8]	–500	+500	V
		IEC61000-4-2 on pins BP and BM to ground	[9]	–6.0	+6.0	kV
		IEC61000-4-2 on pin V_{BAT} to ground	[9][10]	–6.0	+6.0	kV
		IEC61000-4-2 on pin WAKE to ground	[9][11]	–6.0	+6.0	kV

[1] According to ISO7637, test pulse 1, class C; verified by an external test house.

[2] According to ISO7637, test pulse 2a, class C; verified by an external test house.

[3] According to ISO7637, test pulse 3a, class C; verified by an external test house.

[4] According to ISO7637, test pulse 3b, class C; verified by an external test house.

[5] In accordance with IEC 60747-1. An alternative definition of T_{vj} is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

[6] HBM: C = 100 pF; R = 1.5 kΩ.

[7] MM: C = 200 pF; L = 0.75 μH; R = 10 Ω.

[8] CDM: R = 1 Ω.

[9] IEC61000-4-2: C = 150 pF; R = 330 Ω; verified by an external test house. The test result is equal to or better than ±6 kV (unaided).

[10] With 100 nF from V_{BAT} to GND.

[11] With 3.3 kΩ in series.

8. Thermal characteristics

Table 12. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	118	K/W

9. Static characteristics

Table 13. Static characteristics

All parameters are guaranteed for V_{BAT} = 4.45 V to 60 V; V_{CC} = 4.45 V to 5.25 V; V_{IO} = 2.55 V to 5.25 V; T_{vj} = −40 °C to +150 °C; C_{bus} = 100 pF; R_{bus} = 40 Ω to 55 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin V_{BAT}						
I_{BAT}	battery supply current	low-power modes; no load on pin INH	-	-	55	μA
		normal-power modes	-	-	1	mA
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin V_{BAT}		4.45	-	4.715	V
$V_{uvr(VBAT)}$	undervoltage recovery voltage on pin V_{BAT}		4.475	-	4.74	V
$V_{uvhys(VBAT)}$	undervoltage hysteresis voltage on pin V_{BAT}		25	-	290	mV
Pin V_{CC}						
I_{CC}	supply current	low-power modes	−1	+2	+10	μA
		Normal mode; V_{BGE} = 0 V; V_{TXEN} = V_{IO}; Receive-only mode	-	11	22	mA
		Normal mode; V_{BGE} = V_{IO}; V_{TXEN} = 0 V	-	47	60	mA
		Normal mode; V_{BGE} = V_{IO}; V_{TXEN} = 0 V; R_{bus} = ∞ Ω	-	21	40	mA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		4.45	-	4.72	V

Table 13. Static characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 4.45 V to 60 V; V_{CC} = 4.45 V to 5.25 V; V_{IO} = 2.55 V to 5.25 V; T_{vj} = −40 °C to +150 °C; C_{bus} = 100 pF; R_{bus} = 40 Ω to 55 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{uvr(VCC)}$	undervoltage recovery voltage on pin V_{CC}		4.47	-	4.74	V
$V_{uvhys(VCC)}$	undervoltage hysteresis voltage on pin V_{CC}		20	-	290	mV
Pin V_{IO}						
I_{IO}	supply current on pin V_{IO}	low-power modes; $V_{TXEN} = V_{IO}$	−1	+2	+10	µA
		Normal and Receive-only modes; $V_{TXD} = V_{IO}$	-	-	1000	µA
$I_{r(VIO)}$	reverse current on pin V_{IO}	from digital input pins; PowerOff mode; V_{TXEN} = 5.25 V; V_{TXD} = 5.25 V; V_{BGE} = 5.25 V; V_{EN} = 5.25 V; V_{STBN} = 5.25 V; $V_{CC} = V_{IO}$ = 0 V	−5	-	+5	µA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		2.55	-	2.765	V
$V_{uvr(VIO)}$	undervoltage recovery voltage on pin V_{IO}		2.575	-	2.79	V
$V_{uvhys(VIO)}$	undervoltage hysteresis voltage on pin V_{IO}		25	-	240	mV
Pin EN						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{EN} = 0.7V_{IO}$	3	-	15	µA
I_{IL}	LOW-level input current	V_{EN} = 0 V	−1	0	+1	µA
Pin STBN						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{STBN} = 0.7V_{IO}$	3	-	15	µA
I_{IL}	LOW-level input current	V_{STBN} = 0 V	−1	0	+1	µA
Pin TXEN						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{TXEN} = V_{IO}$	−1	0	+1	µA
I_{IL}	LOW-level input current	$V_{TXEN} = 0.3V_{IO}$	−300	-	−50	µA
I_L	leakage current	V_{TXEN} = 5.25 V; V_{IO} = 0 V	−1	0	+1	µA
Pin BGE						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{BGE} = 0.7V_{IO}$	3	-	15	µA
I_{IL}	LOW-level input current	V_{BGE} = 0 V	−1	0	+1	µA
Pin TXD						

Table 13. Static characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 4.45 V to 60 V; V_{CC} = 4.45 V to 5.25 V; V_{IO} = 2.55 V to 5.25 V; T_{vj} = −40 °C to +150 °C; C_{bus} = 100 pF; R_{bus} = 40 Ω to 55 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	normal-power modes		$0.6V_{IO}$	-	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage	normal-power modes		−0.3	-	$0.4V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{TXD} = V_{IO}$		3	-	15	µA
I_{IL}	LOW-level input current	normal-power modes; V_{TXD} = 0 V		−5	0	+5	µA
		low-power modes		−1	0	+1	µA
I_{LI}	input leakage current	V_{TXD} = 5.25 V; V_{IO} = 0 V		−1	0	+1	µA
C_i	input capacitance	not tested; with respect to all other pins at ground; V_{TXD} = 100 mV; f = 5 MHz	[1]	-	5	10	pF
Pin RXD							
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO}$ − 0.4 V; $V_{IO} = V_{CC}$		−20	-	−2	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V		2	-	20	mA
V_{OH}	HIGH-level output voltage	$I_{OH(RXD)}$ = −2 mA	[1]	V_{IO} − 0.4	-	V_{IO}	V
V_{OL}	LOW-level output voltage	$I_{OL(RXD)}$ = 2 mA	[1]	-	-	0.4	V
V_O	output voltage	when undervoltage on V_{IO}; $V_{CC} \geq$ 4.75 V; R_L = 100 kΩ to ground		-	-	0.5	V
		R_L = 100 kΩ to V_{IO}; power off		V_{IO} − 0.5	-	V_{IO}	V
Pin ERRN							
I_{OH}	HIGH-level output current	$V_{ERRN} = V_{IO}$ − 0.4 V; $V_{IO} = V_{CC}$		−8	−3	−0.5	mA
I_{OL}	LOW-level output current	V_{ERRN} = 0.4 V		0.5	2	8	mA
V_{OH}	HIGH-level output voltage	$I_{OH(ERRN)}$ = −0.5 mA	[1]	V_{IO} − 0.4	-	V_{IO}	V
V_{OL}	LOW-level output voltage	$I_{OL(ERRN)}$ = 0.5 mA	[1]	-	-	0.4	V
I_L	leakage current	0 V ≤ $V_{ERRN} \leq V_{IO}$; power off		−5	0	+5	µA
V_O	output voltage	when undervoltage on V_{IO}; V_{CC} > 4.75 V; R_L = 100 kΩ to ground		-	-	0.5	V
		R_L = 100 kΩ to ground; power off		-	-	0.5	V
Pin RXEN							
I_{OH}	HIGH-level output current	$V_{RXEN} = V_{IO}$ − 0.4 V; $V_{IO} = V_{CC}$		−8	−3	−0.5	mA
I_{OL}	LOW-level output current	V_{RXEN} = 0.4 V		0.5	2	8	mA
V_{OH}	HIGH-level output voltage	$I_{OH(RXEN)}$ = −0.5 mA	[1]	V_{IO} − 0.4	-	V_{IO}	V

Table 13. Static characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 4.45 V to 60 V; V_{CC} = 4.45 V to 5.25 V; V_{IO} = 2.55 V to 5.25 V; T_{vj} = −40 °C to +150 °C; C_{bus} = 100 pF; R_{bus} = 40 Ω to 55 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$I_{OL(RXEN)}$ = 0.5 mA	[1]	-	-	0.4	V
I_L	leakage current	0 V ≤ V_{RXEN} ≤ V_{IO}; power off		−5	0	+5	µA
V_O	output voltage	when undervoltage on V_{IO}; V_{CC} > 4.75 V; R_L = 100 kΩ to ground		-	-	0.5	V
		R_L = 100 kΩ to V_{IO}; power off		V_{IO} − 0.5	-	V_{IO}	V
Pins BP and BM							
$V_{o(idle)(BP)}$	idle output voltage on pin BP	Normal or Receive-only mode; V_{TXEN} = V_{IO}; 4.5 V ≤ V_{CC} ≤ 5.25 V		$0.4V_{CC}$	$0.5V_{CC}$	$0.6V_{CC}$	V
		Standby, Go-to-sleep or Sleep mode		−0.1	0	+0.1	V
$V_{o(idle)(BM)}$	idle output voltage on pin BM	Normal or Receive-only mode; V_{TXEN} = V_{IO}; 4.5 V ≤ V_{CC} ≤ 5.25 V		$0.4V_{CC}$	$0.5V_{CC}$	$0.6V_{CC}$	V
		Standby, Go-to-sleep or Sleep mode		−0.1	0	+0.1	V
$I_{o(idle)BP}$	idle output current on pin BP	−60 V ≤ V_{BP} ≤ +60 V; with respect to ground and V_{BAT}		−7.5	-	+7.5	mA
$I_{o(idle)BM}$	idle output current on pin BM	−60 V ≤ V_{BM} ≤ +60 V; with respect to ground and V_{BAT}		−7.5	-	+7.5	mA
$V_{o(idle)(dif)}$	differential idle output voltage		[2]	−25	0	+25	mV
$V_{OH(dif)}$	differential HIGH-level output voltage	4.75 V ≤ V_{CC} ≤ 5.25 V	[2]	900	-	2000	mV
		4.45 V ≤ V_{CC} ≤ 5.25 V	[2]	700	-	2000	mV
$V_{OL(dif)}$	differential LOW-level output voltage	4.75 V ≤ V_{CC} ≤ 5.25 V	[2]	−2000	-	−900	mV
		4.45 V ≤ V_{CC} ≤ 5.25 V	[2]	−2000	-	−700	mV
$V_{IH(dif)}$	differential HIGH-level input voltage	normal-power modes; −10 V ≤ V_{cm} ≤ +15 V; see Figure 10	[3] [4]	150	210	300	mV
$V_{IL(dif)}$	differential LOW-level input voltage	normal-power modes; −10 V ≤ V_{cm} ≤ +15 V; see Figure 10	[3] [4]	−300	−210	−150	mV
		low-power modes; see Figure 10	[4]	−400	−300	−100	mV
$\lvert\Delta V_{i(dif)(H-L)}\rvert$	differential input volt. diff. betw. HIGH- and LOW-levels (abs. value)	normal-power modes; V_{cm} = 2.5 V	[4]	−30	-	+30	mV
$\lvert V_{i(dif)det(act)}\rvert$	activity detection differential input voltage (absolute value)	normal-power modes		150	210	300	mV

Table 13. Static characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 4.45 V to 60 V; V_{CC} = 4.45 V to 5.25 V; V_{IO} = 2.55 V to 5.25 V; T_{vj} = −40 °C to +150 °C; C_{bus} = 100 pF; R_{bus} = 40 Ω to 55 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\lvert I_{O(sc)} \rvert$	short-circuit output current (absolute value)	on pin BP; $-5\ V \le V_{BP} \le +60\ V$ $R_{sc} \le 1\ \Omega$; $t_{sc} \ge 1500\ \mu s$	[5] [6]	-	-	72	mA
		on pin BP; $-5\ V \le V_{BP} \le +27\ V$ $R_{sc} \le 1\ \Omega$; $t_{sc} \ge 1500\ \mu s$	[5] [6]	-	-	60	mA
		on pin BM; $-5\ V \le V_{BM} \le +60\ V$ $R_{sc} \le 1\ \Omega$; $t_{sc} \ge 1500\ \mu s$	[5] [6]	-	-	72	mA
		on pin BM; $-5\ V \le V_{BM} \le +27\ V$; $R_{sc} \le 1\ \Omega$; $t_{sc} \ge 1500\ \mu s$	[5] [6]	-	-	60	mA
		on pins BP and BM; $R_{sc} \le 1\ \Omega$; $t_{sc} \ge 1500\ \mu s$; $V_{BP} = V_{BM}$	[5] [6]	-	-	60	mA
$R_{i(BP)}$	input resistance on pin BP	idle level; $R_{bus} = \infty\ \Omega$		10	18	40	kΩ
$R_{i(BM)}$	input resistance on pin BM	idle level; $R_{bus} = \infty\ \Omega$		10	18	40	kΩ
$R_{i(dif)(BP-BM)}$	differential input resistance between pin BP and pin BM	idle level; $R_{bus} = \infty\ \Omega$		20	36	80	kΩ
$I_{LI(BP)}$	input leakage current on pin BP	power off; $V_{BP} = V_{BM}$ = 5 V; all other pins connected to GND; GND connected to 0 V		−5	0	+5	µA
		loss of ground; $V_{BP} = V_{BM}$ = 0 V; all other pins connected to 16 V via 0 Ω	[1]	−1600		+1600	µA
$I_{LI(BM)}$	input leakage current on pin BM	power off; $V_{BP} = V_{BM}$ = 5 V; all other pins connected to GND; GND connected to 0 V		−5	0	+5	µA
		loss of ground; $V_{BP} = V_{BM}$ = 0 V; all other pins connected to 16 V via 0 Ω	[1]	−1600		+1600	µA
$V_{cm(bus)(DATA\_0)}$	DATA_0 bus common-mode voltage			$0.4V_{CC}$	$0.5V_{CC}$	$0.6V_{CC}$	V
$V_{cm(bus)(DATA\_1)}$	DATA_1 bus common-mode voltage			$0.4V_{CC}$	$0.5V_{CC}$	$0.6V_{CC}$	V
$\Delta V_{cm(bus)}$	bus common-mode voltage difference			−30	0	+30	mV
$C_{i(BP)}$	input capacitance on pin BP	with respect to all other pins at ground; V_{BP} = 100 mV; f = 5 MHz	[1]	-	8	15	pF
$C_{i(BM)}$	input capacitance on pin BM	with respect to all other pins at ground; V_{BM} = 100 mV; f = 5 MHz	[1]	-	8	15	pF

Table 13. Static characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 4.45 V to 60 V; V_{CC} = 4.45 V to 5.25 V; V_{IO} = 2.55 V to 5.25 V; T_{vj} = −40 °C to +150 °C; C_{bus} = 100 pF; R_{bus} = 40 Ω to 55 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{i(dif)(BP-BM)}$	differential input capacitance between pin BP and pin BM	with respect to all other pins at ground; $V_{(BM-BP)}$ = 100 mV; f = 5 MHz	[1]	-	2	5	pF
$Z_{o(eq)TX}$	transmitter equivalent output impedance	Normal mode; R_{bus} = 40 Ω or 100 Ω; C_{bus} = 100 pF	[1] [7]	10	-	600	Ω
Pin INH							
$V_{OH(INH)}$	HIGH-level output voltage on pin INH	I_{INH} = −0.2 mA		V_{BAT} − 0.8	V_{BAT} − 0.3	V_{BAT}	V
		I_{INH} = −1 mA; $V_{BAT} \geq$ 5.5 V		V_{BAT} − 4	-	V_{BAT}	V
$I_{L(INH)}$	leakage current on pin INH	Sleep mode		−5	0	+5	µA
$I_{OL(INH)}$	LOW-level output current on pin INH	V_{INH} = 0 V		−7	−4	−1	mA
Pin WAKE							
$V_{th(det)(WAKE)}$	detection threshold voltage on pin WAKE	low-power mode		2	-	3.75	V
V_{hys}	hysteresis voltage			0.3	-	1.2	V
I_{IL}	LOW-level input current	V_{WAKE} = 2 V for t > $t_{fltr(WAKE)}$		3	-	11	µA
		V_{WAKE} = 0 V		−2	-	−0.3	µA
I_{IH}	HIGH-level input current	V_{WAKE} = 3.75 V for t > $t_{fltr(WAKE)}$; 4.75 V ≤ V_{BAT} ≤ 60 V		−11	-	−3	µA
		V_{WAKE} = V_{BAT}		0.2	-	2	µA
Temperature protection							
$T_{j(warn)(medium)}$	medium warning junction temperature	V_{BAT} > 5.5 V		155	165	175	°C
$T_{j(dis)(high)}$	high disable junction temperature	V_{BAT} > 5.5 V		180	190	200	°C
Power-on reset							
$V_{th(det)POR}$	power-on reset detection threshold voltage	of internal digital circuitry		3.0	-	3.4	V
$V_{th(rec)POR}$	power-on reset recovery threshold voltage	of internal digital circuitry		3.1	-	3.5	V
$V_{hys(POR)}$	power-on reset hysteresis voltage	of internal digital circuitry		100	-	500	mV

[1] Not tested in production; guaranteed by design.

[2] Values also guaranteed when the signal on TXD is constant for between 100 ns and 4400 ns before the first edge.

[3] Activity detected previously.

[4] V_{cm} is the BP/BM common mode voltage.

[5] R_{sc} is the short-circuit resistance; voltage difference between bus pins BP and BM is 60 V max.

[6] t_{sc} is the minimum duration of the short circuit.

[7] $Z_{o(eq)TX} = 50\ \Omega \times (V_{bus(100)} - V_{bus(40)})/(2.5 \times V_{bus(40)} - V_{bus(100)})$ where:
- $V_{bus(100)}$ is the differential output voltage on a load of 100 Ω and 100 pF in parallel
- $V_{bus(40)}$ is the differential output voltage on a load of 40 Ω and 100 pF in parallel when driving a DATA_1.

10. Dynamic characteristics

Table 14. Dynamic characteristics

All parameters are guaranteed for V_{BAT} = 4.45 V to 60 V; V_{CC} = 4.45 V to 5.25 V; V_{IO} = 2.55 V to 5.25 V; T_{vj} = −40 °C to +150 °C; C_{bus} = 100 pF; R_{bus} = 40 Ω to 55 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pins BP and BM							
$t_{d(TXD-bus)}$	delay time from TXD to bus	Normal mode; see Figure 9	[1] [2]				
		DATA_0		-	-	50	ns
		DATA_1		-	-	50	ns
$\Delta t_{d(TXD-bus)}$	delay time difference from TXD to bus	Normal mode; between DATA_0 and DATA_1; see Figure 10	[1] [2] [3]	−4	-	+4	ns
$t_{d(bus-RXD)}$	delay time from bus to RXD	Normal mode; V_{cm} = 2.5 V; C_{RXD} = 25 pF; see Figure 10	[3]				
		DATA_0		-	-	75	ns
		DATA_1		-	-	75	ns
$\Delta t_{d(bus-RXD)}$	delay time difference from bus to RXD	Normal mode; V_{cm} = 2.5 V; C_{RXD} = 25 pF; between DATA_0 and DATA_1; see Figure 10	[3]	−5	-	+5	ns
$t_{d(TXEN-busidle)}$	delay time from TXEN to bus idle	Normal mode; see Figure 9		-	35	75	ns
$t_{d(TXEN-busact)}$	delay time from TXEN to bus active	Normal mode; see Figure 9		-	46	75	ns
$\Delta t_{d(TXEN-bus)}$	delay time difference from TXEN to bus	Normal mode; between TXEN-to-bus active and TXEN-to-bus idle; TXD LOW; see Figure 9		−50	-	+50	ns
$t_{d(BGE-busidle)}$	delay time from BGE to bus idle	Normal mode; see Figure 9		-	35	75	ns
$t_{d(BGE-busact)}$	delay time from BGE to bus active	Normal mode; see Figure 9		-	47	75	ns
$t_{d(TXENH-RXDH)}$	delay time from TXEN HIGH to RXD HIGH	Normal mode; TXD LOW		-	-	325	ns
Bus slope							
$t_{r(dif)(bus)}$	bus differential rise time	20 % to 80 %	[1]	6	-	18.75	ns
		DATA_0 to idle; −300 mV to −30 mV; Normal mode		-	-	30	ns
$t_{f(dif)(bus)}$	bus differential fall time	80 % to 20 %	[1]	6	-	18.75	ns
		idle to DATA_0; −30 mV to −300 mV; Normal mode		-	-	30	ns
		DATA_1 to idle; 300 mV to 30 mV; Normal mode		-	-	30	ns
$\Delta t_{(r-f)(dif)}$	difference between differential rise and fall time	80 % to 20 %		−3	-	+3	ns

Table 14. Dynamic characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 4.45 V to 60 V; V_{CC} = 4.45 V to 5.25 V; V_{IO} = 2.55 V to 5.25 V; T_{vj} = −40 °C to +150 °C; C_{bus} = 100 pF; R_{bus} = 40 Ω to 55 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pin RXD							
t_r	rise time	C_{RXD} = 15 pF; 20 % to 80 %		-	-	9	ns
		C_{RXD} = 25 pF; 20 % to 80 %		-	-	10.75	
t_f	fall time	C_{RXD} = 15 pF; 80 % to 20 %		-	-	9	ns
		C_{RXD} = 25 pF; 80 % to 20 %		-	-	10.75	
$t_{(r+f)}$	sum of rise and fall time	C_{RXD} = 15 pF; 20 % to 80 % and 80 % to 20 %		-	-	13	ns
		C_{RXD} = 25 pF; 20 % to 80 % and 80 % to 20 %		-	-	16.5	ns
		C_{RXD} = 10 pF load at end of 50 Ω µstrip with 1 ns delay; 20 % to 80 % and 80 % to 20 %; simulation only		-	-	16.5	ns
$\Delta t_{(r-f)}$	difference between rise and fall time	C_{RXD} = 15 pF; 20 % to 80 %		−5	-	+5	ns
		C_{RXD} = 25 pF; 20 % to 80 %		−5	-	+5	ns
		C_{RXD} = 10 pF load at end of 50 Ω µstrip with 1 ns delay; 20 % to 80 % and 80 % to 20 %; simulation only		−5	-	+5	ns
WAKE symbol detection							
$t_{det(wake)DATA\_0}$	DATA_0 wake-up detection time	Standby or Sleep mode; −10 V ≤ V_{cm} ≤ +15 V		1	-	4	µs
$t_{det(wake)idle}$	idle wake-up detection time			1	-	4	µs
$t_{det(wake)tot}$	total wake-up detection time			50	-	115	µs
$t_{sup(int)wake}$	wake-up interruption suppression time		[4]	130	-	1000	ns
Reaction time							
$t_{d(wakedet-INHH)}$	delay time from wake-up detection to INH HIGH	low-power mode; $R_{L(INH-GND)}$ = 100 kΩ; V_{INH} = 2 V		-	-	35	µs
$t_{d(event-ERRNL)}$	delay time from event detection to ERRN LOW	low-power mode		-	-	10	µs
$t_{d(wakedet-RXDL)}$	delay time from wake-up detection to RXD LOW	low-power mode		-	-	10	µs
$t_{d(STBNX-moch)}$	delay time from STBN changing to mode change			-	-	100	µs
$t_{d(ENX-moch)}$	delay time from EN changing to mode change			-	-	100	µs
Undervoltage detection							
$t_{det(uv)(VCC)}$	undervoltage detection time on pin V_{CC}	V_{CC} = 4.35 V		5	-	100	µs
$t_{to(uvd)(VCC)}$	undervoltage detection time-out time on pin V_{CC}			100	-	670	ms
$t_{rec(uv)(VCC)}$	undervoltage recovery time on pin V_{CC}	V_{CC} = 4.85 V		5	-	100	µs
$t_{to(uvr)(VCC)}$	undervoltage recovery time-out time on pin V_{CC}			1	-	5.2	ms

Table 14. Dynamic characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 4.45 V to 60 V; V_{CC} = 4.45 V to 5.25 V; V_{IO} = 2.55 V to 5.25 V; T_{vj} = −40 °C to +150 °C; C_{bus} = 100 pF; R_{bus} = 40 Ω to 55 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{det(uv)(VIO)}$	undervoltage detection time on pin V_{IO}	V_{IO} = 2.45 V	5	-	100	µs
$t_{to(uvd)(VIO)}$	undervoltage detection time-out time on pin V_{IO}		100	-	670	ms
$t_{rec(uv)(VIO)}$	undervoltage recovery time on pin V_{IO}	V_{IO} = 2.9 V	5	-	100	µs
$t_{to(uvr)(VIO)}$	undervoltage recovery time-out time on pin V_{IO}		1	-	5.2	ms
$t_{det(uv)(VBAT)}$	undervoltage detection time on pin V_{BAT}	V_{BAT} = 4.35 V	5	-	100	µs
$t_{rec(uv)(VBAT)}$	undervoltage recovery time on pin V_{BAT}	V_{BAT} = 4.85 V	5	-	100	µs
$t_{to(uvr)(VBAT)}$	undervoltage recovery time-out time on pin V_{BAT}		1	-	5.2	ms
Activity detection						
$t_{det(act)(bus)}$	activity detection time on bus pins	V_{dif}: 0 mV → 400 mV; V_{cm} = 2.5 V;	100	-	200	ns
$t_{det(idle)(bus)}$	idle detection time on bus pins	V_{dif}: 400 mV → 0 mV; V_{cm} = 2.5 V;	100	-	200	ns
$\Delta t_{det(act-idle)}$	difference between active and idle detection time	V_{cm} = 2.5 V	−50	-	+50	ns
Mode control pins						
$t_{d(STBN-RXD)}$	STBN to RXD delay time	STBN HIGH to RXD HIGH; remote or local wake-up source flag set	3	-	12	µs
$t_{fltr(STBN)}$	filter time on pin STBN	rising and falling edges	3	-	10	µs
$t_{d(STBN-stb)}$	delay time from STBN to standby mode	STBN LOW to Standby mode; Receive-only mode [5]	-	-	10	µs
$t_{h(gotosleep)}$	go-to-sleep hold time		20	35	50	µs
Status register						
$t_{det(EN)}$	detection time on pin EN	for mode control	5	-	20	µs
$T_{clk(EN)}$	clock period on pin EN	EN signal used as clock for reading status bits; see Figure 8	1	-	5	µs
$t_{d(EN-ERRN)}$	delay time from EN to ERRN	when reading status bits; see Figure 8	-	-	0.5	µs
Pin WAKE						
$t_{fltr(WAKE)}$	filter time on pin WAKE	low-power modes; falling edge on pin WAKE; 5.5 V ≤ V_{BAT} ≤ 27 V	2.9	-	100	µs
		low-power modes; falling edge on pin WAKE; 27 V ≤ V_{BAT} ≤ 60 V	2.9	-	175	µs

Table 14. Dynamic characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 4.45 V to 60 V; V_{CC} = 4.45 V to 5.25 V; V_{IO} = 2.55 V to 5.25 V; T_{vj} = −40 °C to +150 °C; C_{bus} = 100 pF; R_{bus} = 40 Ω to 55 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Miscellaneous							
$t_{detCL(TXEN)}$	TXEN clamp detection time			650	-	2600	µs
$t_{d(busact-RXDL)}$	delay time from bus active to RXD LOW	Normal mode; V_{cm} = 2.5 V; C_{RXD} = 25 pF; see Figure 9	[6] [7]	100	-	275	ns
$t_{d(busidle-RXDH)}$	delay time from bus idle to RXD HIGH	Normal mode; V_{cm} = 2.5 V; C_{RXD} = 25 pF; see Figure 9	[6] [8]	100	-	275	ns

[1] Values also guaranteed when the signal on TXD is constant for between 100 ns and 4400 ns before the first edge.

[2] Sum of rise and fall times on TXD (20 % to 80 % on V_{IO}) is 9 ns (max).

[3] Guaranteed for $V_{bus(dif)}$ = ±300 mV and $V_{bus(dif)}$ = ±150 mV; $V_{bus(dif)}$ is the differential bus voltage $V_{BP} - V_{BM}$.

[4] The minimum value is guaranteed when the phase that was interrupted was present continuously for at least 870 ns.

[5] Same parameter is guaranteed by design for the transition from Normal to Go-to-sleep mode.

[6] Not tested in production; guaranteed by design.

[7] $t_{d(busact-RXDL)} = t_{d(bus-RXD)} + t_{det(act)(bus)}$.

[8] $t_{d(busidle-RXDH)} = t_{d(bus-RXD)} + t_{det(idle)(bus)}$.

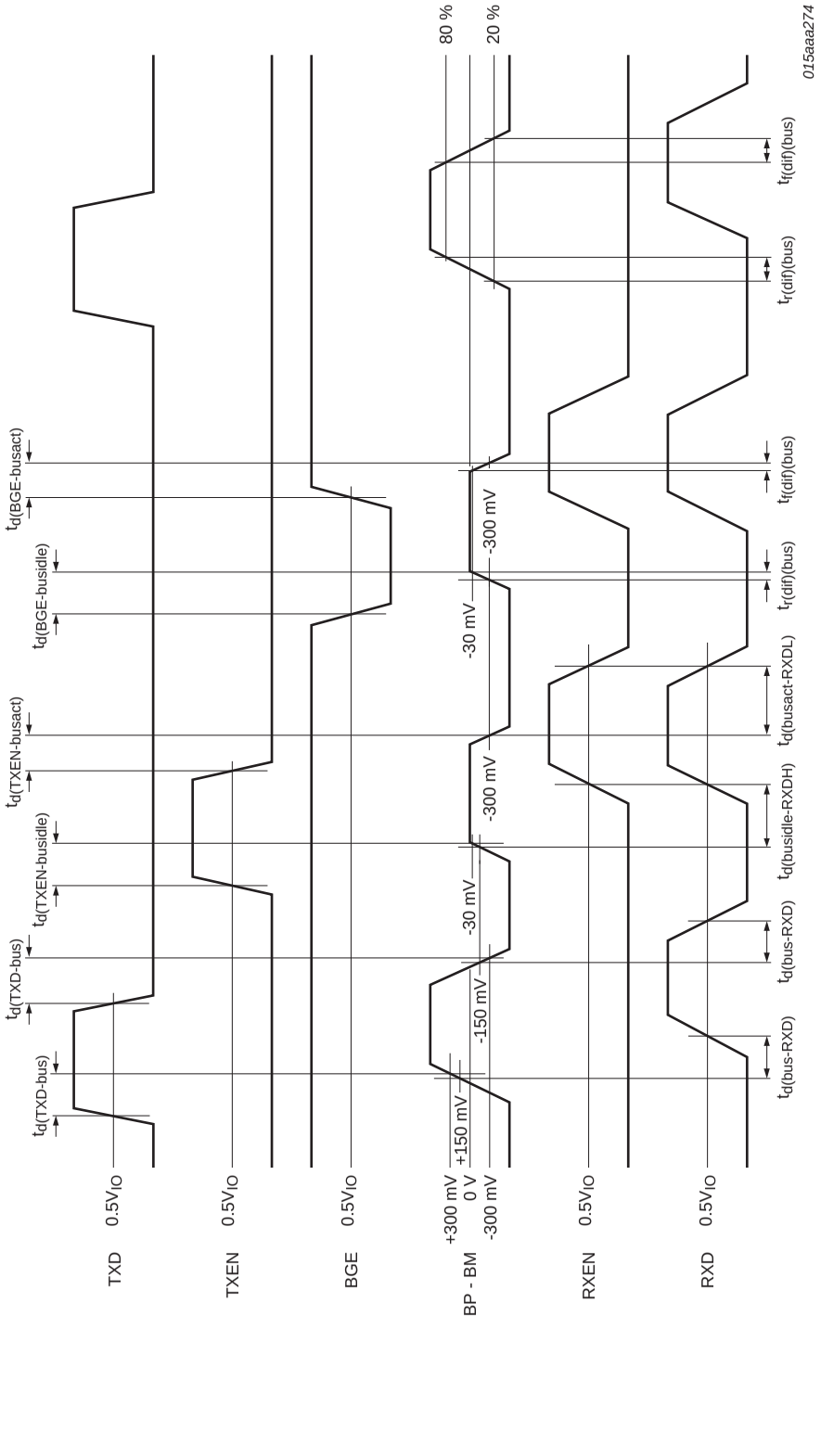
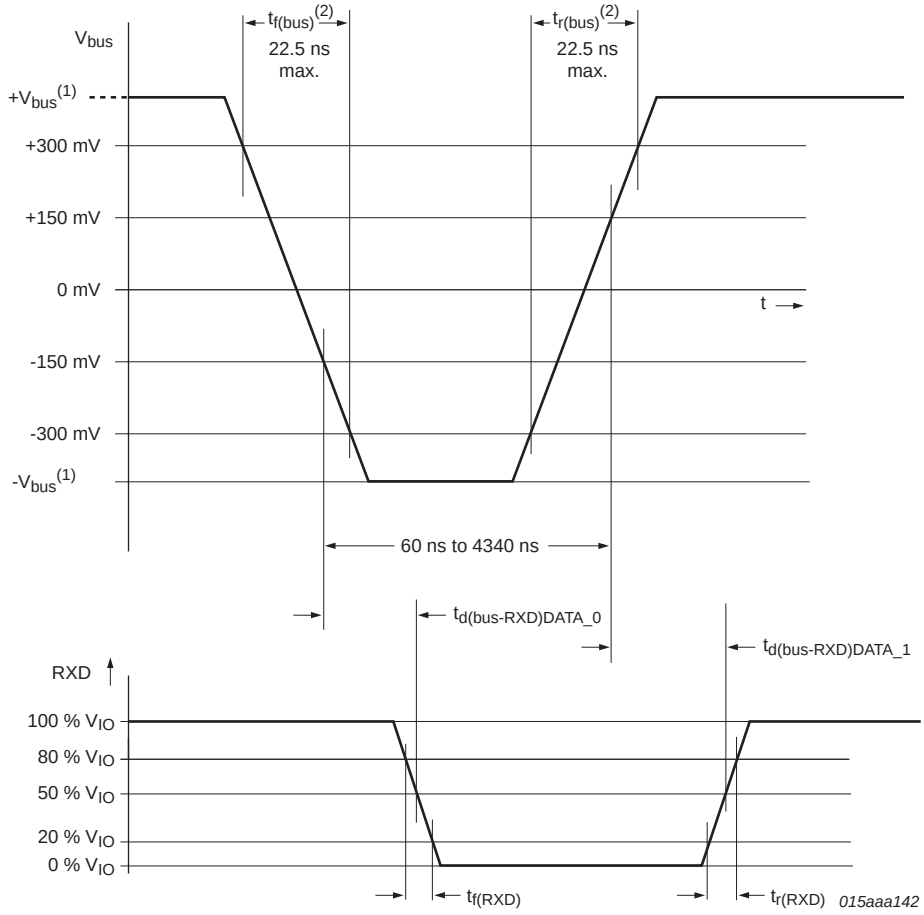


Fig 9. Detailed timing diagram



(1) $|V_{bus}|$ = 400 mV (min) to 3000 mV (max).

(2) $t_{r(bus)}$ and $t_{f(bus)}$ are defined for V_{bus} between −300 mV and +300 mV; $t_{r(bus)} = t_{f(bus)}$ = 22.5 ns for $|V_{bus}|$ = 400 mV to 800 mV; value will be lower for $|V_{bus}| > 800$ mV.

Fig 10. Normal receiver timing diagram

11. Test information

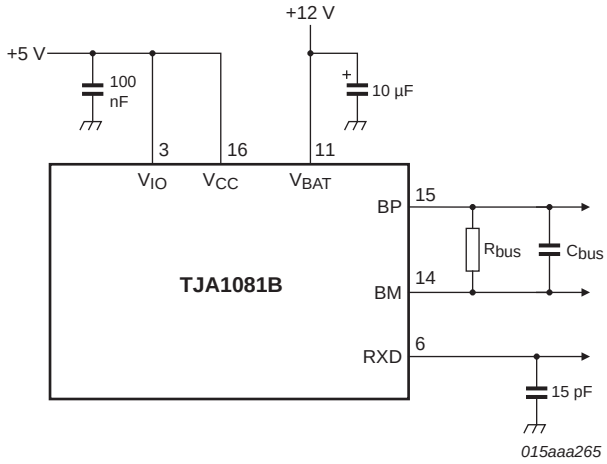
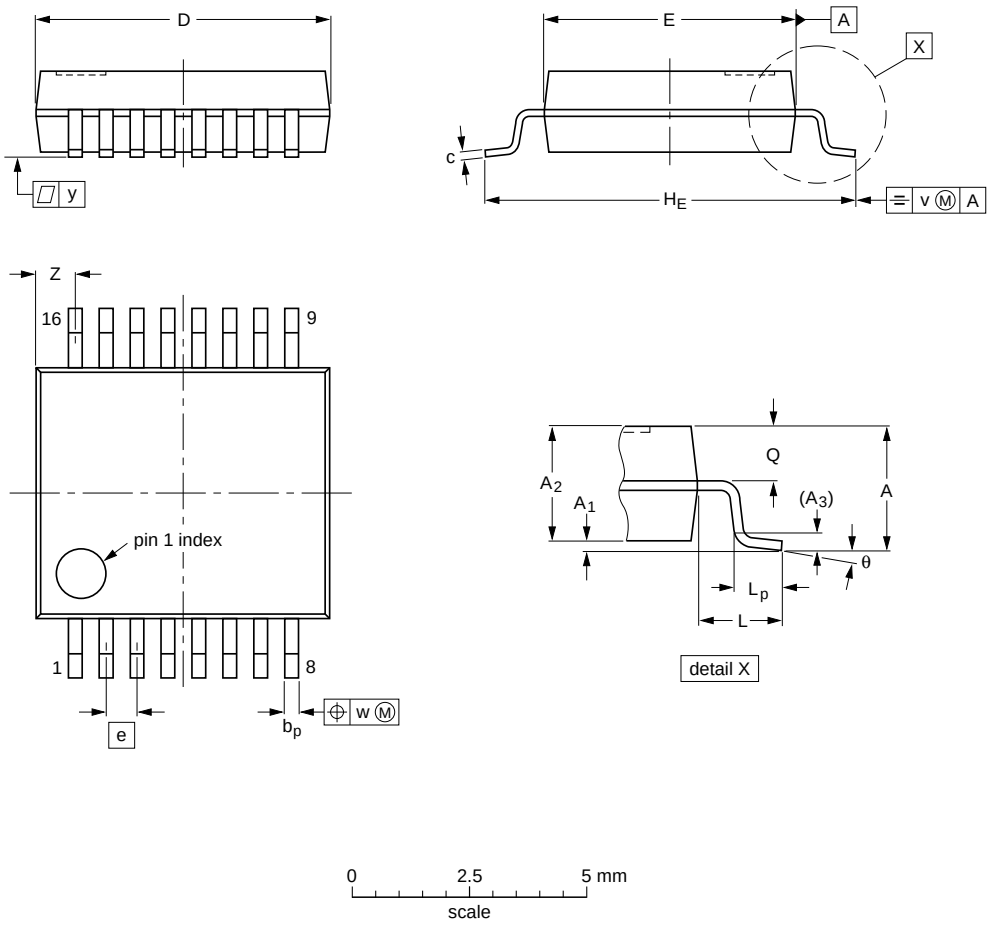


Fig 11. Test circuit for dynamic characteristics

12. Package outline

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT338-1 (SSOP16)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15 and 16

Table 15. SnPb eutectic process (from J-STD-020C)

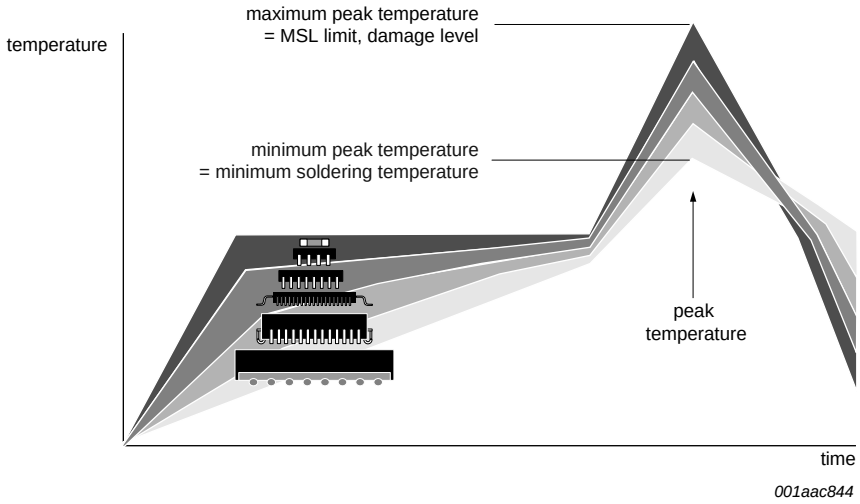
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 16. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Appendix: EPL 3.0.1 to TJA1081B parameter conversion

Table 17. EPL 3.0.1 to TJA1081B conversion

EPL 3.0.1				TJA1081B			
Symbol	**Min**	**Max**	**Unit**	**Symbol**	**Min**	**Max**	**Unit**
dBDRxAsym	-	5	ns	$\Delta t_{d(bus\text{-}RXD)}$	-	5	ns
dBDRx10	-	75	ns	$t_{d(bus\text{-}RXD)}$	-	75	ns
dBDRx01	-	75	ns	$t_{d(bus\text{-}RXD)}$	-	75	ns
dBDRxai	50	275	ns	$t_{d(busidle\text{-}RXDH)}$	100	275	ns
dBDRxia	100	325	ns	$t_{d(busact\text{-}RXDL)}$	100	275	ns
dBDTxAsym	-	4	ns	$\Delta t_{d(TXD\text{-}bus)}$	-	4	ns
dBDTx10	-	75	ns	$t_{d(TXD\text{-}bus)}$	-	50	ns
dBDTx01	-	75	ns	$t_{d(TXD\text{-}bus)}$	-	50	ns
dBDTxai	-	75	ns	$t_{d(TXEN\text{-}busidle)}$	-	75	ns
dBDTxia	-	75	ns	$t_{d(TXEN\text{-}busact)}$	-	75	ns
dBusTxai	-	30	ns	$t_{r(dif)(bus)(DATA\_0\text{-}idle)}$	-	30	ns
dBusTxia	-	30	ns	$t_{f(dif)(bus)(idle\text{-}DATA\_0)}$	-	30	ns
dBusTx01	6	18.75	ns	$t_{r(dif)(bus)}$	6	18.75	ns
dBusTx10	6	18.75	ns	$t_{f(dif)(bus)}$	6	18.75	ns
$uBDTx_{active}$	600	2000	mV	$V_{OH(dif)}$	900	2000	mV
$uBDTx_{idle}$	0	30	mV	$V_{O(idle)(dif)}$	–25	+25	mV
$uV_{DIG\text{-}OUT\text{-}HIGH}$	80	100	%	$V_{OH(RXD)}$	$V_{IO} - 0.4$	V_{IO}	V
$uV_{DIG\text{-}OUT\text{-}LOW}$	-	20	%	$V_{OL(RXD)}$	-	0.4	V
$uV_{DIG\text{-}IN\text{-}HIGH}$	-	70	%	$V_{IH(TXEN)}$	$0.7V_{IO}$	5.5	V
				$V_{IH(EN)}$	$0.7V_{IO}$	5.5	V
				$V_{IH(STBN)}$	$0.7V_{IO}$	5.5	V
				$V_{IH(BGE)}$	$0.7V_{IO}$	5.5	V
$uV_{DIG\text{-}IN\text{-}LOW}$	30	-	%	$V_{IL(TXEN)}$	–0.3	$0.3V_{IO}$	V
				$V_{IL(EN)}$	–0.3	$0.3V_{IO}$	V
				$V_{IL(STBN)}$	–0.3	$0.3V_{IO}$	V
				$V_{IL(BGE)}$	–0.3	$0.3V_{IO}$	V
uData0	–300	–150	mV	$V_{IL(dif)}$	–300	–150	mV
uData1	150	300	mV	$V_{IH(dif)}$	150	300	mV
uData1-|uData0|	–30	–30	mV	$\Delta V_{i(dif)(H\text{-}L)}$	–30	–30	mV
dBDActivityDetection	100	250	ns	$t_{det(act)(bus)}$	100	200	ns
dBDIdleDetection	50	200	ns	$t_{det(idle)(bus)}$	100	200	ns
R_{CM1}, R_{CM2}	10	40	kΩ	$R_{i(BP)}$, $R_{i(BM)}$	10	40	kΩ
uCM	–10	+15	V	V_{cm}[1]	–10	+15	V
$iBM_{GNDShortMax}$	-	60	mA	$\lvert I_{O(sc)(BM)} \rvert$	-	60	mA
$iBP_{GNDShortMax}$	-	60	mA	$\lvert I_{O(sc)(BP)} \rvert$	-	60	mA
$iBM_{BAT48ShortMax}$	-	72	mA	$\lvert I_{O(sc)(BM)} \rvert$	-	72	mA
$iBP_{BAT48ShortMax}$	-	72	mA	$\lvert I_{O(sc)(BP)} \rvert$	-	72	mA
$iBM_{BAT27ShortMax}$	-	60	mA	$\lvert I_{O(sc)(BM)} \rvert$	-	60	mA

Table 17. EPL 3.0.1 to TJA1081B conversion *…continued*

EPL 3.0.1				TJA1081B			
Symbol	**Min**	**Max**	**Unit**	**Symbol**	**Min**	**Max**	**Unit**
$iBP_{BAT27ShortMax}$	-	60	mA	$\lvert I_{O(sc)(BP)}\rvert$	-	60	mA
uBias - Non-Low-Power	1800	3200	mV	$V_{o(idle)(BP)}$, $V_{o(idle)(BM)}$[2]	1800	3150	mV
uBias - Low-Power	–200	+200	mV	$V_{o(idle)(BP)}$, $V_{o(idle)(BM)}$[3]	–0.1	+0.1	V
dBDWakePulseFilter	1	500	µs	$t_{fltr(WAKE)}$	2.9	100	µs
$dWU_{0Detect}$	1	4	µs	$t_{det(wake)DATA\_0}$	1	4	µs
$dWU_{IdleDetect}$	1	4	µs	$t_{det(wake)idle}$	1	4	µs
$dWU_{Timeout}$	48	140	µs	$t_{det(wake)tot}$	50	115	µs
$uV_{BAT\text{-}WAKE}$ (V_{CC} implemented)	-	7	V	V_{BAT}	4.75	60	V
$uBDUVV_{BAT}$	4	5.5	V	$V_{uvd(VBAT)}$	4.45	4.715	V
$uBDUVV_{CC}$	4	-	V	$V_{uvd(VCC)}$	4.45	4.72	V
$dBDUVV_{CC}$	-	1000	ms	$t_{det(uv)(VCC)}$	5	100	µs
				$t_{to(uvd)(VCC)}$	100	670	ms
iBP_{Leak}	-	25	µA	$I_{LI(BP)}$	–5	+5	µA
iBM_{Leak}	-	25	µA	$I_{LI(BM)}$	–5	+5	µA
Functional class: BD voltage regulator control				implemented; see Section 2.5			
Functional class: Bus Driver logic level adaptation				implemented; see Section 2.5			
Functional class: Bus Driver - Bus guardian interface				implemented; see Section 2.5			
Device qualification according to AEC-Q100 (Rev. F)				see Section 2.1			
T_{AMB_Class1}	–40	+125	°C	T_{amb}	–40	+125	°C
dBDTxDM	–50	+50	ns	$\Delta t_{d(TXEN\text{-}bus)}$	–50	+50	µS
$iBM_{\text{-}5VshortMax}$	-	60	mA	$\lvert I_{O(sc)(BM)}$	-	60	mA
$iBP_{\text{-}5VshortMax}$	-	60	mA	$\lvert I_{O(sc)(BP)}$	-	60	mA
$iBM_{BPShortMax}$	-	60	mA	$\lvert I_{O(sc)(BP\text{-}BM)}\rvert$	-	60	mA
$iBP_{BMShortMax}$	-	60	mA	$\lvert I_{O(sc)(BM\text{-}BP)}\rvert$	-	60	mA
$iBM_{BAT60ShortMax}$	-	90	mA	$\lvert I_{O(sc)(BM)}\rvert$	-	72	mA
$iBP_{BAT60ShortMax}$	-	90	mA	$\lvert I_{O(sc)(BP)}\rvert$	-	72	mA
$dBDUVV_{BAT}$	-	1000	ms	$t_{det(uv)(VBAT)}$	5	100	µs
uUV_{IO}	2	-	V	$V_{uvd(VIO)}$	2.55	2.765	V
$dBDUVV_{IO}$	-	1000	ms	$t_{det(uv)(VIO)}$	5	100	ms
				$t_{to(uvd)(VIO)}$	100	670	µs
$dBDWakeupReaction_{local}$	-	100	µs	$t_{d(wakedet\text{-}INHH)}$	-	35	µs
				$t_{d(event\text{-}ERRNL)}$	-	10	µs
				$t_{d(wakedet\text{-}RXDL)}$	-	10	µs
$dBDWakeupReaction_{remote}$	-	100	µs	$t_{d(wakedet\text{-}INHH)}$	-	35	µs
				$t_{d(wake\text{-}ERRN)}$	-	10	µs
				$t_{d(wakedet\text{-}RXDL)}$	-	10	µs
dBDTxActiveMax	650	2600	µs	$t_{detCL(TXEN)}$	650	2600	µs
dBDModeChange	-	100	µs	$t_{d(STBNX\text{-}moch)}$	-	100	µs
				$t_{d(ENX\text{-}moch)}$	-	100	µs
$dReactionTime_{ERRN}$	-	100	µs	$t_{d(event\text{-}ERRNL)}$	-	10	µs

Table 17. EPL 3.0.1 to TJA1081B conversion *…continued*

EPL 3.0.1				TJA1081B			
Symbol	**Min**	**Max**	**Unit**	**Symbol**	**Min**	**Max**	**Unit**
$uINH1_{Not\_Sleep}$	uVBAT – 1 V	-	V	$V_{OH(INH)}$	V_{BAT} – 0.8	V_{BAT}	V
$iINH1_{Leak}$	-	10	µA	$I_{L(INH)}$	–5	+5	µA
uData0_LP	–400	–100	mV	$V_{IL(dif)}$ (pins BP and BM)	–400	–100	mV
$dWU_{Interrupt}$	0.13	1	µs	$t_{sup(int)wake}$	130	1000	ns
uBDLogic_1	-	60	%	$V_{IH(TXD)}$	$0.6V_{IO}$	V_{IO} + 0.3 V	V
uBDLogic_0	40	-	%	$V_{IL(TXD)}$	–0.3	$0.4V_{IO}$	V
$dBDRV_{CC}$	-	10	ms	$t_{rec(uv)(VCC)}$	5	100	µs
				$t_{to(uvr)(VCC)}$	1	5.2	ms
$dBDRV_{BAT}$	-	10	ms	$t_{rec(uv)(VBAT)}$	5	100	µs
				$t_{to(uvr)(VBAT)}$	1	5.2	ms
$dBDRV_{IO}$	-	10	ms	$t_{rec(uv)(VIO)}$	5	100	µs
				$t_{to(uvr)(VIO)}$	1	5.2	ms
$iBP_{LeakGND}$	-	1600	µA	$I_{LI(BP)}$	–1600	+1600	µA
$iBM_{LeakGND}$	-	1600	µA	$I_{LI(BM)}$	–1600	+1600	µA
Functional class: Bus Driver Remote Wakeup				implemented; see Section 2.5			
Functional class: Increased Voltage Amplitude Transmitter				implemented; see Section 2.5			
$uESD_{EXT}$	6	-	kV	$\|V_{ESD}\|$: HBM on pins BP and BM to GND	8	-	kV
				$\|V_{ESD}\|$: HBM on pins V_{BAT} and WAKE to GND	6	-	kV
$uESD_{INT}$	2	-	kV	$\|V_{ESD}\|$ (HBM on any other pin)	4	-	kV
$uESD_{IEC}$	6	-	kV	IEC61000-4-2 on pins BP, BM, V_{BAT} and WAKE	6	-	kV
$dBDRxD_{R15}$ + $dBDRxD_{F15}$	-	13	ns	$t_{(r+f)}$ (pin RXD; 15 pF load)	-	13	ns
$\|dBDRxD_{R15} - dBDRxD_{F15}\|$	-	5	ns	$\|\Delta t_{(r-f)}\|$ (pin RXD)	-	5	ns
C_BDTxD	-	10	pF	C_I (pin TXD)	-	10	pF
dBDTxRxai	-	325	ns	$t_{d(TXENH-RXDH)}$	-	325	ns
$uV_{DIG-OUT-UV}$	-	500	mV	$V_{O(ERRN)}$; with $V_{IO} < V_{uvd(VIO)}$	-	500	mV
				$V_{O(RXD)}$; with $V_{IO} < V_{uvd(VIO)}$	-	500	mV
				$V_{O(RXEN)}$; with $V_{IO} < V_{uvd(VIO)}$	-	500	mV
valid operating modes when $V_{BAT} \geq$ 5.5 V; V_{CC} = nominal (if implemented)				Normal, Receive only, Standby, Sleep			
valid operating modes when $V_{BAT} \geq$ 7 V; V_{CC} = nominal				Normal, Receive only, Standby, Sleep			
$uV_{DIG-OUT-OFF}$	product specific			$V_{O(ERRN)}$[4]	-	0.5	V
				$V_{O(RXD)}$[4]	V_{IO} – 0.5	V_{IO}	V
				$V_{O(RXEN)}$[4]	V_{IO} – 0.5	V_{IO}	V
$R_{BDTransmitter}$	product-specific			$Z_{o(eq)TX}$	10	600	Ω
RxD signal sum of rise and fall time at TP4_CC	-	16.5	ns	$t_{(r+f)(RXD)}$ (10 pF load on 50 Ω µstrip; simulated)	-	16.5	ns
$uV_{BAT-WAKE}$ (no V_{CC})	-	5.5	V	V_{BAT} (operating range)	4.75	60	V

Table 17. EPL 3.0.1 to TJA1081B conversion *…continued*

EPL 3.0.1				TJA1081B			
Symbol	**Min**	**Max**	**Unit**	**Symbol**	**Min**	**Max**	**Unit**
$dBDRxD_{R25} + dBDRxD_{F25}$	-	16.5	ns	$t_{(r+f)(RXD)}$ (25 pF load)	-	16.5	ns
$\lvert dBDRxD_{R25} - dBDRxD_{F25}\rvert$	-	5	ns	$\Delta t_{(r-f)(RXD)}$	–5	+5	ns
dBusTxDif	-	3	ns	$\Delta t_{(r-f)(dif)}$ (on bus)	–3	+3	ns
RxD signal difference of rise and fall time at TP4_CC	-	5	ns	$\lvert\Delta t_{(r-f)(RXD)}\rvert$ (10 pF load on 50 Ω µstrip; simulated)	-	5	ns

[1] V_{cm} is the BP/BM common mode voltage ($V_{BP} + V_{BM}/2$) and is specified in conditions column for $V_{IH(dif)}$ and $V_{IH(dif)}$ for pins BP and BM; see Table 13. V_{cm} is tested on a receiving bus driver with a transmitting bus driver that has a ground offset voltage in the range –12.5 V to +12.5 V and that transmits a 50/50 pattern.

[2] Min: $V_{o(idle)(BP)} = V_{o(idle)(BM)} = 0.4V_{CC} = 0.4 \times 4.5$ V = 1800 mV; max value: $V_{o(idle)(BP)} = V_{o(idle)(BM)} = 0.6V_{CC} = 0.6 \times 5.25$ V = 3150 mV; the nominal voltage is 2500 mV.

[3] The nominal voltage is 0 mV.

[4] Power off.

15. Abbreviations

Table 18. Abbreviations

Abbreviation	Description
BSS	Byte Start Sequence
CDM	Charged Device Model
ECU	Electronic Control Unit
EMC	ElectroMagnetic Compatibility
EME	ElectroMagnetic Emission
EMI	ElectroMagnetic Immunity
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TSS	Transmission Start Sequence

16. References

[1] **EPL —** FlexRay Communications System Electrical Physical Layer Specification Version 3.0.1, FlexRay Consortium

[2] **TJA1081 —** FlexRay transceiver data sheet, www.nxp.com

[3] **TJA1080A —** FlexRay transceiver data sheet, www.nxp.com

17. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1081B v.1	20120604	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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