ISL97656

Step-Up Regulator with 4A Integrated Switch

FN6439
Rev 6.00
July 19, 2012

The ISL97656 is a high frequency, high efficiency current mode control non-synchronous step-up voltage regulator operated at constant PMW switching frequency. It has an internal 4.0A, 120mΩ Low side MOSFET and can deliver high output current and efficiency over 90%. The selectable 640kHz and 1.22MHz switching frequency allows use of smaller inductor and faster transient response. An external compensation pin gives the user flexibility in setting frequency compensation allowing the use of low ESR ceramic output capacitors.

When in shut down mode, ISL97656 draws current <1µA and can operate at as low as 2.2V input. These features along with higher switching frequency allows use of tiny external components and makes it an ideal device for portable equipment and TFT-LCD displays.

The ISL97656 is available in a 10 Ld TDFN package with a maximum height of 1.1mm. The device is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL97656IRTZ	656Z	10 Ld TDFN	L10.3x3B

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL97656. For more information on MSL please see techbrief TB363.

Features

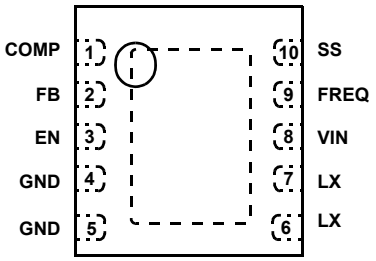
- 4.0A, Low $r_{DS(ON)}$ Integrated Low Side MOSFET
- +2.2V to +6.0V Operating Input Voltage Range
- +1.1*VIN to +24V Output Voltage Range
- 640kHz or 1.22MHz Switching Frequency
- Higher Efficiency and Better Thermal Performance
- Adjustable Soft-Start
- Internal Thermal Protection
- 0.8mm Maximum Height 10 Ld TDFN Package
- Pb-Free (RoHS Compliant)
- Halogen Free

Applications

- Portable Equipment, Digital Cameras
- TFT-LCD Displays, DSL Modems
- PCMCIA Cards, GSM/CDMA Phones

Pin Configuration

ISL97656
(10 LD TDFN)
TOP VIEW



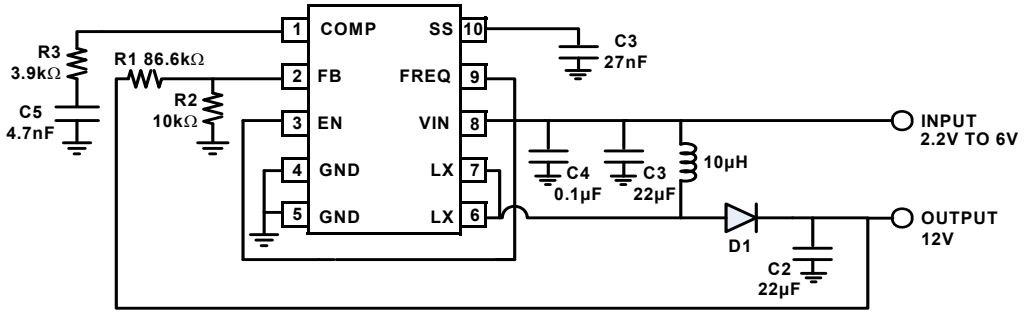


FIGURE 1. TYPICAL APPLICATION CIRCUIT

Absolute Maximum Ratings (T_A = +25°C)

Temperature Under Bias . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Terminal Voltage with Respect to GND:
VIN to GND 6.5V
LX to GND 26V
COMP, FB, EN, SS, FREQ to GND . . . . . -0.3V to (VIN +0.3V)
Maximum Continuous Junction Temperature . . . . . +135°C
ESD Rating (JEDEC)
Human Body Model 2kV
Machine Model 200V
Charged Device Model 1.2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld TDFN Package (Notes 4, 5)	53	3

Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

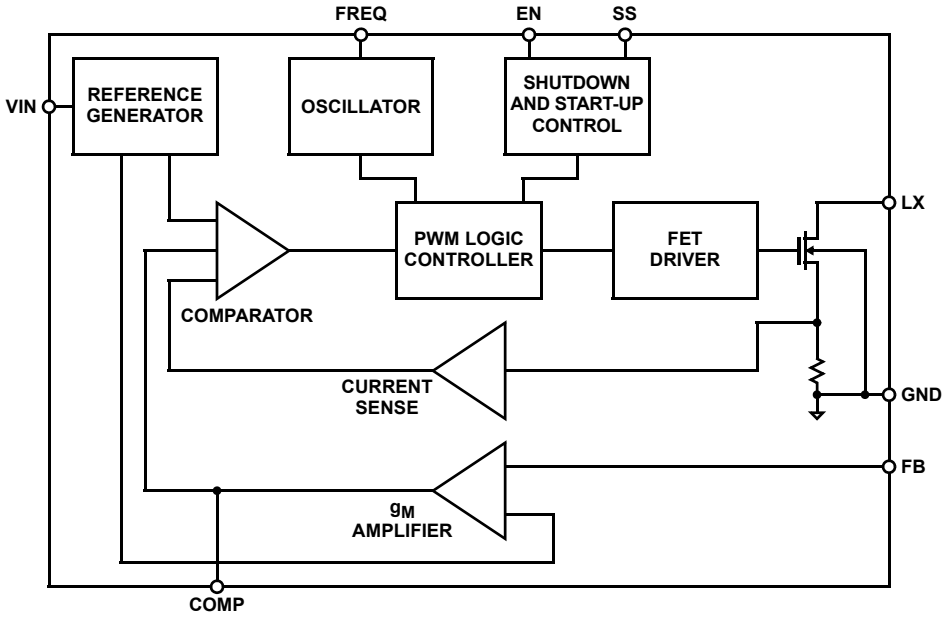
V_{IN} = 3V, V_{OUT} = 12V, I_{OUT} = 0mA, FREQ = GND, T_A = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$I_{DD-SHDN}$	Shutdown Supply Current	EN = 0V		0.1	**5**	µA
$I_{DD-STDBY}$	Standby Supply Current	EN = VIN, FB = 1.3V		0.7		mA
$I_{DD-ACTIVE}$	Active Supply Current	EN = VIN, FB = 1.0V		3	5	mA
V_{FB}	Feedback Voltage		**1.22**	1.24	**1.26**	V
I_{DD-FB}	Feedback Input Bias Current			0.01	**0.5**	µA
VIN	Input Voltage Range		**2.2**		**6.0**	V
D_{MAX} - 640kHz	Maximum Duty Cycle	FREQ = 0V	**85**	92		%
D_{MAX} - 1.2MHz	Maximum Duty Cycle	FREQ = VIN	**85**	90		%
I_{LIM}	Current Limit - Max Peak Input Current		**3.8**	4.0	**5.1**	A
I_{EN}	EN pin Input Bias Current	EN = 0V		0.01	**0.5**	µA
$r_{DS(ON)}$	Switch ON Resistance	VIN = 2.7V, I_{LX} = 1A		0.12		Ω
$I_{LX-LEAK}$	Switch Leakage Current	VSW = 26V		0.01	3	µA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	2.2V < V_{IN} < 5.5V, V_{OUT} = 12V		0.2		%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = 3.3V, V_{OUT} = 12V, I_O = 30mA to 200mA		0.3		%
F_{OSC1}	Switching Frequency Accuracy	FREQ = 0V	**500**	640	**740**	kHz
F_{OSC2}	Switching Frequency Accuracy	FREQ = VIN	**1000**	1220	**1500**	kHz
V_{IL}	EN, FREQ pin Input Low Level				**0.5**	V
V_{IH}	EN, FREQ pin Input High Level		**1.5**			V
g_M	Error Amp Tranconductance		**70**	130	**250**	µA/V
VIN_{UVLO}	VIN UVLO Threshold rising		**2.00**	2.10	**2.20**	V
$VIN_{UVLO-HYST}$	VIN UVLO Hysteresis			50		mV
I_{SS}	Soft-Start Charge Current		**2.5**	4.5	**7.5**	µA
T_{OTP}	Over-Temperature Protection			150		°C

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Block Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	COMP	Compensation pin. Output of the internal error amplifier. Capacitor and resistor from COMP pin to ground.
2	FB	Voltage feedback pin. Internal reference is 1.24V nominal. Connect a resistor divider from V_{OUT}. $V_{OUT} = 1.24V (1 + R_1/R_2)$. See “Typical Application Circuit” on page 1.
3	EN	Enable control pin. Pull the pin high to turn the device ON.
4, 5	GND	Power Ground.
6, 7	LX	Power switch pin. Connected to the drain of the internal power MOSFET.
8	VIN	Analog power supply input pin.
9	FREQ	Frequency select pin. When FREQ pin is set low, switching frequency is set to 640kHz when set high switching frequency is set to 1.22MHz.
10	SS	Soft-start control pin. Connect a capacitor to control the converter output slew rate.

Performance Curves

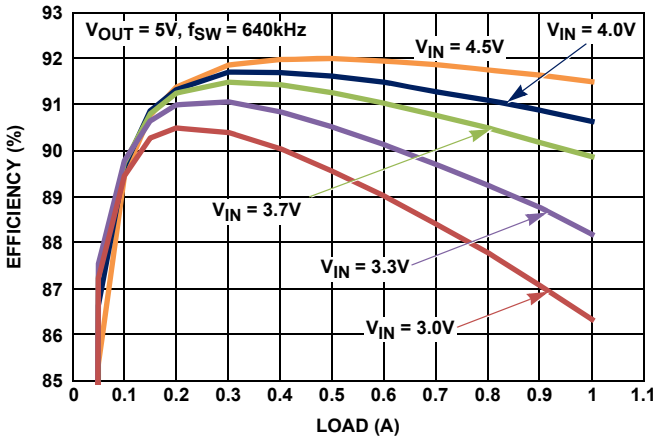


FIGURE 2. V_{OUT} = 5V EFFICIENCY

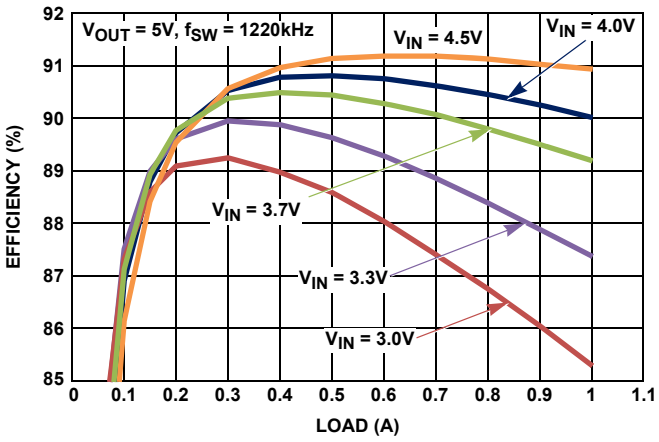


FIGURE 3. V_{OUT} = 5V EFFICIENCY

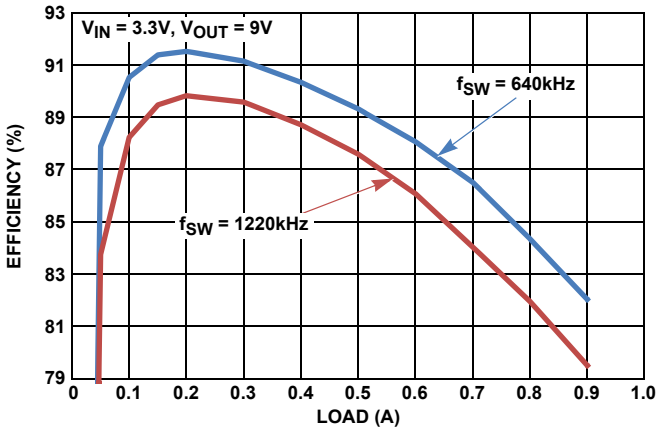


FIGURE 4. V_{OUT} = 9V EFFICIENCY

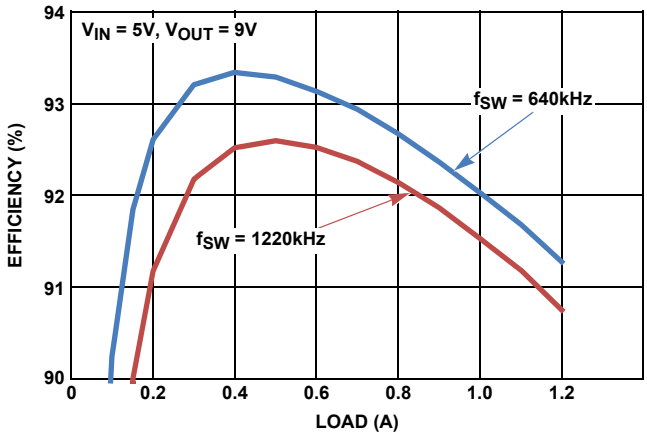


FIGURE 5. V_{OUT} = 9V EFFICIENCY

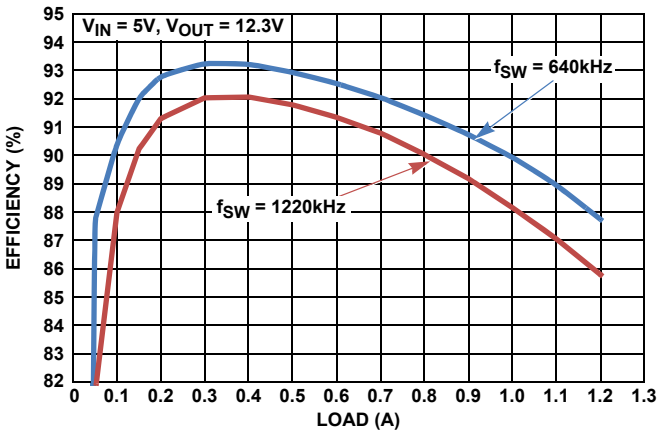


FIGURE 6. V_{OUT} = 12.3V EFFICIENCY

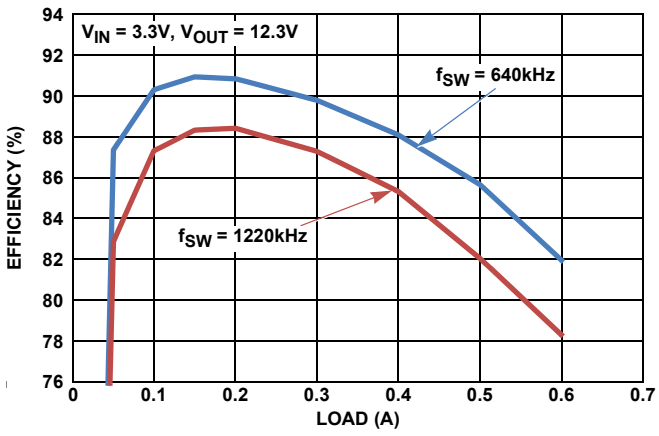


FIGURE 7. V_{OUT} = 12.3V EFFICIENCY

Performance Curves (Continued)

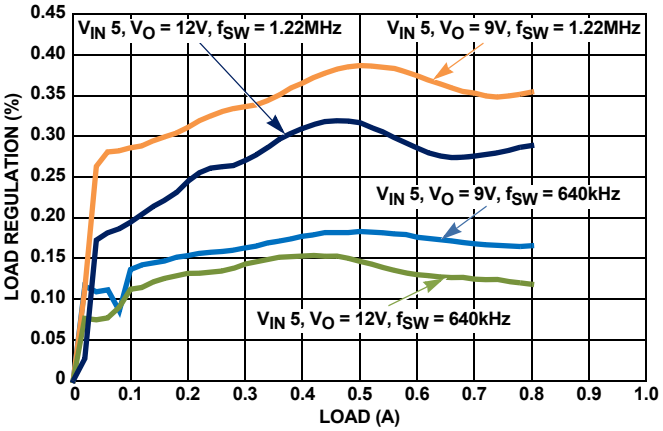


FIGURE 8. V_{IN} = 5V, LOAD REGULATION

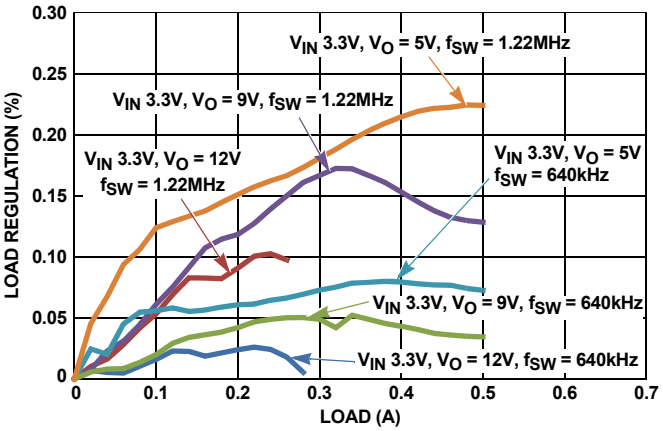


FIGURE 9. V_{IN} = 3.3V, LOAD REGULATION

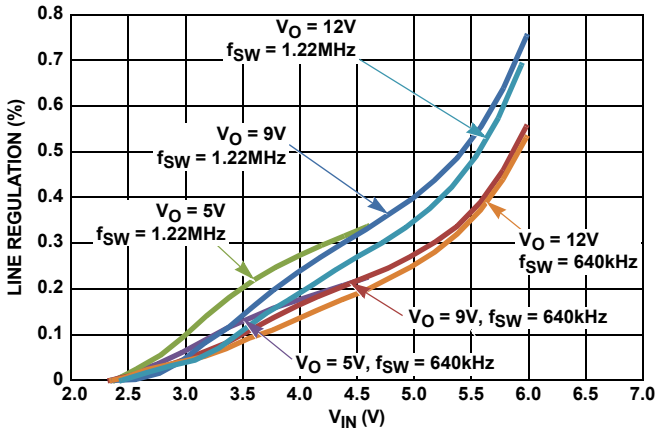


FIGURE 10. LINE REGULATION

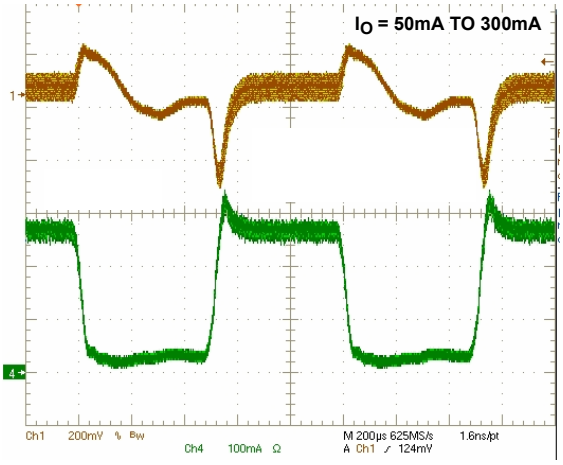


FIGURE 11. V_{IN} = 3.3V, V_O = 12V, f_{SW} = 640kHz, TRANSIENT RESPONSE

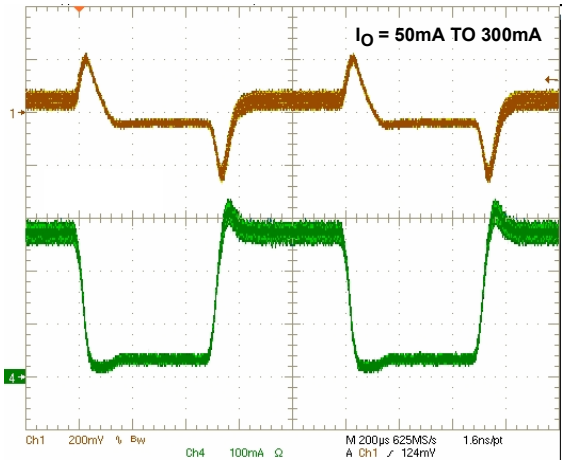


FIGURE 12. V_{IN} = 3.3V, V_O = 12V, f_{SW} = 1.22MHz, TRANSIENT RESPONSE

Applications Information

The ISL97656 is a high frequency, high efficiency boost regulator operated at constant frequency PWM mode. The boost converter stores energy from an input voltage source and delivers higher output voltage. The input voltage range is 2.2V to 6.0V and the output voltage range is 5V to 25V. The switching frequency can be selected between 640kHz and 1.22MHz. The higher switching frequency allows use of smaller inductors and faster transient response. An external compensation pin gives the user greater flexibility in setting output transient response and tighter load regulation. The converter soft-start characteristic can be controlled by the external C_{SS} capacitor. The EN pin allows the user to shut down the device.

Boost Converter Operations

Figure 13 shows a boost converter with all the key components. In steady state and continuous conduction mode, the boost converter operates in two cycles. During the first cycle, as shown in Figure 14, the internal power FET turns on and the Schottky diode is reverse biased and cuts off the current flow to the output. The output current is supplied from the output capacitor. The voltage across the inductor is V_{IN} and the inductor current ramps up with a rate of V_{IN}/L, where L is the inductance. The inductor is magnetized and energy is stored in the inductor. The change in inductor current is shown in Equation 1:

$$\Delta I_{L1} = \Delta T1 \times \frac{V_{IN}}{L}$$

$$\Delta T1 = \frac{D}{f_{SW}}$$

$$D = \text{Duty Cycle}$$

$$\Delta V_O = \frac{I_{OUT}}{C_{OUT}} \times \Delta T_1 \quad \text{(EQ. 1)}$$

During the second cycle, the power FET turns off and the Schottky diode is forward biased, (see Figure 15). The energy stored in the inductor is supplied to the output. This energy is used to charge the output capacitor and supply output current. In this cycle switching node (LX) is held to V_{OUT} + Schottky diode drop. Voltage drop across the inductor is V_{IN} - V_{OUT} (ignoring diode drop across Schottky diode). The change in inductor current during the second cycle is shown in Equation 2:

$$\Delta I_L = \Delta T2 \times \frac{V_{IN} - V_{OUT}}{L}$$

$$\Delta T2 = \frac{1 - D}{f_{SW}} \quad \text{(EQ. 2)}$$

In steady state operation, the change in the inductor current must be equal as shown in Equation 3.

$$\Delta I1 + \Delta I2 = 0$$

$$\frac{D}{f_{SW}} \times \frac{V_{IN}}{L} + \frac{1 - D}{f_{SW}} \times \frac{V_{IN} - V_{OUT}}{L} = 0$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D} \quad \text{(EQ. 3)}$$

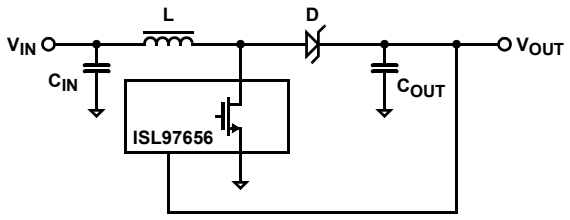


FIGURE 13. BOOST CONVERTER

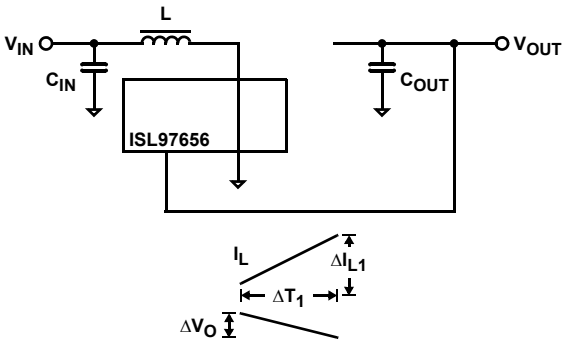


FIGURE 14. BOOST CONVERTER - CYCLE 1, POWER SWITCH CLOSED

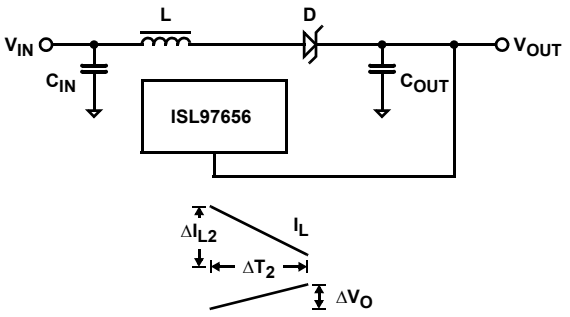


FIGURE 15. BOOST CONVERTER - CYCLE 2, POWER SWITCH OPEN

Output Voltage

An external feedback resistor divider is required to divide the output voltage down to the nominal 1.24V reference voltage. The current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network less than 100k is recommended. The boost converter output voltage is determined by the relationship as shown in Equation 4. The nominal VFB voltage is 1.24V.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 4)}$$

Inductor Selection

The inductor selection determines the output ripple voltage, transient response, output current capability and efficiency. Its selection depends on the input voltage, output voltage, switching frequency and maximum output current. For most applications, the inductance should be in the range of 2µH to 33µH. The inductor maximum DC current specification must be greater than the peak inductor current required by the regulator. The peak inductor current can be calculated using Equation 5:

$$I_{L(PEAK)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} + 1/2 \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times V_{OUT} \times FREQ} \quad \text{(EQ. 5)}$$

Output Capacitor

Low ESR capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors (X5R and X7R) are preferred for the output capacitors because of their lower ESR and small packages. Tantalum capacitors with higher ESR can also be used. The output ripple can be calculated using Equation 6:

$$\Delta V_O = \frac{I_{OUT} \times D}{f_{SW} \times C_O} + I_{OUT} \times ESR \quad \text{(EQ. 6)}$$

For noise sensitive applications, a 0.1µF placed in parallel with the larger output capacitor is recommended to reduce the switching noise coupled from the LX switching node.

Schottky Diode

In selecting the Schottky diode, the reverse break-down voltage, forward current and forward voltage drop must be considered for optimum converter performance. The diode must be rated to handle 4.0A, the current limit of the ISL97656. The breakdown voltage must exceed the maximum output voltage. Low forward voltage drop, low leakage current, and fast reverse recovery will help the converter to achieve the maximum efficiency.

Input Capacitor

The value of the input capacitor depends on the input and the output voltages, maximum output current, inductor value and maximum permissible noise fed back in the input line. For most applications, a minimum 10µF is required. For applications that run close to the maximum output current limit, an input capacitor in the range of 22µF to 47µF is recommended.

The ISL97656 is powered from the VIN. A High frequency 0.1µF bypass capacitor is recommended to be close to the VIN pin to reduce supply line noise and ensure stable operation.

Loop Compensation

The ISL97656 incorporates a transconductance amplifier in its feedback path to allow the user some adjustment on the transient response and better regulation. The ISL97656 uses current mode control architecture, which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation. The slow voltage loop must be compensated for stable operation. The compensation network is a series RC network from the COMP pin to ground. The resistor sets the high frequency integrator gain for fast transient response and the capacitor sets the integrator zero to ensure loop stability. For most applications, the compensation resistor in the range of 0k to 2.0k and the compensation capacitor in the range of 3nF to 10nF.

Soft-Start

The regulator goes through the soft-start sequence after EN is pulled high. The soft-start is provided by an internal 4.5µA current source. This internal current source is used to charge the external C_{SS} capacitor. The peak MOSFET current is limited by the voltage on the capacitor. As the voltage at the C_{SS} capacitor increases, this results in ramping up of the current limit from 0A to full scale. This in turn controls the rising rate of the output voltage.

Frequency Selection

The ISL97656 switching frequency can be user selectable. The ISL97656 operates at either constant 640KHz or 1.22MHz switching frequency. Connecting the FREQ pin to ground sets the PWM switching frequency to 640kHz. When connecting FREQ high or V_{IN}, the switching frequency is set to 1.22MHz.

Shutdown Control

When the EN pin is pulled low, the ISL97656 is in shutdown mode, reducing the supply current to <1µA.

Maximum Output Current

The MOSFET current limit is nominally 4.0A and guaranteed 3.8A. This restricts the maximum output current, I_{OMAX}, based on Equation 7:

$$I_L = I_{L(AVG)} + (1/2 \times \Delta I_L) \quad \text{(EQ. 7)}$$

where:

I_L = MOSFET current limit

$I_{L(AVG)}$ = average inductor current

ΔI_L = inductor ripple current

$$\Delta I_L = \frac{V_{IN} \times [(V_O + V_{DIODE}) - V_{IN}]}{L \times (V_O + V_{DIODE}) \times f_{SW}} \quad \text{(EQ. 8)}$$

V_{DIODE} = Schottky diode forward voltage, typically, 0.6V

f_{SW} = switching frequency, 640kHz or 1.22MHz

$$I_{L\text{-}AVG} = \frac{I_{OUT}}{1 - D} \quad \text{(EQ. 9)}$$

D = MOSFET turn-on ratio:

$$D = 1 - \frac{V_{IN}}{V_{OUT} + V_{DIODE}} \quad \text{(EQ. 10)}$$

Cascaded MOSFET Application

A 24V N-Channel MOSFET is integrated in the boost regulator. For the applications where the output voltage is greater than 24V, an external cascaded MOSFET is needed as shown in Figure 16. The voltage rating of the external MOSFET should be greater than VIN.

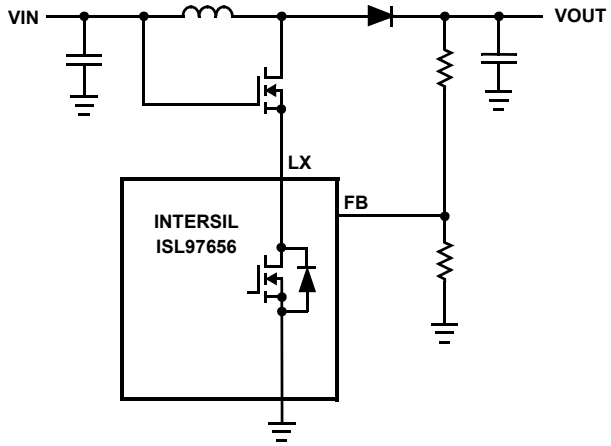


FIGURE 16. CASCADED MOSFET TOPOLOGY FOR HIGH OUTPUT VOLTAGE APPLICATIONS

DC PATH BLOCK APPLICATION

There is a DC path in the boost converter from the input to the output through the inductor and diode. In the non-synchronous topology, although the system is still in shutdown mode, the output voltage will be the input voltage minus the forward voltage diode drop of the Schottky diode. If this voltage is not desired, the following circuit (see Figure 17) can be used between input and inductor to disconnect the DC path when the ISL97656 is in shutdown mode.

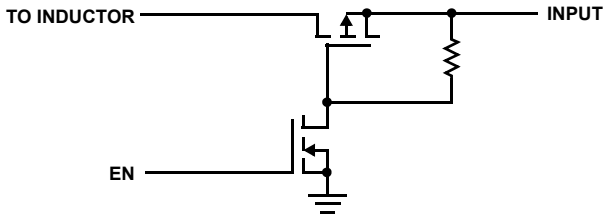


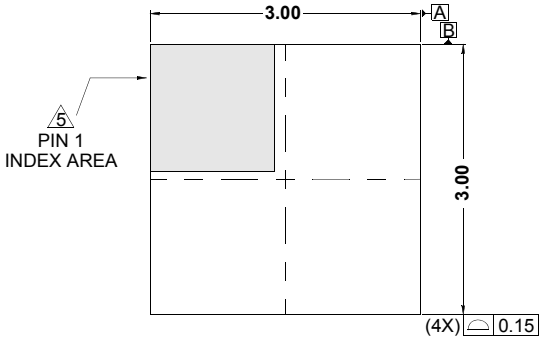
FIGURE 17. CIRCUIT TO DISCONNECT THE DC PATH OF BOOST CONVERTER

Package Outline Drawing

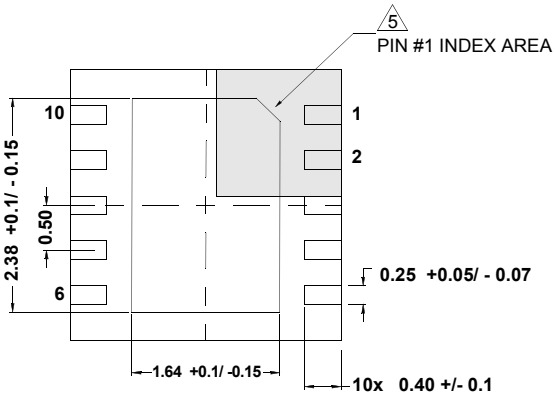
L10.3x3B

10 LEAD THIN DUAL FLAT PACKAGE (TDFN) WITH E-PAD

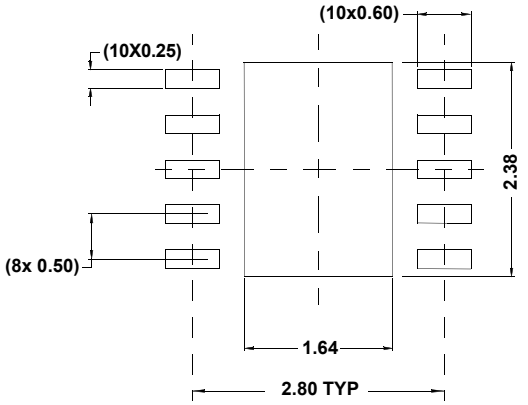
Rev 3, 10/11



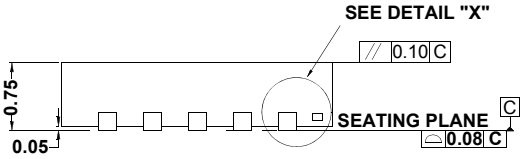
TOP VIEW



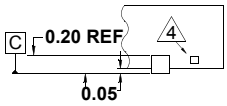
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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