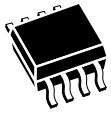
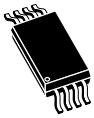
ST25DV02K-W1 ST25DV02K-W2

Datasheet

Dynamic NFC/RFID tag IC with up to two PWM outputs and 2-Kbit EEPROM



SO8



TSSOP8

Product status link
ST25DV02K-W1
ST25DV02K-W2

Features

Pulse width modulation outputs

- Two independent outputs: 1x PWM output on ST25DV02K-W1, 2x PWM outputs on ST25DV02K-W2
- From 488 Hz to 31250 Hz
- 62.5 ns pulse width resolution: from 15-bit resolution at 488 Hz to 9-bit resolution at 31.25 kHz
- Accuracy: ±10% over temperature range
- No need for external oscillator
- Supply voltage from 1.8 V to 5.5 V, independent from contactless interface
- Independent push-pull outputs
  - Up to 4 mA drive capability per output
  - Adjustable output drive for low power and low noise application
- Live update of PWM parameters controlled by contactless interface

Contactless interface

- Based on ISO/IEC 15693 and NFC Forum Type 5 Tag
- Supports all ISO/IEC 15693 modulations, coding, sub-carrier modes and data rates
- Single and multiple blocks read
- Internal tuning capacitance: 28.5 pF

Memory

- 2-kbit of EEPROM
- Accessible in blocks of 4x bytes
- 5 ms typical write time (one block)
- Data retention: 40 years
- Write cycles endurance: 100k write cycles at 85 ºC

Data protection

- Up to four independent areas, including the PWM control area, with flexible protection mechanism based on 32/64-bits passwords
- System configuration: write protection by 32-bit password
- TruST25™ Digital signature mechanism for authentication

Temperature range

- From -40°C to +85°C (Contactless interface)
- From -40 °C to +105 °C (PWM interface)

Package

- SO8N and TSSOP8
- ECOPACK2 (RoHS compliant)

1 Description

The ST25DV02K-W1/2 is an ISO 15693 and NFC Forum Type 5 tag, with one or two pulse width modulation (PWM) outputs and 2 Kbits of electrically erasable programmable memory (EEPROM).

It offers two interfaces. The first delivers up to 2x independent PWM output signals and the second is an RF link activated by the received carrier electromagnetic wave.

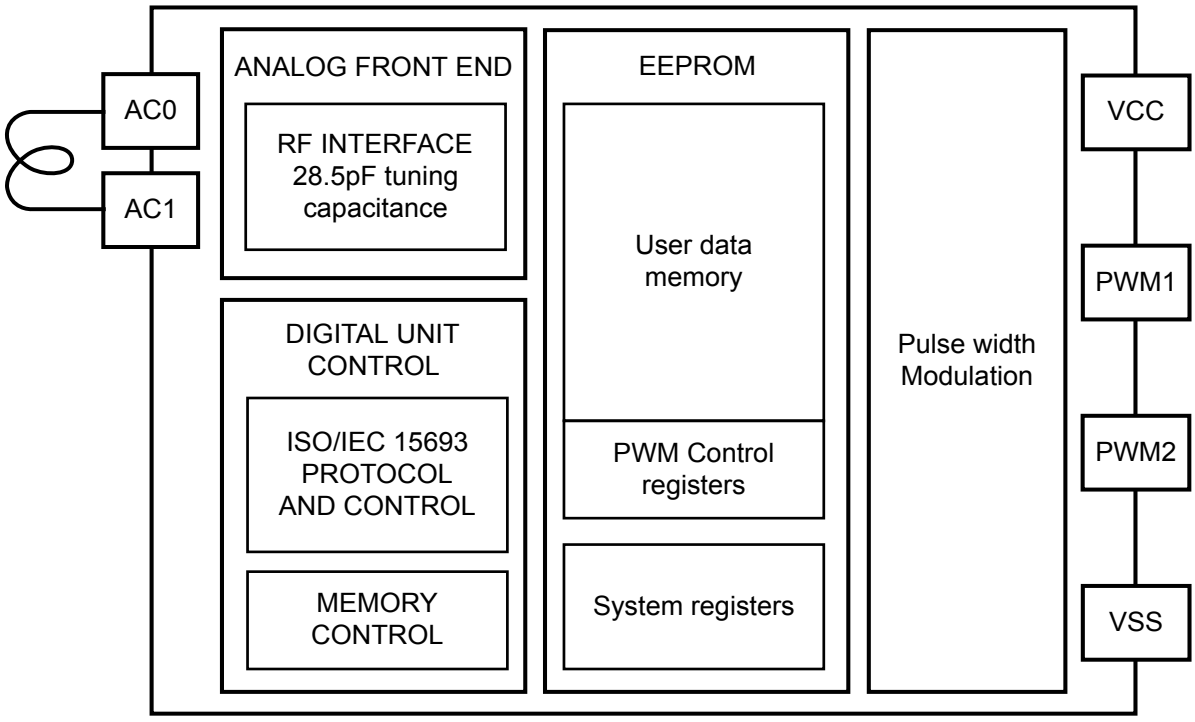
The PWM outputs are configured at boot time, and can be updated live through RF link. RF and PWM are independently powered and can work in stand-alone mode.

The ST25DV02K-W1/2 contains 256 bytes (64 blocks) of memory for User data. This memory is accessible through the RF interface, following ISO/IEC 15693 or NFC Forum Type 5 Tag recommendations.

The device is based on technology and design solutions for which there are pending patents.

1.1 Block diagram

Figure 1. Block diagram



Note: PWM2 is available only on ST25DV02K-W2.

1.2 Package connections

ST25DV02K-W1/2 is provided in two different packages:

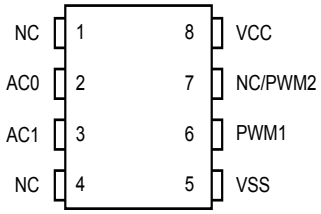
- SO8N
- TSSOP8

Table 1. Signal names

Signal name	Function	Direction
AC0	Antenna coils	I/O
AC1	Antenna coils	I/O
V_{CC}	PWM supply voltage	Power
PWM1	PWM output	Output
PWM2 (1)	PWM output	Output
V_{SS}	Ground	-

1. *Available only on ST25DV02K-W2.*

Figure 2. ST25DV02K-W1/2 8-pin package connections



2 Signal description

2.1 Pulse width modulation output (PWM1)

This signal provides a pulse width modulation output. It is a push-pull output signal, driven between V_{SS} and V_{CC}. PWM1 output is in high impedance state, as long as it is disabled.

2.2 Pulse width modulation output (PWM2)

This signal provides a pulse width modulation output. It is a push-pull output signal, driven between V_{SS} and V_{CC}. PWM2 is independent from PWM1. PWM2 output is available on ST25DV02K-W2 only, and it is in high impedance state, as long as it is disabled.

2.3 PWM power supply (V_{CC})

This pin must be connected to an external DC supply voltage to have the PWM output(s) working.

PWM power supply is independent from the RF NFC tag part: The RF NFC tag works whatever V_{CC} power supply state is. On the other side, PWM outputs work as soon as V_{CC} power is supplied, and whatever RF field state is.

2.4 PWM ground reference (V_{SS})

V_{SS} is the reference for the V_{CC} and PWM pins.

2.5 Antenna coil (AC0, AC1)

These inputs are used exclusively to connect the ST25DV02K-W1/2 device to an external coil. It is advised not to connect any other DC or AC path to AC0 or AC1.

When correctly tuned, the coil is used to power and access the device using the ISO/IEC 15693 and ISO 18000-3 mode 1 protocols.

3 Power management

3.1 Wired interface

Operating supply voltage V_{CC}

A valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied to guarantee PWM outputs within expected range (clock stability, jitter). To maintain a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually one ~10 nF capacitor plus one ~100 pF capacitor) close to the V_{CC}/V_{SS} package pins.

Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. The V_{CC} rise time must not vary faster than 1V/µs.

At power-up (continuous rise of V_{CC}), the ST25DV02K-W enter PWM boot, as soon as V_{CC} reaches the power-on reset threshold voltage.

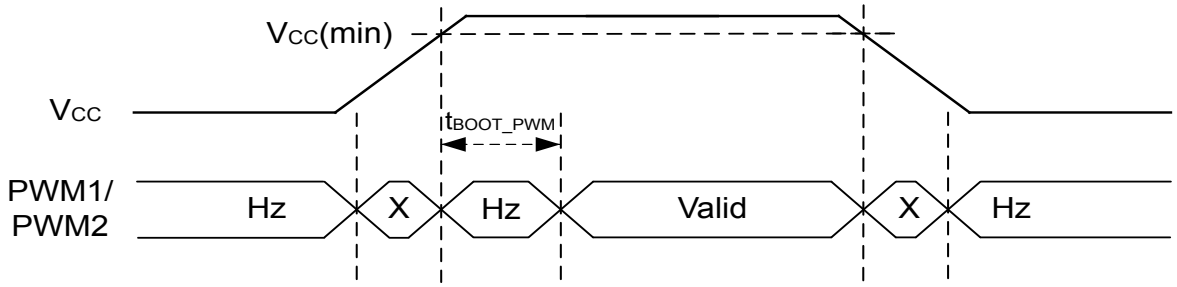
t_boot_PWM time applies to complete PWM boot and get valid PWM output signals.

In case of contactless interface access to EEPROM, the PWM boot is waiting for the end of EEPROM accesses to start.

Power-down conditions

At power-down (continuous decrease of V_{CC}), as soon as V_{CC} drops below the power-on reset threshold voltage, the PWM output states are not guaranteed anymore.

Figure 3. Power-up/down sequence



Note: Valid when RF interface is OFF, otherwise the priorities described in Section 3.3 RF and PWM boots priority apply.

3.2 Contactless interface

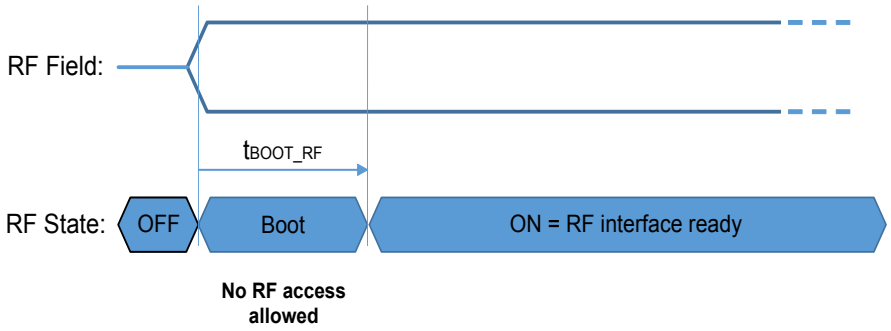
Device set in RF mode

To ensure a proper boot of the RF circuitry, the RF field must be turned ON without any modulation for a minimum period of time t_{RF_ON}. Before this time, ST25DV02K-W1/2 ignores all received RF commands (see Figure 4. RF power-up sequence).

Device reset in RF mode

To ensure a proper reset of the RF circuitry, the RF field must be turned off for a minimum t_{RF_OFF} period of time.

Figure 4. RF power-up sequence



1. Valid when PWM power supply (V_{CC}) is stable since t_boot_PWM, otherwise the priorities described in Section 3.3 RF and PWM boots priority apply.

3.3 RF and PWM boots priority

RF and PWM interfaces are independent, but the following boots priorities apply:

- If PWM boot (V_{CC} rising edge) occurs while RF is booting, or RF is in use, the PWM boot is delayed upon end of RF boot, or end of RF activity (EOF).
- If RF boot (Field On) occurs while PWMs are booting, the RF boot is delayed upon PWM boot completion.
- If RF boot (Field On) occurs while PWMs are running (valid PWM output signals), RF boot starts as described in Section 3.2 Contactless interface.

Note: It is recommended to run RF sequences (RF Field On, set of RF commands, RF Field Off) either before PWM boot (V_{CC} power supply is OFF and stable), or after PWM boot is completed (V_{CC} power supply is ON and stable).

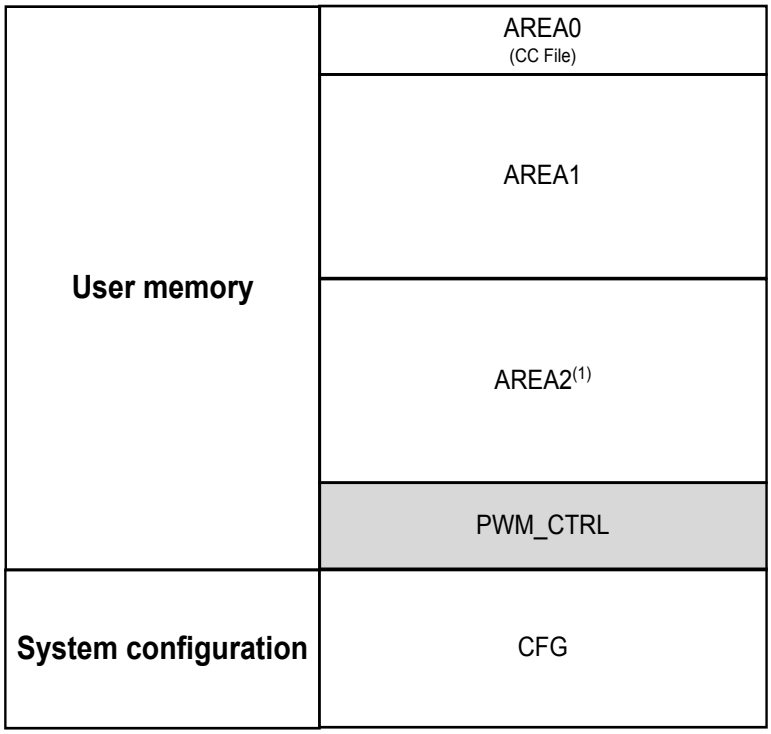
4 Memory management

4.1 Memory organization

The ST25DV02K-W1/2 memory is organized as follows:

- User memory: it is composed of four different areas, as described in Section 4.2 User memory. It contains areas for user's data, area for PWM control and area to store NFC T5 CC file if required.
- System configuration memory: it is composed of different configuration registers, among which the device configuration, the ISO15693 AFI & DSFID registers. It also contains the UID and different protection registers. Refer to Section 4.3 System configuration memory for more details

Figure 5. Memory organization



1. Can be merged with AREA1

4.2 User memory

User memory is addressed as blocks (= pages) of 4 bytes, starting at address 0.

All the blocks of the user memory are initialized to 00h in the factory.

The ST25DV02K-W1/2 user memory areas are defines as follow:

- AREA0 starts at address 00h. It is composed of 1x block (4x bytes) which is always readable, and can be locked. AREA0 has been though for the CC file content according to NFC Type 5 formalism. However an application, which does not require to be NFC Type5 compliant, can do any other usage of this block.
- AREA1 starts at address 01h. It is composed of 31x blocks (124x bytes). It can be read and/or write-protected by dedicated 1x32-bit password. AREA1 is dedicated to user's data.
- AREA2 starts at address 20h. It is composed of 32x blocks (128x bytes). It can be read, and/or write-protected by dedicated 1x32-bit password. AREA2 is dedicated to user's data.

Note: AREA1 and AREA2 can be merged in a single area of 63x blocks (252x bytes), which can be read - and/or - write-protected by 1x64-bit password.

- PWM CTRL area starts at address F8h. It is composed of 2x blocks, one per PWM, and is dedicated to PWM control (Enable, Period value and Pulse Width value). It can be individually read - and/or - write-protected by 32-bit password.

Areas definition are fixed and can not be changed (expect the merge of AREA1 and AREA2)

Table 2 and Table 3 show the user area mode explained above.

Table 2. User memory 4x areas configuration

Block addr. (hex)	Data bits [31:1]	Comment	RF command
0	User 0 (4x bytes)	AREA0 = CC file in case of NFC T5 application	Read Single Block Read Multiple Blocks Write Single Block
1	User area (124x bytes)	AREA1	
2			
…			
1E			
1F			
20	User area (128x bytes)	AREA2	
…			
…			
…			
3F			
-	-	-	
F8	PWM1 control	PWM_CTRL	
F9	PWM2 control		

Table 3. User memory 3x areas configuration

Block addr. (hex)	Data bits [31:0]	Comment	RF command
0	User 0 (4x bytes)	AREA0 = CC file in case of NFC T5 application	Read Single Block Read Multiple Blocks Write Single Block
1	User area (252x bytes)	AREA1 merged with AREA2	
2			
…			
1E			
1F			
20			
…			
…			
…			
3F			
-	-	-	
F8	PWM1 control	PWM_CTRL	
F9	PWM2 control		

4.3 System configuration memory

In addition to user memory, ST25DV02K-W1/2 includes a set of registers located in the system configuration memory. Registers content is read during the boots sequences and define basic ST25DV02K-W1/2 behaviour.

Some of those registers can be accessed via Read Configuration and Write Configuration commands, with an identifier acting as the register address.

Table 4. System configuration memory map shows the complete map of the system configuration registers, including their accessibility (Read / Write) and related conditions. More details are available in related registers table descriptions.

Table 4. System configuration memory map

RF access		Static Register	
Address	Type	Name	Function
00h	RW (1)	Table 15. A1SA access	AREA1 security attributes
01h	RW(1)	Table 17. A2SA access	AREA2 security attributes
02h	RW(1)	Table 19. APSA access	Area PWM_CTRL security attributes
03h	RW(1)	Table 9. PWM_CFG access	PWM Configuration and coexistence with RF interface
04h	RW(1)	Table 21. LOCK_CFG access	Configuration registers permanent lock
NA	R (2) W (3)	Table 23. LOCK_BLOCK of AREA0/1/2 and PWM_CTRL access	Blocks Write protection (1x lock bit per block)
NA	WO (4)	Table 34. LOCK_DSFID access	DSFID lock status
NA	WO (5)	Table 36. LOCK_AFI access	AFI lock status
NA	RW(4)	Table 38. DSFID access	DSFID value
NA	RW(5)	Table 40. AFI access	AFI value
NA	RO	Table 42. IC_REF access	IC reference value
NA	RO	Table 44. UID access	Unique identifier, 8 bytes
NA	WO (6)	Table 25. PWD_PWM access	PWM Control area security session password, 4 bytes
NA	WO(6)	Table 27. PWD_A1 access	User AREA1 security session password, 4 bytes
NA	WO(6)	Table 29. PWD_A2 access	User AREA2 security session password, 4 bytes
NA	WO(6)	Table 31. PWD_CFG access	Configuration security session password, 4 bytes

1. *Write access is granted if RF configuration security session is open and configuration is not locked (LOCK_CFG register equals to 0).*
2. *LOCK_BLOCK content is only readable through reading the Block Security Status of blocks.*
3. *Write access if the blocks are not already locked (=corresponding security session is open + block not already locked by a previous LOCK_BLOCK command).*
4. *Write access if DSFID is not already locked by a previous LOCK_DSFID command.*
5. *Write access if AFI is not already locked by a previous LOCK_AFI command.*
6. *Write access only if corresponding security session is open.*

5 Specific features

ST25DV02K-W1/2 offers the following features:

- Pulse width modulation output
- Data protection
- TruST25 digital signature
- Device parameter registers

For some of them, the control registers are located in System Configuration area, and require the use of Read_Configuration or Write_Configuration commands. Update is only possible when the access right has been granted by presenting the configuration password (PWD_CFG), and if the system configuration was not previously locked (by LOCK_CFG=1).

After any valid write access to the configuration registers, the new configuration is immediately applied.

5.1 Pulse width modulation output

The chip provides up to 2x Pulse width modulation (PWM) outputs. This chapter describes how to configure and use each PWM.

5.1.1 Control and configuration registers

PWM control registers define the basic PWM settings for each PWM output: Enable, Period and Pulse width, as described in Section 5.1.2 Pulse width modulation feature description.

Table 5. PWM1_CTRL access

RF	
Command	**Type**
Read Single Block (cmd code 20h) @F8h Read Multiple Blocks (cmd code 23h) @F8h Lock Single Block (cmd code 22h) @ F8h Write Single Block (cmd code 21h) @F8h	Read and Write protectable depending on APSA register content, on block lock status and on security session status (opened or closed)

Table 6. PWM1_CTRL

Bit	Name	Function	Factory Value
b14-b0	PWM1_PERIOD	**PWM period value**(1) The period of the PWM1 output signal is calculated using the following formula: Period = 'PWM1_PERIOD' x PWMres (see Table 113. PWM characteristics). PWM1_PERIOD value must be within the [512 : 32767] range.	0000h
b15	RFU	Reserved for future usage	0b
b30-b16	PWM1_PULSEW	**PWM pulse width value**(1): The pulse width duration of the PWM1 output signal is calculated using the following formula: Pulse width = 'PWM1_PULSEW' x PWMres (see Table 113. PWM characteristics). PWM1_PULSEW value must be within the [0 : 32767] range.	00000h
b31	PWM1_ENABLE	Enable of PWM output signal	0b

1. *Refer to Section 5.1.2 Pulse width modulation feature description for details on PWM1_PERIOD and PWM1_PULSEW values.*

PWM2_CTRL register only applies with ST25DV02K-W2 chip version (2x PWM outputs). In case of single PWM output device version (ST25DV02K-W1), PWM2_CTRL register value has to be kept to its factory value (all bits = 0).

Table 7. PWM2_CTRL access

RF	
Command	**Type**
Read Single Block (cmd code 20h) @F9h Read Multiple Blocks (cmd code 23h) @F9h Lock Single Block (cmd code 22h) @ F9h Write Single Block (cmd code 21h) @F9h	R & W protectable depending on APSA register content, on block lock status and on security session status (opened or closed)

Table 8. PWM2_CTRL

Bit	Name	Function	Factory Value
b14-b0	PWM2_PERIOD	**PWM period value**: (1) The period of the PWM2 output signal is calculated using following formula: Period = 'PWM2_PERIOD' x PWMres (see Table 113. PWM characteristics) PWM2_PERIOD value must be within the [512 : 32767] range.	0000h
b15	RFU	Reserved for future usage	0b
b30-b16	PWM2_PULSEW	**PWM pulse width value**(1): The pulse width duration of the PWM2 output signal is calculated using the following formula: Pulse Width = 'PWM2_PULSEW' x PWMres (see Table 113. PWM characteristics) PWM2_PULSEW value must be within the [0 : 32767] range.	00000h
b31	PWM2_ENABLE	Enable of PWM output signal	0b

1. *Refer to Section 5.1.2 Pulse width modulation feature description for details on PWM2_PERIOD and PWM2_PULSEW values.*

PWM Configuration register defines the expert PWM settings: Drive and coexistence parameters, as described in Section 5.1.2 Pulse width modulation feature description.

Table 9. PWM_CFG access

RF	
Command	**Type**
Read Configuration (cmd code A0h) @03h	R always
Write Configuration (cmd code A1h) @03h	W if configuration security session is open and configuration not locked

Table 10. PWM_CFG

Bit	Name	Function	Factory Value
b1-b0	PWM1_DRIVE	PWM output driver trimming: • 00: Full power output available • 01: ¾ of full power output available • 10: ½ of full power output available • 11: ¼ of full power output available	00b
b3-b2	PWM2_DRIVE		00b
b6-b4	DUALITY_MNGT	PWM and RF interface coexistence (applies to both PWM): • 000: Full coexistence of PWM output and RF interface • 1xx: PWM output set in HiZ during RF commands(1) • 01x: Power of PWM output reduced to ¼ of full power during RF commands (1) • 0x1: PWM frequency reduced below Low_Freq(2) during RF commands(1), while keeping PWM duty cycle	000b
b7	RFU	Reserved for future usage	0b

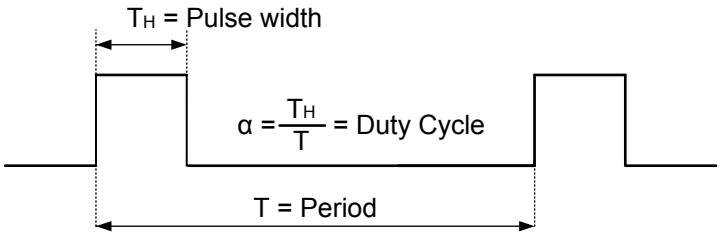
1. *During RF command period starts from SOF (Start of Frame) and ends at the end of the Answer.*
2. *Refer to Section 8 Device parameters.*

5.1.2 Pulse width modulation feature description

A PWM output is characterized by two parameters:

- its period (or frequency)
- its duty cycle, representing the percentage of time the signal is in high state

Figure 6. PWM output



Period and pulse width are used to define and control the PWM output, in addition to an enable signal, allowing to put the PWM output in HiZ state.

PWM stage is supplied by V_{CC}/V_{SS} power pins. It is not supplied by RF interface. PWM works even when RF interface is OFF, as long as power is supplied through V_{CC}/V_{SS} pins. Similarly, RF interface works without V_{CC}/V_{SS}.

The PWM output stage is a push pull.

Refer to Section 3 Power managementfor details on V_{CC} Power-on/power-off and related PWM output states.

PWM control (PWM1_CTRL and PWM2_CTRL)

PWM control registers are located in a dedicated user area (PWM_CTRL), which is protected by a dedicated password (PWD_PWM) and its own access right register (APSA). Each PWM output is controlled by an independent register: PWM1_CTRL and PWM2_CTRL.

Each PWM control register provides user access to period value, pulse width value and an enable bit of the corresponding PWM output. Period and pulse width parameters are coded on 15 bits each: PWMx_PERIOD and PWMx_PULSEW.

PWM output state is defined from these three parameters as follows:

Table 11. PWM output parameters

PWM_EN	PWMx_PERIOD	PWMx_PULSEW	PWM output state	Comments
0	x	x	HiZ	Disabled
1	P [512 : 32767]	0	0	< V_{OL}
		0 < W < P		PWM w. Duty Cycle
		≥ P	1	> V_{OH}

An internal oscillator fixes the PWM resolution to PWMres (see Table 113. PWM characteristics). The PWM output period and pulse width are defined as multiples of this resolution value:

- Period = PWMres x PWMx_PERIOD
- Pulse Width = PWMres x PWMx_PULSEW

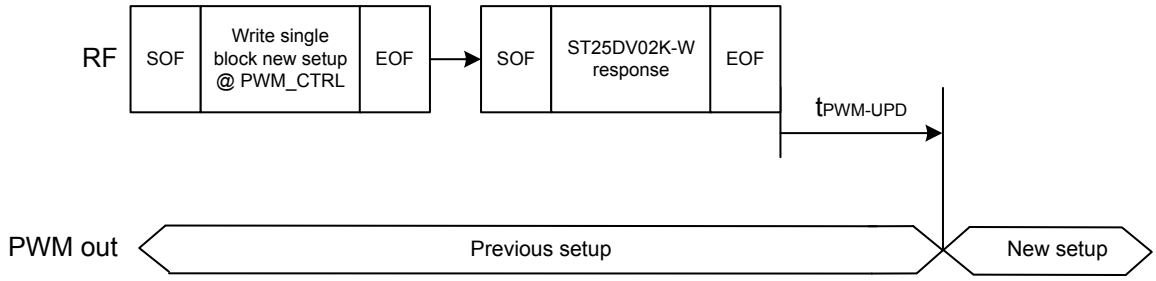
PWM output functionality is guaranteed over PWMx_PERIOD range from 512 to 32767, which implies a Period range from 32 to 2048 µs (corresponding to a frequency from 31250 to 488.3 Hz). Over this range, the PWM output resolution is as follows:

Table 12. PWM output resolution

PWM output frequency (Hz)	Number of bits used for PWMx_PERIOD	PWM resolution (number of bits available to code PWMx_PULSEW)
31250	9	9
15625	10	10
7813	11	11
3906	12	12
1953	13	13
977	14	14
488	15	15

When PWM_CTRL registers are updated by a successful RF command (Write Single Block @ F8h/F9h with response), the related PWM output change applies as follows:

Figure 7. PWM output change



There is no anti-tearing mechanism on PWM_CTRL registers. Write access to PWM_CTRL registers must be done with stable RF field and constant V_{CC} state (either ON or OFF). Otherwise the RF write operation may not complete properly, implying a loss/corruption of register content, requiring a new Write operation.

PWM Configuration (PWM_CFG)

PWM configuration register is located in System Configuration area.

It provides access to output driver level adjustment, in addition to extended coexistence modes between RF and PWM interfaces.

Configuration of PWM output driver trimming: the PWM push-pull output stage is able to drive up to I_{MAX} (refer to Section 8 Device parameters) by default. If the application does not require full power it is possible to reduce the output drive capability independently through PWM_CFG trimming registers (PWM_CFG bits b1-b0 for PWM1 and PWM_CFG bits b3-b2 for PWM2).

Table 13. PWM output driver trimming

PWM_CFG[1:0]/PWM_CFG[3:2]/	PWM1/PWM2 output drive capability (sink and source)
00b	I_{MAX} (default setup) (1)
01b	75% of I_{MAX} (1)
10b	50% of I_{MAX} (1)
11b	25% I_{MAX} (1)

1. *Refer to Section 8 Device parameters.*

Configuration of PWM output coexistence with RF: a PWM_CFG Duality_Mngt register (PWM_CFG bits b6-b4) allows to reduce the impact of PWM noise over RF interface, and then help the coexistence. This register applies to both PWM outputs (when applicable).

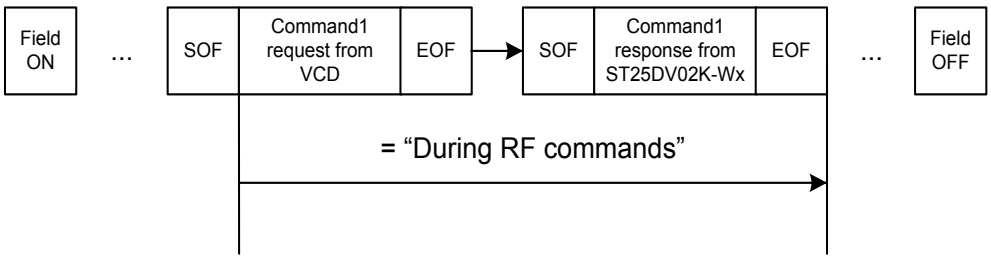
Table 14. PWM output coexistence with RF interface

PWM_CFG[6:4]	Coexistence setting
000b	PWM and RF working normally and simultaneously (default setup)
1xxb	Put PWM outputs in HiZ state during RF commands.
01xb	Reduce PWM outputs drive to minimum power level (25% of the maximum output power level), during RF commands.
0x1b	Reduce PWM outputs frequencies (while keeping duty cycles), in order to move them below a predefined value (Low_Freq, see Table 113. PWM characteristics), and then move out of the VCD RF sensitivity region. This option only applies if PWM output frequencies are above the predefined frequency value

The option 1xxb = "Put PWM outputs in HiZ state" is exclusive option, whereas "Reduced PWM drive" and "Reduced frequency" options can be cumulated if needed.

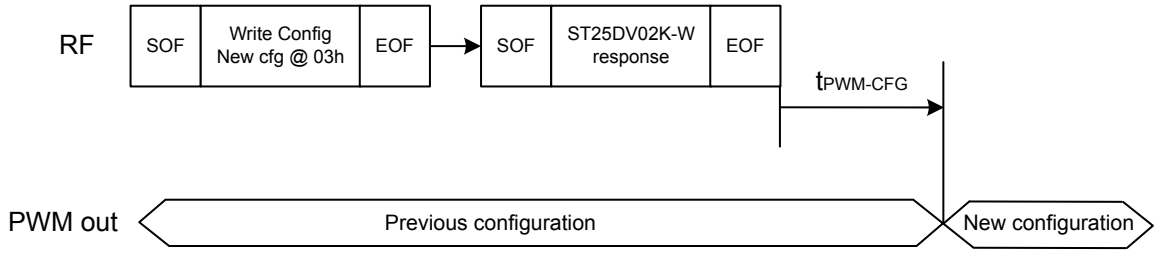
Coexistence options only applies "during RF commands", in order to minimize impact on PWM output signals. "During RF commands" period is defined from Start-of-Frame of the request command, up to the End-of-Frame of the corresponding answer:

Figure 8. PWM answer



When PWM_CFG register is updated by a successful RF command (Write_Config @ 03h with response), PWM outputs change applies as follow:

Figure 9. PWM output change



There is no anti-tearing mechanism on PWM_CFG register. Write access to PWM_CFG registers shall be done with stable RF field and constant VCC state (either ON or OFF). Otherwise the RF write operation may not complete properly, and could imply a loss/corruption of register content, requiring a new Write config operation.

5.2 Data protection

ST25DV02K-W1/2 provides a special data protection mechanism based on passwords that unlock security sessions. 4 x 32 bits passwords are stored in EEPROM, covering:

- Password for AREA1
- Password for AREA2 (If AREA1 and AREA2 are merged, the corresponding area will be protected by a 64 bits password),
- Password for PWM control area
- Password for System Configuration area

User memory can be protected from read and/or write access. The system configuration is always protected from write access.

Other lock mechanisms are supported (lock block, lock AFI, lock DSFID), as described in the following sections.

5.2.1 Data protection registers

Registers described in this chapter are all located in System configuration memory. Refer to Table 4. System configuration memory map for more details.

Table 15. A1SA access

RF	
Command	**Type**
Read Configuration (cmd code A0h) @00h	R always
Write Configuration (cmd code A1h) @00h	W if configuration security session is open and configuration not locked

Table 16. A1SA

Bit	Name	Function	Factory Value
b1-b0	RW_PROTECTION_A1	AREA1 access rights: 00: Read always is allowed / Write always allowed 01: Read always is allowed / Write allowed only if AREA1 user security session is opened (= the proper AREA1 password has been presented) 10: Read and Write is allowed only if AREA1 user security session is opened (the proper AREA1 password has been presented) 11: Read is only allowed if AREA1 user security session is opened (the proper AREA1 password has been presented) / Write always forbidden	00b
b2	MEM_ORG	User memory split: 0: user memory is split in four areas (AREA0/1/2 & PWM_CTRL) 1: user memory is split in three areas (AREA0/1 & PWM_CTRL) = AREA1 & AREA2 are merged in a single AREA1. In case of merged areas, RW_PROTECTION_A1 register applies as access rights.	1b
b7-b3	RFU	-	00000b

Table 17. A2SA access

RF	
Command	**Type**
Read Configuration (cmd code A0h) @01h	R always
Write Configuration (cmd code A1h) @01h	W if configuration security session is open and configuration not locked

Table 18. A2SA

Bit	Name	Function	Factory Value
b1-b0	RW_PROTECTION_A2	AREA2 access rights: 00: Read is always allowed / Write always allowed 01: Read always is allowed. Write is only allowed if AREA2 user security session is opened (= the proper AREA2 password has been presented) 10: Read and Write is only allowedif AREA2 user security session is opened (the proper AREA2 password has been presented) 11: Read is only allowed if AREA2 user security session is opened (the proper AREA2 password has been presented), Write is always forbidden. In case of merged AREA1 + AREA2 in a single AREA1, the RW_PROTECTION_A2 bits are not used.	00b
b7-b2	RFU	-	00000b

Table 19. APSA access

RF	
Command	**Type**
Read Configuration (cmd code A0h) @02h	R always
Write Configuration (cmd code A1h) @02h	W if configuration security session is open and configuration not locked

Table 20. APSA

Bit	Name	Function	Factory Value
b1-b0	RW_PROTECTION_AP	Area PWM_CTRL access rights: 00: Read and Write are always allowed. 01: Read is always allowed. Write is only allowed if Area PWM_CTRL user security session is opened (= the proper Area PWM_CTRL password has been presented) 10: Read and Write are only allowed if Area PWM_CTRL user security session is opened (the proper area PWM_CTRL password has been presented) 11: Read is only allowed if Area PWM_CTRL user security session is opened (the proper area PWM_CTRL password has been presented). Write is always forbidden.	00b
b7-b2	RFU	-	00000b

Table 21. LOCK_CFG access

RF	
Command	**Type**
Read Configuration (cmd code A0h) @04h	R always
Write Configuration (cmd code A1h) @04h	W if configuration security session is open and configuration not locked

Table 22. LOCK_CFG

Bit	Name	Function	Factory Value
b0	LOCK_CFG	Lock configuration register: 0: Configuration registers are unlocked 1: Configuration registers are permanently locked in write. It only concerns configuration registers accessible by Write_Config command. Passwords, AFI, DSFID, Block lock, AFI lock & DSFID lock are not concerned by this mechanism.	0b
b7-b1	RFU	-	0000000b

Table 23. LOCK_BLOCK of AREA0/1/2 and PWM_CTRL access

RF	
Command	**Type**
Read Block (cmd code 20h) @Block addr Read Multi Block (cmd code 23h) @Block addr Get Multi Block Security Status (cmd code 2Ch) @Block addr Lock single Block (cmd code 22h) @Block addr	R always W only if corresponding Block is not locked

Table 24. LOCK_BLOCK of AREA0/1/2 and PWM_CTRL

Bit	Name	Function	Factory Value	
N/A	LOCK_BLOCK	Lock write access of corresponding block: 0: Block not locked in Write 1: Block permanently locked in write		0b

Table 25. PWD_PWM access

RF	
Command	**Type**
No Read Write password (cmd code B1h) with Pwd_Id = 00h	No Read W only if PWM_CTRL Area security session is opened

Table 26. PWD_PWM

Bit	Name	Function	Factory Value
bit31-b0	PWD_PWM	Password value for PWM_CTRL area	00000000h

Table 27. PWD_A1 access

RF	
Command	**Type**
No Read Write password (cmd code B1h) with Pwd_Id = 01h	No Read W only if AREA1 security session is opened.

Table 28. PWD_A1

Bit	Name	Function	Factory Value
b31-b0	PWD_A1	When MEM_ORG=0: Password value for user AREA1 When MEM_ORG=1: LSB password value (32bits out of 64) for user AREA1 (merged with AREA2)	00000000h

Table 29. PWD_A2 access

RF	
Command	**Type**
No Read Write password (cmd code B1h) with Pwd_Id = 02h	No Read W only if: • AREA2 security session is opened (when MEM_ORG=0) • AREA1 security session is opened (when MEM_ORG=1, AREA1+AREA2 are merged)

Table 30. PWD_A2

Bit	Name	Function	Factory Value
b31-b0	PWD_A2	When MEM_ORG = 0: Password value for user AREA2 When MEM_ORG = 1: MSB password value (32 bits out of 64) for user area 1 (merged with AREA2)	00000000h

Table 31. **PWD_CFG access**

RF	
Command	**Type**
No Read Write password (cmd code B1h) with Pwd_Id = 03h	No Read W only if the System Configuration Area security session is opened.

Table 32. **PWD_CFG**

Bit	Name	Function	Factory Value
b31-b0	PWD_CFG	Password value for configuration area	00000000h

5.2.2 Passwords and security sessions

ST25DV02K-W1/2 provides protection of user memory and system configuration registers. User can access to the protected data by opening security sessions thanks to the help of corresponding password.

There is two types of security sessions, as shown in Table 33:

Table 33. **Security session type**

Security session	Open by presenting	Right granted when security session is open, and until it is closed
user	PWD_A1 PWD_A2 PWD_PWM	User can access to corresponding user memory as defined in AiSA registers User can update the password corresponding to the opened session.
configuration	PWD_CFG	User can write configuration registers (if not permanently locked) User can update PWM_CFG password

If AREA1 and AREA2 are independent (MEM_ORG = 0b), each of the AREA1 and 2 passwords is 32-bit long.

If AREA1 and AREA2 are merged in a single area (MEM_ORG = 1b), the merged area password is 64-bit long (made with 32-bit AREA1 password + 32-bit AREA2 password).

The ST25DV02K-W1/2 passwords management is based on two commands:

- Write Password (code B1h) (see Section 6.4.17 Write Password).
- Present Password (code B3h) (See Section 6.4.18 Present Password).

For any of the 4x passwords available, three actions are possible:

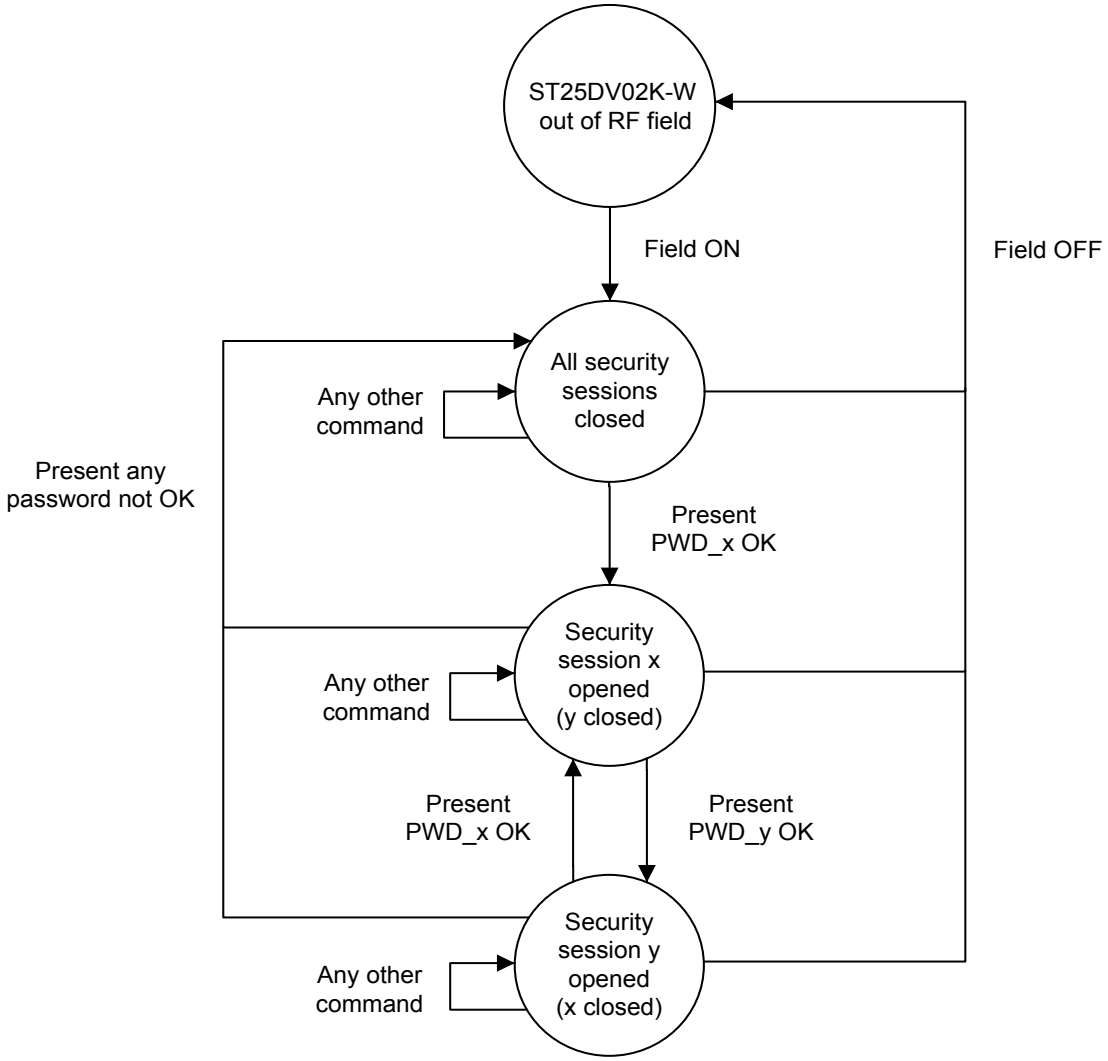
- Open Security Session: use Present_Password command, with password identifier (00h for PWD_PWM, 01h for PWD_A1, 02h for PWD_A2 and 03h for PWD_CFG) and the valid corresponding password.
- Write password: use Present_Password command, with password identifier (00h for PWD_PWM, 01h for PWD_A1, 02h for PWD_A2 and 03h for PWD_CFG) and the valid corresponding password. Then use Write_Password command, with same password identifier and the new password.
- Close Security Session: to close the current security session, user can choose one of the following options:
  - Remove tag from RF field
  - Use Present_Password command with a wrong password
  - Use Present_Password command to open security session of another Area (using a different password identifier). Opening a new security session (user or configuration) automatically close the previously opened one (even if the new opening fails)

Note: In case of merged AREA1 + AREA2 (MEM_ORG=1b), the Security session opening is different:

- The 64-bit password is presented with one Present_Password operation,
- Write_Password command still applies on 32-bit password, hence update of the 64-bit password must be done by 2x Write_Password operations, with AREA1 password Id and with AREA2 password Id,

Figure 10 describes the mechanism to open/close the security sessions.

Figure 10. Security sessions management



5.2.3 User memory protection

- AREA0 (composed of a single block= block0):
  - It is always readable,
  - It can only be individually write locked by issuing a Lock Single Block command. This lock is permanent,
  - User needs no password to lock block 0,
  - Locking block 0 is possible even if the configuration is locked (LOCK_CFG=1).
- AREA1, AREA2 and PWM_CTRL areas:
  - Protections are independently defined by corresponding AiSA registers (A1SA, A2SA, APSA). See Table 15, Table 17 and Table 19 for details about available read and write protections.
  - When updating AiSA registers, the new protection value is effective immediately after the register write completion.
  - In addition to the password protection mechanism, each block composing AREA1, AREA2 & PWM_CTRL can be individually locked by issuing a Lock Single Block command (permanently lock the write access to the corresponding block).

On factory delivery, user areas protection are all disabled.

Retrieve the security status of a user memory block or byte

User can read a block security status by issuing following commands:

- Get Multiple Blocks Security Status command
- Read Single Block with option flag set to 1
- Read Multiple Blocks with option flag set to 1

ST25DV02K-W1/2will respond with a Block security status containing a Lock_bit flag as specified in ISO 15693 standard. This lock_bit flag is set to one if block is locked against write.

Such lock against write can be obtained by different ways:

- Either the Lock_Block bit of the block has been set (permanent)
- Or security session is closed with protection in Write (RW_PROTECTION_Ax = 01b or 10b or 11b)
- Or security session is opened with protection on Write always forbidden (RW_PROTECTION_Ax = 11b)

5.2.4 System configuration memory protection

By default, system memory is write protected.

To enable write access to system configuration registers, user must open the configuration security session by presenting a valid password PWD_CFG (Id=03h) and system configuration must not be permanently locked (LOCK_CFG=00h).

By default, user can read every system configuration registers, except passwords, LOCK_DSFID and LOCK_AFI.

Configuration lock:

- Write access to system configuration registers can be permanently locked by writing 01h in the LOCK_CFG register.
- User cannot unlock system configuration if LOCK_CFG=01h, even after opening configuration security session (Lock is definitive).
- When system configuration is locked (LOCK_CFG=01h), it is still possible to change passwords (PWD_A1, PWD_A2, PWD_PWM, PWD_CFG).
- When system configuration is locked (LOCK_CFG=01h), it is still possible to lock AFI & DSFID registers (as described here after).

Device identification registers:

- AFI and DFSID registers can be independently locked by user, issuing respectively a Lock AFI and a Lock DSFID command. Lock is definitive: once locked, AFI and DSFID registers cannot be unlocked.
- Other device identification registers (IC_REF, UID) are read only registers.

5.3 TruST25 digital signature

The ST25DV02K-W devices support the TruST25 digital signature feature, which allows the user to verify the authenticity of the device, thanks to a unique digital signature.

TruST25 solution encompasses secure industrialization processes and tools deployed by STMicroelectronics to generate, store and check the signature in the device.

Refer to “AN5149 – TruST25 digital signature for ST25DV02K-W series Dynamic NFC Tags", available under NDA, for more details on how to use it. Contact your STMicroelectronics sales office to get this document.

5.4 Device parameter registers

Registers described in this chapter are located in System configuration memory. Refer to Table 4. System configuration memory map for more details.

Table 34. LOCK_DSFID access

RF	
Command	**Type**
Lock DSFID (cmd code 2Ah)	WO if DSFID not locked

Table 35. LOCK_DSFID

Bit	Name	Function	Factory Value
b0	LOCK_DSFID	0: DSFID is not locked 1: DSFID is locked	0b
b7-b1	RFU	-	0000000b

Table 36. LOCK_AFI access

RF	
Command	**Type**
Lock AFI (cmd code 28h)	WO if AFI not locked

Table 37. LOCK_AFI

Bit	Name	Function	Factory Value
b0	LOCK_AFI	0: AFI is not locked 1: AFI is locked	0b
b7-b1	RFU	-	0000000b

Table 38. DSFID access

RF	
Command	**Type**
Inventory (cmd code 01h) Get System Info (cmd code 2Bh) Write DSFID (cmd code 28h)	R always W if DSFID not locked

Table 39. DSFID

Bit	Name	Function	Factory Value
b7-b0	DSFID	ISO/IEC 15693 Data Storage Format Identifier	00h

Table 40. AFI access

RF	
Command	**Type**
Inventory (cmd code 01h) Get System Info (cmd code 2Bh) Write AFI (cmd code 27h)	R always W if AFI not locked

Table 41. AFI

Bit	Name	Function	Factory Value
b7-b0	AFI	ISO/IEC 15693 Application Family Identifier	00h

Table 42. IC_REF access

RF	
Command	**Type**
Get System Info (cmd code 2Bh)	RO

Table 43. IC_REF

Bit	Name	Function	Factory Value
b7-b0	IC_REF	ISO/IEC 15693 IC Reference	38/39h (1)

1. *38h applies to ST25DV02K-W1, 39h applies to ST25DV02K-W2.*

Table 44. UID access

RF	
Command	**Type**
Inventory (cmd code 01h) Get System Info (cmd code 2Bh)	RO

Table 45. UID

Bit	Name	Function		Factory Value
b7-b0	UID	ISO/IEC 15693 UID byte 0 (LSB)		IC manufacturer serial number
b15-b8		ISO/IEC 15693 UID byte 1		
b23-b16		ISO/IEC 15693 UID byte 2		
b31-b24		ISO/IEC 15693 UID byte 3		
b39-b32		ISO/IEC 15693 UID byte 4		
b47-b40		ISO/IEC 15693 UID byte 5: ST Product code		38/39h (1)
b55-b48		ISO/IEC 15693 UID byte 6: IC Mfg code		02h
b63-b56		ISO/IEC 15693 UID byte 7 (MSB)		E0h

1. *38h applies to ST25DV02K-W1, 39h applies to ST25DV02K-W2*

6 RF operation

Contactless exchanges are performed as specified by ISO/IEC 15693 and NFC Forum Type 5 Tag. The device communicates via the 13.56 MHz carrier electromagnetic wave on which incoming data are demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). The received ASK wave is 10% or 100% modulated with a data rate of 1.6 Kbit/s using the 1/256 pulse coding mode or a data rate of 26 Kbit/s using the 1/4 pulse coding mode.

Outgoing data are generated by the ST25DV02K-W1/2 load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data are transferred from the ST25DV02K-W1/2 at 6.6 Kbit/s in low data rate mode and 26 Kbit/s in high data rate mode.

The device follows ISO/IEC 15693 and NFC Forum Type 5 Tag recommendation for radio-frequency power and signal interface and for anticollision and transmission protocol.

6.1 RF communication

6.1.1 Access to an ISO/IEC 15693 device

The dialog between the reader and the ST25DV02K-W1/2 takes place as follows:

- activation of the ST25DV02K-W1/2 by the operating field of the reader
- transmission of a command by the reader (ST25DV02K-W1/2 detects carrier amplitude modulation)
- transmission of a response by the ST25DV02K-W1/2 using load modulation.

These operations use the power transfer and communication signal interface described below. This technique is called RTF (reader talk first).

Operating field

The ST25DV02K-W1/2 operates continuously between the minimum and maximum values of the electromagnetic field H defined in Table 112. RF characteristics. The reader has to generate a field within these limits.

Power transfer

Power is transferred to the ST25DV02K-W1/2 by radio frequency at 13.56 MHz via coupling antennas in the ST25DV02K-W1/2 and the reader. The operating field of the reader is transformed on the ST25DV02K-W1/2 antenna to an AC voltage that is rectified, filtered and internally regulated. During communications, the amplitude modulation (ASK) on this received signal is demodulated by the ASK demodulator.

Frequency

The ISO 15693 standard defines the carrier frequency (f_C) of the operating field as 13.56 MHz ± 7 kHz.

6.2 RF protocol

6.2.1 Protocol description

The transmission protocol (or simply “the protocol”) defines the mechanism used to exchange instructions and data between the VCD (vicinity coupling device) and the VICC (vicinity integrated circuit card) in both directions. It is based on the concept of “VCD talks first”. The device acts as the VICC.

This means that a ST25DV02K-W1/2 does not start transmitting unless it has received and properly decoded an instruction sent by the VCD. The protocol is based on an exchange of:

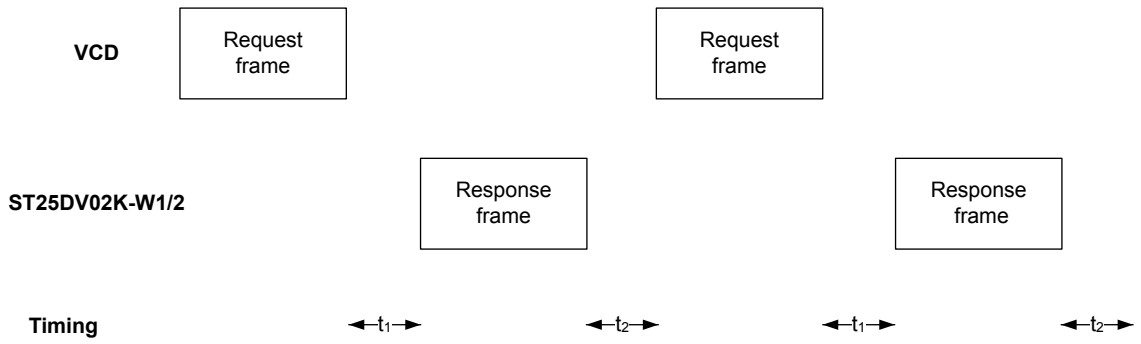
- a request from the VCD to the ST25DV02K-W1/2
- a response from the ST25DV02K-W1/2 to the VCD.

Each request and each response are contained in a frame. The frames are delimited by a Start of Frame (SOF) and End of Frame (EOF).

The protocol is bit-oriented. The number of bits transmitted in a frame is a multiple of eight (8), that is an integer number of bytes.

A single-byte field is transmitted least significant bit (LSBit) first. A multiple-byte field is transmitted least significant byte (LSByte) first and each byte is transmitted least significant bit (LSBit) first.

Figure 11. ST25DV02K-W1/2 protocol timing



6.2.2 Supported states

- Power-off
- Ready
- Quiet
- Selected

Transitions between these states are specified in Figure 12. Device state transition diagram and Table 46. Device response depending on Request_flags.

Power-off state

The ST25DV02K-W1/2 is in RF Power-off state when it does not receive enough energy from the VCD.

Ready state

The ST25DV02K-W1/2 is in the Ready state when it receives enough energy from the VCD. When in the Ready state, the ST25DV02K-W1/2 answers any request where the Select_flag is not set.

Quiet state

When in the Quiet state, the ST25DV02K-W1/2 answers any request with the Address_flag set, except for Inventory requests.

Selected state

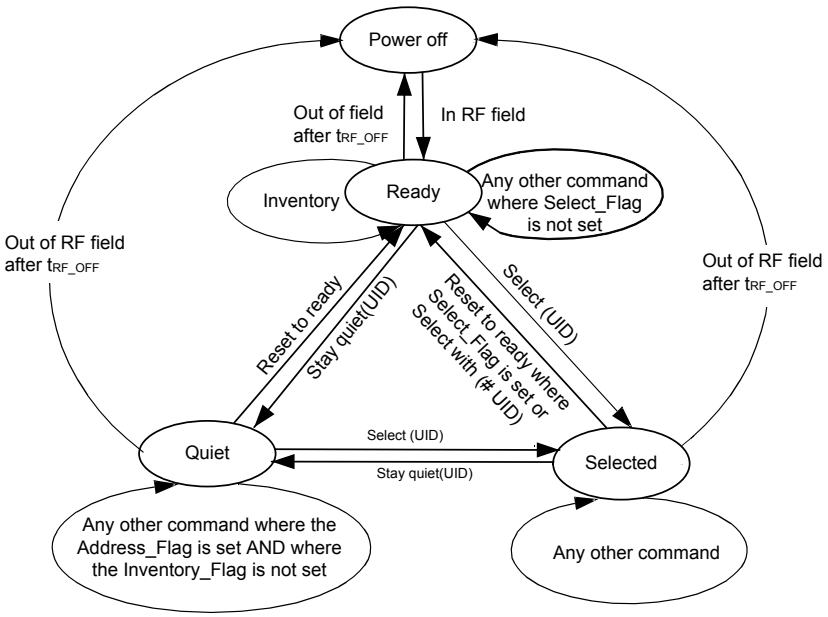
In the Selected state, the ST25DV02K-W1/2 answers any request in all modes (see Section 6.2.3 Modes):

- Request in Select mode with the Select_flag set
- Request in Addressed mode if the UID matches
- Request in Non-Addressed mode as it is the mode for general requests

Table 46. Device response depending on Request_flags

Flags	Address_flag		Select_flag	
	1 Addressed	0 Non addressed	1 Selected	0 Non selected
ST25DV02K-W1/2 in Ready or Selected state (devices in Quiet state do not answer)	-	X	-	X
ST25DV02K-W1/2 in Selected state	-	X	X	-
ST25DV02K-W1/2 in Ready, Quiet or Selected state (the device matching the UID)	X	-	-	X
Error (03h) or no response (command dependent)	X	-	X	-

Figure 12. Device state transition diagram



The ST25DV02K-W1/2 returns to the power-off state if the tag is out of the field for at least t_{RF_OFF}.

The intention of the state transition method is that only one ST25DV02K-W1/2 must be in the Selected state at any given time.

When the Select_flag is set to 1, the request must NOT contain a unique ID.

When the Address_flag is set to 0, the request must NOT contain a unique ID.

6.2.3 Modes

The term “mode” refers to the mechanism used in a request to specify the set of ST25DV02K-W1/2 devices that must execute the request.

Addressed mode

When the Address_flag is set to 1 (Addressed mode), the request contains the UID (unique ID) of the addressed ST25DV02K-W1/2.

Any ST25DV02K-W1/2 receiving a request with the Address_flag set to 1 compares the received UID to its own. If it matches the device executes the request (if possible) and returns a response to the VCD as specified in the command description.

If the UID does not match the device remains silent.

Non-addressed mode (general request)

When the Address_flag is cleared to 0 (Non-Addressed mode), the request does not contain a UID.

Select mode

When the Select_flag is set to 1 (Select mode), the request does not contain a unique ID. The ST25DV02K-W1/2 in the Selected state that receives a request with the Select_flag set to 1 executes it and returns a response to the VCD as specified in the command description.

Only the ST25DV02K-W1/2 in the Selected state answers a request where the Select_flag is set to 1.

The system design ensures that only one ST25DV02K-W1/2 can be in the Select state at a given time.

6.2.4 Request format

The request consists of:

- an SOF
- flags
- a command code
- parameters and data
- a CRC
- an EOF.

Table 47. General request format

SOF	Request_flags	Command code	Parameters	Data	2 byte CRC	EOF

6.2.5 Request flags

In a request, the “flags” field specifies the actions to be performed by the ST25DV02K-W1/2 and whether corresponding fields are present or not.

The flags field consists of eight bits. Bit 3 (Inventory_flag) of the request flag defines the contents of the four MSBs (bits 5 to 8). When bit 3 is reset (0), bits 5 to 8 define the ST25DV02K-W1/2 selection criteria. When bit 3 is set (1), bits 5 to 8 define the ST25DV02K-W1/2 Inventory parameters.

Table 48. Definition of request flags 1 to 4

Bit No	Flag	Level	Description
Bit 1	Subcarrier_flag (1)	0	A single subcarrier frequency is used by the ST25DV02K-W1/2
		1	Two subcarriers are used by the ST25DV02K-W1/2
Bit 2	Data_rate_flag (2)	0	Low data rate is used
		1	High data rate is used
Bit 3	Inventory_flag	0	The meaning of flags 5 to 8 is described in Table 49. Request flags 5 to 8 when inventory_flag, Bit 3 = 0
		1	The meaning of flags 5 to 8 is described in Table 50. Request flags 5 to 8 when inventory_flag, Bit 3 = 1
Bit 4	Protocol_extension_flag	0	No Protocol format extension
		1	Protocol format extension. Reserved for future use.

1. *Subcarrier_flag refers to the ST25DV02K-W1/2-to-VCD communication.*
2. *Data_rate_flag refers to the ST25DV02K-W1/2-to-VCD communication.*

Table 49. Request flags 5 to 8 when inventory_flag, Bit 3 = 0

Bit nb	Flag	Level	Description
Bit 5	Select flag (1)	0	The request is executed by any ST25DV02K-W1/2 according to the setting of Address_flag
		1	The request is executed only by the ST25DV02K-W1/2 in Selected state
Bit 6	Address flag	0	The request is not addressed. UID field is not present. The request is executed by all ST25DV02K-W1/2s.
		1	The request is addressed. UID field is present. The request is executed only by the ST25DV02K-W1/2 whose UID matches the UID specified in the request.
Bit 7	Option flag	0	Option not activated.
		1	Option activated.
Bit 8	RFU	0	-

1. *If the Select_flag is set to 1, the Address_flag is set to 0 and the UID field is not present in the request.*

Table 50. Request flags 5 to 8 when inventory_flag, Bit 3 = 1

Bit nb	Flag	Level	Description
Bit 5	AFI flag	0	AFI field is not present
		1	AFI field is present
Bit 6	Nb_slots flag	0	16 slots
		1	1 slot
Bit 7	Option flag	0	-
Bit 8	RFU	0	-

6.2.6 Response format

The response consists of:

- an SOF,
- flags,
- parameters and data,
- a CRC,
- an EOF.

Table 51. **General response format**

SOF	Response_flags	Parameters	Data	2 byte CRC	EOF

6.2.7 Response flags

Table 52. **Definitions of response flags 1 to 8**

Bit Nb	Flag	Level	Description
Bit 1	Error_flag	0	No error
		1	Error detected. Error code is in the “Error” field.
Bit 2	RFU	0	-
Bit 3	RFU	0	-
Bit 4	RFU	0	-
Bit 5	RFU	0	-
Bit 6	RFU	0	-
Bit 7	RFU	0	-
Bit 8	RFU	0	-

In a response, the flags indicate how actions have been performed by the ST25DV02K-W1/2 and whether corresponding fields are present or not. The response flags consist of eight bits.

6.2.8 Response and error code

If the Error_flag is set by the ST25DV02K-W1/2 in the response, the Error code field is present and provides information about the error that occurred.

Error codes not specified in Table 53. Response error code definition are reserved for future use.

Table 53. **Response error code definition**

Error code	Meaning
01h	Command is not supported.
02h	Command is not recognized (format error).
03h	The option is not supported.
0Fh	Error with no information given.
10h	The specified block is not available.
11h	The specified block is already locked and thus cannot be locked again.
12h	The specified block is locked and its contents cannot be changed.
13h	The specified block was not successfully programmed.
14h	The specified block was not successfully locked.
15h	The specified block is protected in read.
No response	It could indicate illegal programming.

6.3 Timing definition

t_1: VICC response delay

Upon detection of the rising edge of the EOF received from the VCD, the ST25DV02K-W1/2 waits for a t_{1nom} time before transmitting its response to a VCD request or switching to the next slot during an inventory process. Values of t_1 are given in Table 54. Timing values.

t_2: VCD new request delay

t_2 is the time after which the VCD may send an EOF to switch to the next slot when one or more ST25DV02K-W1/2 responses have been received during an Inventory command. It starts from the reception of the EOF from the ST25DV02K-W1/2s.

The EOF sent by the VCD may be either 10% or 100% modulated regardless of the modulation index used for transmitting the VCD request to the ST25DV02K-W1/2.

t_2 is also the time after which the VCD may send a new request to the ST25DV02K-W1/2, as described in Figure 11. ST25DV02K-W1/2 protocol timing.

Values of t_2 are given in Table 54. Timing values.

t_3: VCD new request delay when no response is received from the VICC

t_3 is the time after which the VCD may send an EOF to switch to the next slot when no ST25DV02K-W1/2 response has been received.

The EOF sent by the VCD may be either 10% or 100% modulated regardless of the modulation index used for transmitting the VCD request to the ST25DV02K-W1/2.

From the time the VCD has generated the rising edge of an EOF:

- If this EOF is 100% modulated, the VCD waits for a time at least equal to t_{3min} for 100% modulation before sending a new EOF.
- If this EOF is 10% modulated, the VCD waits for a time at least equal to t_{3min} for 10% modulation before sending a new EOF.

Table 54. Timing values

	Minimum (min) values		Nominal (nom) values	Maximum (max) values
	100% modulation	10% modulation		
t_1	4320 / f_c = 318.6 µs		4352 / f_c = 320.9 µs	4384 / f_c = 323.3 µs (1)
t_2	4192 / f_c = 309.2 µs		No t_{nom}	No t_{max}
t_3	t_{1max} (2)+ t_{SOF} (3)	t_{1max}(2) + t_{NRT} (4) + t_{2min}	No t_{nom}	No t_{max}

1. *VCD request will not be interpreted during the first milliseconds following the field rising.*
2. *t_{1max} does not apply for write-alike requests. Timing conditions for write-alike requests are defined in the command description.*
3. *t_{SOF} is the time taken by the ST25DV02K-W1/2 to transmit an SOF to the VCD. t_{SOF} depends on the current data rate: High data rate or Low data rate.*
4. *t_{NRT} is the nominal response time of the ST25DV02K-W1/2. t_{NRT} depends on VCD to ST25DV02K-W1/2 data rate and subcarrier modulation mode.*

Note: The tollerance of specific timing is ± 32/f_C.

6.4 RF commands

The ST25DV02K-W1/2 supports the following RF command set:

- **Inventory**, used to perform the anticollision sequence.
- **Stay Quiet**, used to put the ST25DV02K-W1/2 in quiet mode, where it does not respond to any inventory command.
- **Read Single Block**, used to output the 32 bit of the selected block and its locking status.
- **Write Single Block**, used to write and verify the new content for an update of a 32 bit block, provided that it is not in a locked memory area.
- **Lock Block**, used to write the blocks security status bits (protect against writing).
- **Read Multiple Blocks**, used to read the selected blocks in a unique area, and send back their value.
- **Select**, used to select the ST25DV02K-W1/2. After this command, the ST25DV02K-W1/2 processes all Read/Write commands with Select_flag set.
- **Reset to Ready**, used to put the ST25DV02K-W1/2 in the ready state.
- **Write AFI**, used to write the 8-bit value in the AFI register.
- **Lock AFI**, used to lock the AFI register.
- **Write DSFID**, used to write the 8-bit value in the DSFID register.
- **Lock DSFID**, used to lock the DSFID register.
- **Get System information**, used to provide the standard system information values.
- **Get multiple block security status**, used to send the security status of the selected block.
- **Read Configuration**, used to read configuration registers.
- **Write Configuration**, used to write configuration registers.
- **Write Password**, used to change password of an opened security session.
- **Present Password**, used to present a password and to open a security session.

Their codes are given in Table 55. Command codes.

Table 55. Command codes

Command code	Function	Command code	Function
01h	Inventory	28h	Lock AFI
02h	Stay Quiet	29h	Write DSFID
20h	Read Single Block	2Ah	Lock DSFID
21h	Write Single Block	2Bh	Get System Info
22h	Lock Block	2Ch	Get Multiple Block Security Status
23h	Read Multiple Blocks	A0h	Read Configuration
25h	Select	A1h	Write Configuration
26h	Reset to Ready	B1h	Write Password
27h	Write AFI	B3h	Present Password

Following paragraphs describe the expected behaviour for each valid command.

In case of an invalid command, in a general manner, the ST25DV02K-W1 ST25DV02K-W2 behaves as follow:

1. If flag usage is incorrect, the error code 03h is issued only if the right UID is used in the command, otherwise no response will be issued.
2. The code error 02h is issued if the custom command is used with the manufacturer code different from the ST one

6.4.1 Inventory

Upon receiving the Inventory request, the ST25DV02K-W1/2 runs the anticollision sequence. The Inventory_flag is set to 1. The meaning of flags 5 to 8 is shown in Table 50. Request flags 5 to 8 when inventory_flag, Bit 3 = 1.

- The Request flags
- the Inventory command code (001)
- AFI if the AFI flag is set
- Mask length
- Mask value if mask length is different from 0
- the CRC

The ST25DV02K-W1/2 does not generate any answer in case of error.

Table 56. Inventory request format

Request SOF	Request_flags	Inventory	Optional AFI	Mask length	Mask value	CRC16	Request EOF
-	8 bits	01h	8 bits	8 bits	0 - 64 bits	16 bits	-

The response contains:

- the flags
- the Unique ID

Table 57. Inventory response format

Response SOF	Response_flags	DSFID	UID	CRC16	Response EOF
-	8 bits	8 bits	64 bits	16 bits	-

During an Inventory process, if the VCD does not receive an RF ST25DV02K-W1/2 response, it waits for a time t_3 before sending an EOF to switch to the next slot. t_3 starts from the rising edge of the request EOF sent by the VCD.

- If the VCD sends a 100% modulated EOF, the minimum value of t_3 is:

  $t_3min = 4384/f_C$ (323.3µs) + t_{SOF}
- If the VCD sends a 10% modulated EOF, the minimum value of t_3 is:

  $t_3min = 4384/f_C$ (323.3µs) + t_{NRT} + t_{2min}

where:

- t_{SOF} is the time required by the ST25DV02K-W1/2 to transmit an SOF to the VCD,
- t_{NRT} is the nominal response time of the ST25DV02K-W1/2.

t_{NRT} and t_{SOF} are dependent on the ST25DV02K-W1/2-to-VCD data rate and subcarrier modulation mode.

Note: In case of error, no response is sent by ST25DV02K-W1 ST25DV02K-W2.

6.4.2 Stay Quiet

On receiving the Stay Quiet command, the ST25DV02K-W1/2 enters the Quiet state if no error occurs, and does NOT send back a response. There is NO response to the Stay Quiet command even if an error occurs. The Option_flag is not supported. The Inventory_flag must be set to 0.

When in the Quiet state:

- the ST25DV02K-W1/2 does not process any request if the Inventory_flag is set,
- the ST25DV02K-W1/2 processes any request with Address_flag set.

The ST25DV02K-W1/2 exits the Quiet state when:

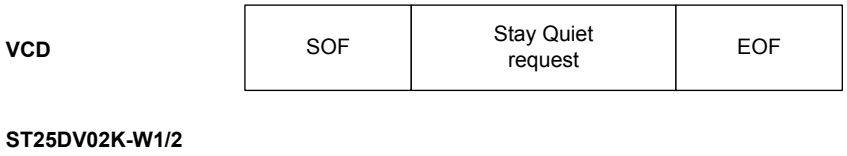
- it is reset (power off),
- receiving a Select request. It then goes to the Selected state,
- receiving a Reset to Ready request. It then goes to the Ready state.

Table 58. Stay Quiet request format

Request SOF	Request flags	Stay Quiet	UID	CRC16	Request EOF
-	8 bits	02h	64 bits	16 bits	-

The Stay Quiet command must always be executed in Addressed mode (Select_flag is reset to 0 and Address_flag is set to 1).

Figure 13. Stay Quiet frame exchange between VCD and ST25DV02K-W1/2



6.4.3 Read Single Block

On receiving the Read Single Block command, the ST25DV02K-W1/2 reads the requested block and sends back its 32-bit value in the response. The Option_flag is supported, when set response include the Block Security Status. The Inventory_flag must be set to 0.

Block number is coded on 1 Byte.

Table 59. Read Single Block request format

Request SOF	Request_flags	Read Single Block	UID (1)	Block number	CRC16	Request EOF
-	8 bits	20h	64 bits	8 bits	16 bits	-

1. *The field is optional.*

Request parameters:

- Request flags
- UID (optional)
- Block number

Table 60. Read Single Block response format when Error_flag is NOT set

Response SOF	Response_flags	Block security status (1)	Data	CRC16	Response EOF
-	8 bits	8 bits	32 bits	16 bits	-

1. *The field is optional.*

Response parameters:

- Block security status if Option_flag is set (see Table 61. Block security status)
- Four bytes of block data

Table 61. Block security status

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Reserved for future use. All at 0.							0: Current block not locked 1: Current block locked

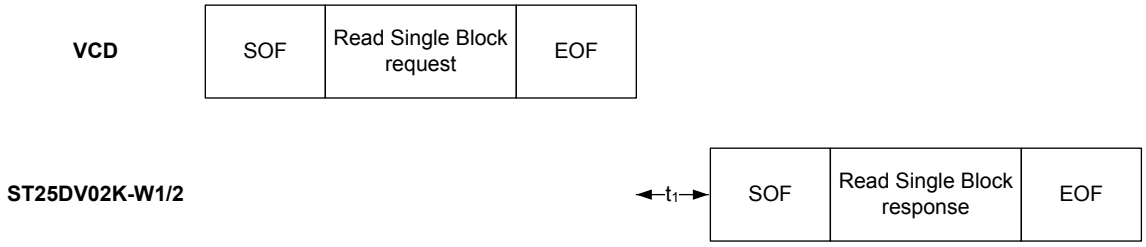
Table 62. Read Single Block response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 03h: command option not supported
  - 0Fh: error with no information
  - 10h: the specified block is not available
  - 15h: the specified block is read-protected

Figure 14. Read Single Block frame exchange between VCD and ST25DV02K-W1/2



6.4.4 Write Single Block

On receiving the Write Single Block command, the ST25DV02K-W1/2 writes the data contained in the request to the targeted block and reports whether the write operation was successful in the response. When the Option_flag is set, wait for EOF to respond. The Inventory_flag must be set to 0.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the ST25DV02K-W1/2 may not program correctly the data into the memory. Block number is coded on 1 Byte.

Table 63. Write Single Block request format

Request SOF	Request_flags	Write Single Block	UID (1)	Block number	Data	CRC16	Request EOF
-	8 bits	21h	64 bits	8 bits	32 bits	16 bits	-

1. *The field is optional.*

Request parameters:

- Request flags
- UID (optional)
- Block number
- Data

Table 64. Write Single Block response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter. The response is sent back after the writing cycle.

Table 65. Write Single Block response format when Error_flag is set

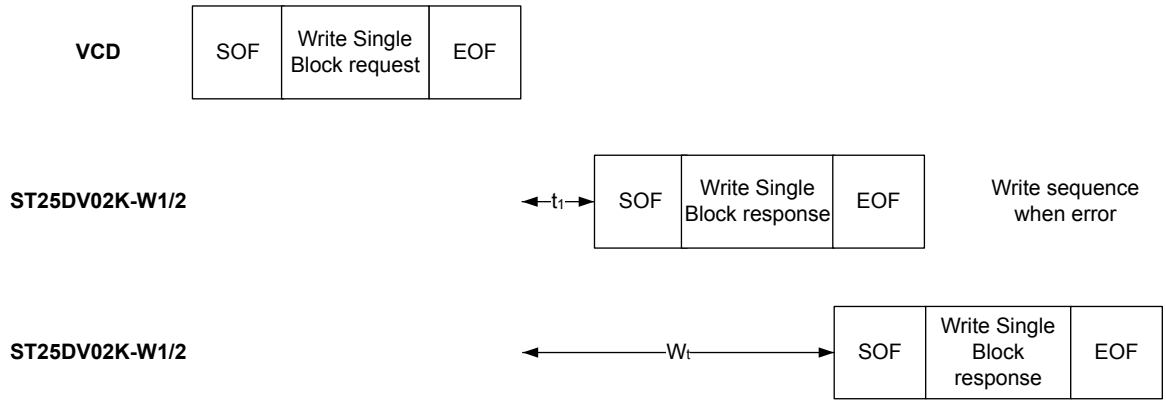
Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set(1)
  - 03h: command option not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available
  - 12h: the specified block is locked or protected and its contents cannot be changed
  - 13h: the specified block was not successfully programmed

1. *For more details, see Figure 5. Memory organization.*

Figure 15. Write Single Block frame exchange between VCD and ST25DV02K-W1/2



6.4.5 Lock Block

On receiving the Lock block request, the ST25DV02K-W1/2 locks the corresponding block value permanently and protects its content against new writing.

Lock block command is applicable and successful, if and only if the block is not protected in Write (ie, the block is not already locked, or protected in Write by password).

The Option_flag is supported, when set wait for EOF to respond. The Inventory_flag must be set to 0.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the ST25DV02K-W1/2 may not lock correctly the block value in memory.

Table 66. Lock Block request format

Request SOF	Request_flags	Lock block	UID (1)	block number	CRC16	Request EOF
-	8 bits	22h	64 bits	8 bits	16 bits	-

1. *The field is optional.*

Request parameter:

- Request Flags
- UID (optional)
- Block number

Table 67. Lock block response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

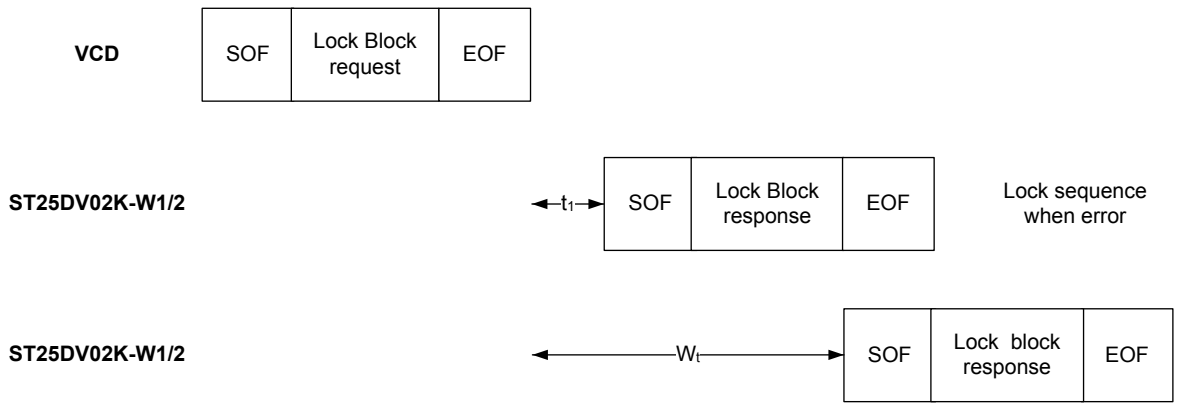
Table 68. Lock single block response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 03h: command option not supported
  - 10h: block not available
  - 11h: the specified block is already locked and thus cannot be locked again
  - 14h: the specified block was not successfully locked

Figure 16. Lock single block frame exchange between VCD and ST25DV02K-W1/2



6.4.6 Read Multiple Blocks

When receiving the Read Multiple Block command, the ST25DV02K-W1/2 reads the selected blocks and sends back their value in multiples of 32 bits in the response. The blocks are numbered from 00h to FFh in the request and the value is minus one (-1) in the field. For example, if the “Number of blocks” field contains the value 06h, seven blocks are read. If the number of blocks overlaps areas, the ST25DV02K-W1/2 returns an error code. When the Option_flag is set, the response returns the Block Security Status. The Inventory_flag must be set to 0.

Block number is coded on 1 byte.

Table 69. Read Multiple Block request format

Request SOF	Request_flags	Read Multiple Block	UID (1)	First block number	Number of blocks	CRC16	Request EOF
-	8 bits	23h	64 bits	8 bits	8 bits	16 bits	-

1. *The field is optional.*

Request parameters:

- Request flags
- UID (optional)
- First block number
- Number of blocks

Table 70. Read Multiple Block response format when Error_flag is NOT set

Response SOF	Response_ flags	Block security status (1)	Data	CRC16	Response EOF
-	8 bits	8 bits (2)	32 bits(2)	16 bits	-

1. *The field is optional.*
2. *Repeated as needed.*

Response parameters:

- Block security status if Option_flag is set (see Table 71)
- N blocks of data

Table 71. Block security status

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Reserved for future use. All at 0.							0: Current block not locked 1: Current block locked

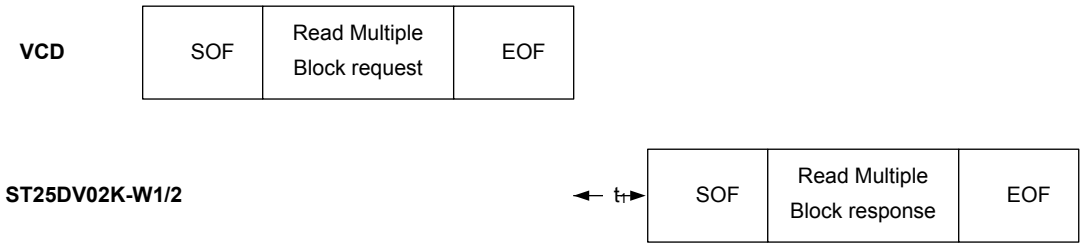
Table 72. Read Multiple Block response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: command option is not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available
  - 15h: the specified block is read-protected

Figure 17. Read Multiple Block frame exchange between VCD and ST25DV02K-W1/2



6.4.7 Select

When receiving the Select command:

- If the UID is equal to its own UID, the ST25DV02K-W1/2 enters or stays in the Selected state and sends a response.
- If the UID does not match its own UID, the selected ST25DV02K-W1/2 returns to the Ready state and does not send a response.

The ST25DV02K-W1/2 answers an error code only if the UID is equal to its own UID. If not, no response is generated. If an error occurs, the ST25DV02K-W1/2 remains in its current state. The Option_flag is not supported. The Inventory_flag must be set to 0.

Table 73. Select request format

Request SOF	Request_flags	Select	UID	CRC16	Request EOF
-	8 bits	25h	64 bits	16 bits	-

Request parameter:

- Request flags
- UID

Table 74. Select Block response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

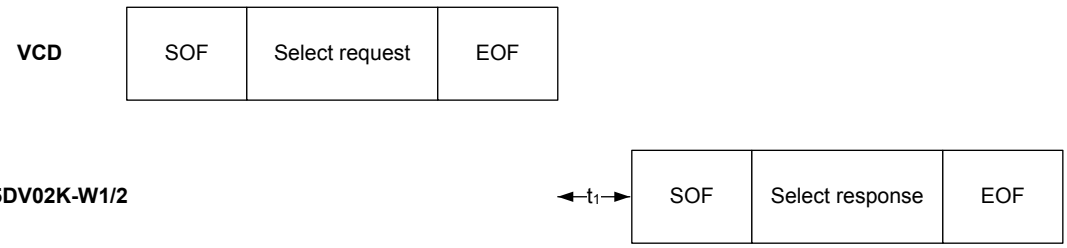
Table 75. **Select response format when Error_flag is set**

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 0Fh: error with no information given

Figure 18. **Select frame exchange between VCD and ST25DV02K-W1/2**



6.4.8 Reset to Ready

On receiving a Reset to Ready command, the ST25DV02K-W1/2 returns to the Ready state if no error occurs. In the Addressed mode, the ST25DV02K-W1/2 answers an error code only if the UID is equal to its own UID. If not, no response is generated.The Option_flag is not supported. The Inventory_flag must be set to 0.

Table 76. **Reset to Ready request format**

Request SOF	Request_flags	Reset to Ready	UID (1)	CRC16	Request EOF
-	8 bits	26h	64 bits	16 bits	-

1. *The field is optional.*

Request parameter:

- Request flags
- ID (optional)

Table 77. **Reset to Ready response format when Error_flag is NOT set**

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

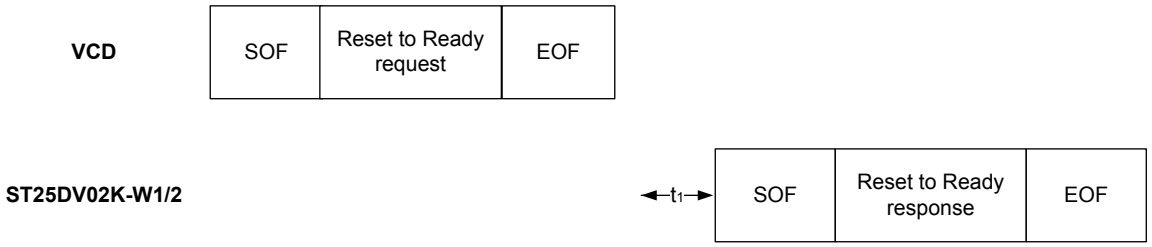
Table 78. **Reset to ready response format when Error_flag is set**

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 0Fh: error with no information given

Figure 19. **Reset to Ready frame exchange between VCD and ST25DV02K-W1/2**



6.4.9 Write AFI

On receiving the Write AFI request, the ST25DV02K-W1/2 programs the 8-bit AFI value to its memory. When the Option_flag is set, wait for EOF to respond. The Inventory_flag must be set to 0.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the ST25DV02K-W1/2 may not write correctly the AFI value into the memory.

Table 79. **Write AFI request format**

Request SOF	Request_flags	Write AFI	UID (1)	AFI	CRC16	Request EOF
-	8 bits	27h	64 bits	8 bits	16 bits	-

1. *The field is optional.*

Request parameter:

- Request flags
- UID (optional)
- AFI

Table 80. **Write AFI response format when Error_flag is NOT set**

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

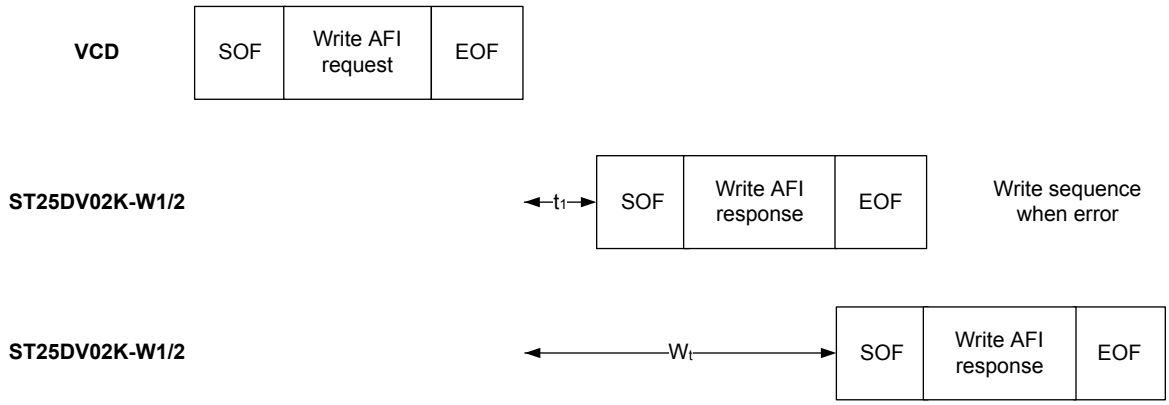
Table 81. **Write AFI response format when Error_flag is set**

Response SOF	Response_ flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 03h: command option is not supported
  - 0Fh: error with no information given
  - 12h: the specified block is locked and its contents cannot be changed
  - 13h: the specified block was not successfully programmed

Figure 20. **Write AFI frame exchange between VCD and ST25DV02K-W1/2**



6.4.10 Lock AFI

On receiving the Lock AFI request, the ST25DV02K-W1/2 locks the AFI value permanently. When the Option_flag is set, wait for EOF to respond.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the ST25DV02K-W1/2 may not lock correctly the AFI value in memory. The Inventory_flag must be set to 0.

Table 82. **Lock AFI request format**

Request SOF	Request_flags	Lock AFI	UID (1)	CRC16	Request EOF
-	8 bits	28h	64 bits	16 bits	-

1. *The field is optional.*

Request parameter:

- Request Flags
- UID (optional)

Table 83. **Lock AFI response format when Error_flag is NOT set**

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

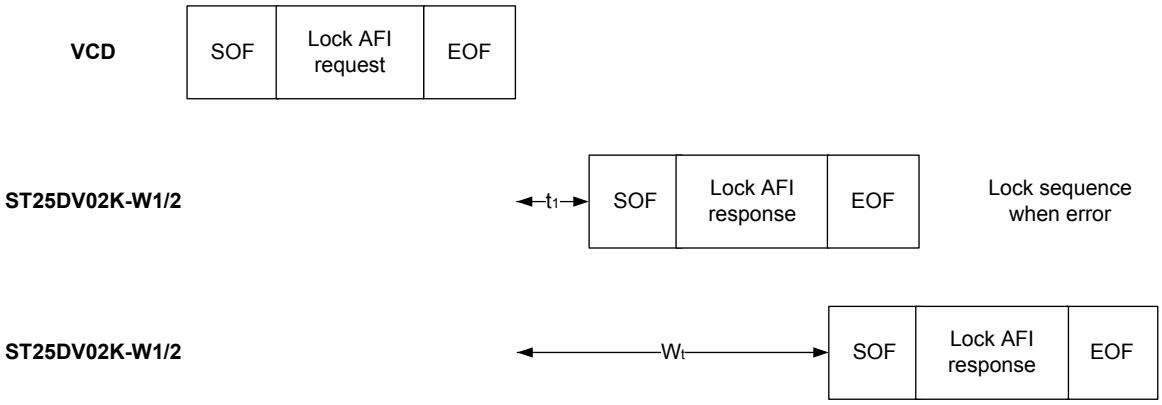
Table 84. Lock AFI response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 03h: command option is not supported
  - 0Fh: error with no information given
  - 11h: the specified block is already locked and thus cannot be locked again
  - 14h: the specified block was not successfully locked

Figure 21. Lock AFI frame exchange between VCD and ST25DV02K-W1/2



6.4.11 Write DSFID

On receiving the Write DSFID request, the ST25DV02K-W1/2 programs the 8-bit DSFID value to its memory. When the Option_flag is set, wait for EOF to respond. The Inventory_flag must be set to 0.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the ST25DV02K-W1/2 may not write correctly the DSFID value in memory.

Table 85. Write DSFID request format

Request SOF	Request_flags	Write DSFID	UID (1)	DSFID	CRC16	Request EOF
-	8 bits	29h	64 bits	8 bits	16 bits	-

1. *The field is optional.*

Request parameter:

- Request flags
- UID (optional)
- DSFID

Table 86. Write DSFID response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter

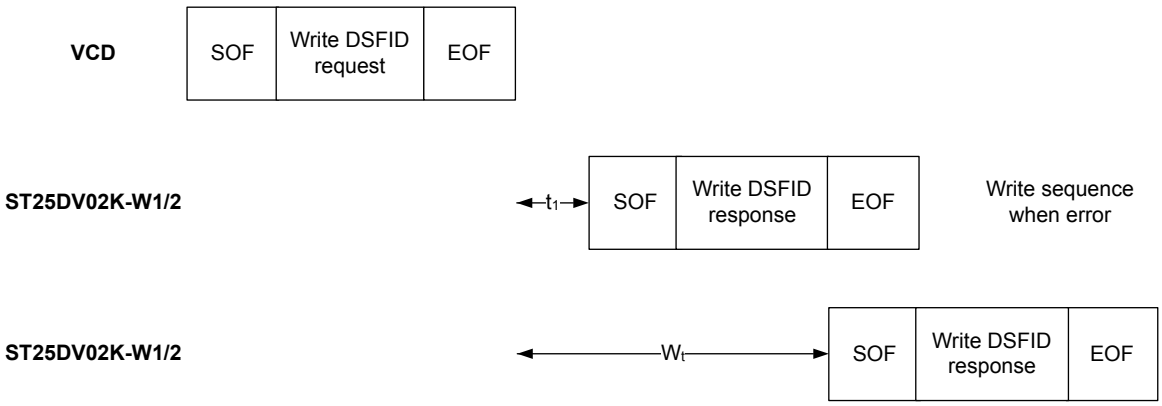
Table 87. Write DSFID response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 03h: command option is not supported
  - 0Fh: error with no information given
  - 12h: the specified block is locked and its contents cannot be changed
  - 13h: the specified block was not successfully programmed

Figure 22. Write DSFID frame exchange between VCD and ST25DV02K-W1/2



6.4.12 Lock DSFID

On receiving the Lock DSFID request, the ST25DV02K-W1/2 locks the DSFID value permanently. When the Option_flag is set, wait for EOF to respond. The Inventory_flag must be set to 0."

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the ST25DV02K-W1/2 may not lock correctly the DSFID value in memory.

Table 88. Lock DSFID request format

Request SOF	Request_flags	Lock DSFID	UID (1)	CRC16	Request EOF
-	8 bits	2Ah	64 bits	16 bits	-

1. *The field is optional.*

Request parameter:

- Request flags
- UID (optional)

Table 89. Lock DSFID response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter.

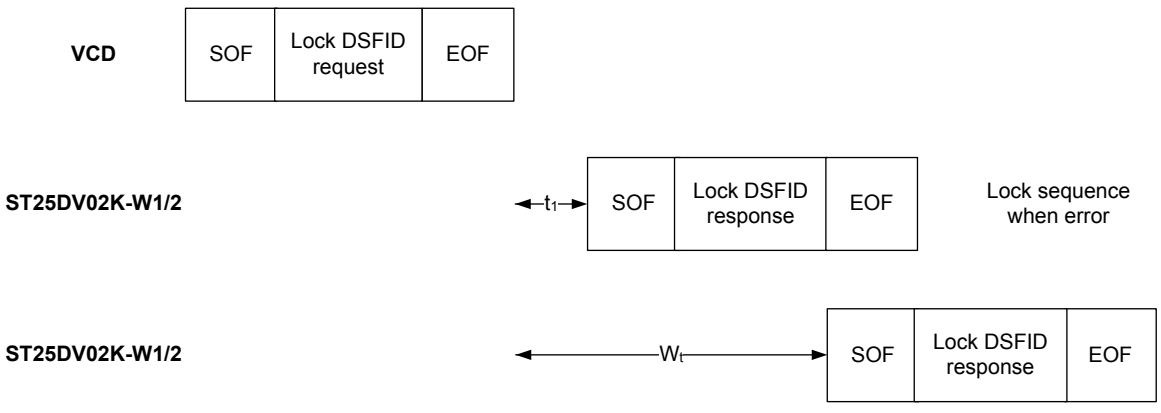
Table 90. Lock DSFID response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: command option is not supported
  - 0Fh: error with no information given
  - 11h: the specified block is already locked and thus cannot be locked again
  - 14h: the specified block was not successfully locked

Figure 23. Lock DSFID frame exchange between VCD and ST25DV02K-W1/2



6.4.13 Get System Info

When receiving the Get System Info command, the ST25DV02K-W1/2 sends back its information data in the response. The Option_flag is not supported. The Get System Info can be issued in both Addressed and Non Addressed modes. The Inventory_flag must be set to 0.

Table 91. Get System Info request format

Request SOF	Request_flags	Get System Info	UID (1)	CRC16	Request EOF
-	8 bits	2Bh	64 bits	16 bits	-

1. *The field is optional.*

Request parameter:

- Request flags
- UID (optional)

Table 92. Get System Info response format Error_flag is NOT set

Response SOF	Response flags	Information flags	UID	DSFID	AFI	Memory size	IC ref.	CRC16	Response EOF
-	00h	0Fh	64 bits	8 bits	8 bits	033Fh	8 bits	16 bits	-

Response parameters:

- Information flags set to 0Fh. DSFID, AFI and IC reference fields are present.
- UID code on 64 bits
- DSFID value
- AFI value
- Memory Size on 16 bits:
  - 8-MSB = Block size in number of Bytes
  - 8-LSB = User Data size in number of Blocks
- ST25DV02K-W1/2 IC reference: the 8 bits are significant.

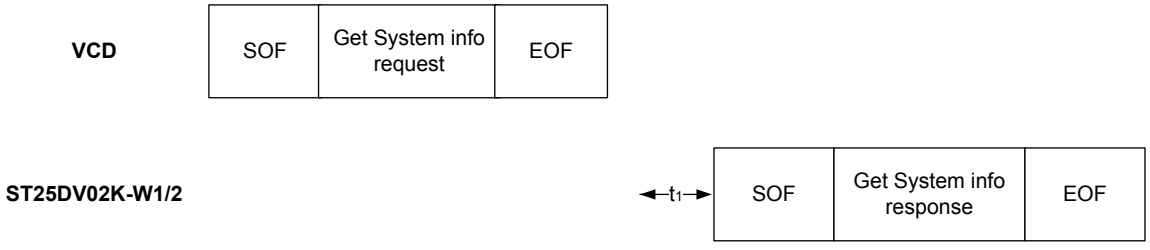
Table 93. Get System Info response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	01h	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: Option not supported
  - 0Fh: error with no information given

Figure 24. Get System Info frame exchange between VCD and ST25DV02K-W1/2



6.4.14 Get Multiple Block Security Status

When receiving the Get Multiple Block Security Status command, the ST25DV02K-W1/2 sends back its security status for each address block: 0 when block is writable else 1 when block is locked for writing. The blocks security status are defined by the area security status (and the lock block status). The blocks are numbered from 00h up to the maximum memory block number in the request, and the value is minus one (–1) in the field. For example, a value of “06” in the “Number of blocks” field requests will return the security status of seven blocks. This command does not respond an error if number of blocks overlap areas.

The number of blocks is coded on 1 Byte. The Option_flag is not supported. The Inventory_flag must be set to 0.

Table 94. Get Multiple Block Security Status request format

Request SOF	Request_flags	Get Multiple Block Security Status	UID (1)	First block number	Number of blocks	CRC16	Request EOF
-	8 bits	2Ch	64 bits	8 bits	8 bits	16 bits	-

1. *The field is optional.*

Request parameter:

- Request flags
- UID (optional)
- First block number
- Number of blocks

Table 95. Get Multiple Block Security Status response format when Error_flag is NOT set

Response SOF	Response_flags	Block security status	CRC16	Response EOF
-	8 bits	8 bits (1)	16 bits	-

1. *Repeated as needed.*

Response parameters:

- Block security status

Table 96. Block security status

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Reserved for future use All at 0							0: Current block not locked 1: Current block locked

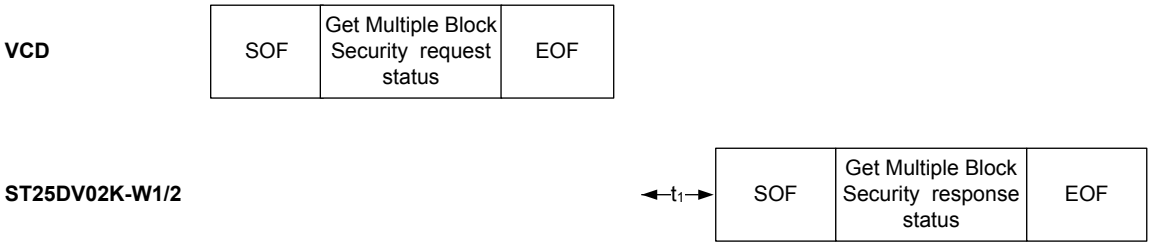
Table 97. Get Multiple Block Security Status response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available

Figure 25. Get Multiple Block Security Status frame exchange between VCD and ST25DV02K-W1/2



6.4.15 Read Configuration

On receiving the Read Configuration command, the ST25DV02K-W1/2 reads the static system configuration register at the Pointer address and sends back its 8-bit value in the response.

The Option_flag is not supported. The Inventory_flag must be set to 0.

Table 98. Read Configuration request format

Request SOF	Request_flags	Read Configuration	IC Mfg code	UID (1)	Pointer	CRC16	Request EOF
-	8 bits	A0h	02h	64 bits	8 bits	16 bits	-

1. *The field is optional.*

Note: Refer to Table 4. System configuration memory map for details on register addresses.

Request parameters:

- System configuration register pointer
- UID (optional)

Table 99. Read Configuration response format when Error_flag is NOT set

Response SOF	Response_flags	Register value	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameters:

- One byte of data: system configuration register

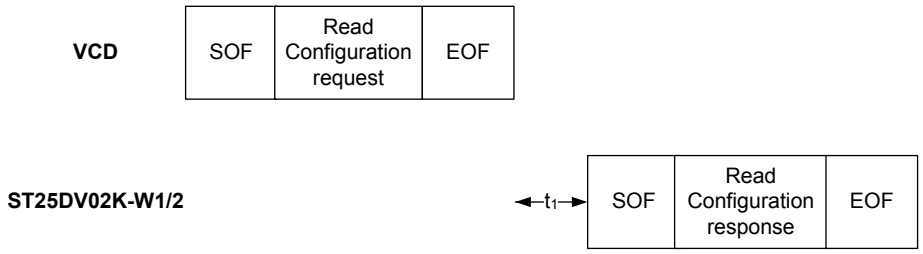
Table 100. Read Configuration response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set
  - 02h: command not recognized
  - 03h: the option is not supported
  - 10h: block not available
  - 0Fh: error with no information given

Figure 26. **Read Configuration frame exchange between VCD and ST25DV02K-W1/2**



6.4.16 Write Configuration

The Write Configuration command is used to write system configuration register. The Write Configuration must be preceded by a valid presentation of the configuration password (03h) to open the configuration security session.

On receiving the Write Configuration command, the ST25DV02K-W1/2 writes the data contained in the request to the system configuration register at the Pointer address and reports whether the write operation was successful in the response or not.

When the Option_flag is set, wait for EOF to respond. The Inventory_flag is not supported.

During the RF write cycle W_t, there should be no modulation (neither 100% nor 10%), otherwise the ST25DV02K-W1/2 may not program correctly the data into the Configuration byte.

Table 101. **Write Configuration request format**

Request SOF	Request_ flags	Write Configuration	IC Mfg code	UID (1)	Pointer	Register Value (2)	CRC16	Request EOF
-	8 bits	A1h	02h	64 bits	8 bits	8 bits	16 bits	-

1. *The field is optional.*
2. *Before updating the register value, check the meaning of each bit in previous sections.*

Request parameters:

- Request flags
- Register pointer
- Register value
- UID (optional)

Table 102. **Write Configuration response format when Error_flag is NOT set**

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Note: Please refer to Table 4. System configuration memory map for details on register addresses.

Response parameter:

- No parameter. The response is sent back after the writing cycle.

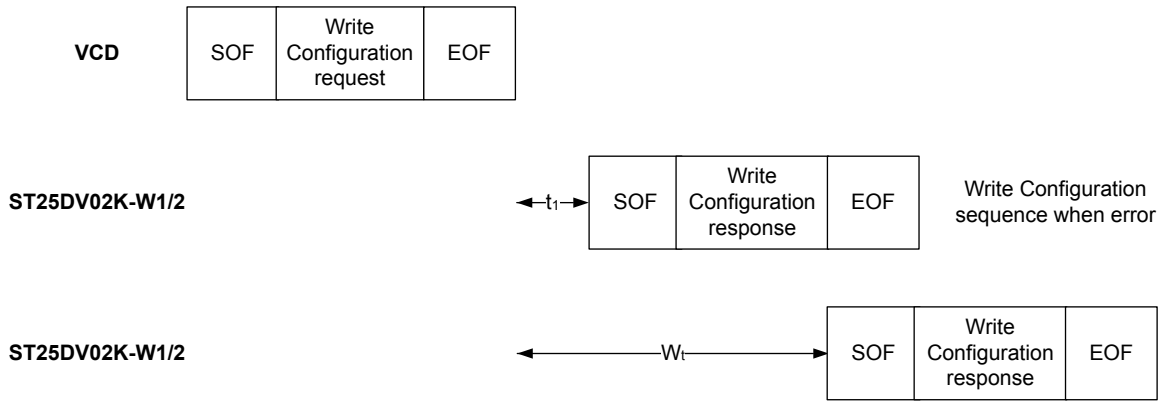
Table 103. **Write Configuration response format when Error_flag is set**

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 02h: command not recognized
  - 03h: command option is not supported
  - 0Fh: error with no information given
  - 10h: block not available
  - 12h: block already locked, content can't change
  - 13h: the specified block was not successfully programmed

Figure 27. Write Configuration frame exchange between VCD and ST25DV02K-W1/2



6.4.17 Write Password

On receiving the Write Password command, the ST25DV02K-W1/2 uses the data contained in the request to write the password and reports whether the operation was successful in the response. It is possible to modify a Password value only after issuing a valid Present password command (of the same password number). When the Option_flag is set, wait for EOF to respond. Refer to Section 5.2 Data protection for details on password Management. The Inventory_flag must be set to 0.

After a successful write, the new value of the selected password is automatically activated.

Write Password command always applies on 32-bits password. When Area1 & Area2 are merged, the corresponding password is 64-bits length. In that case 2x independent Write Password commands are required to update the 64-bits equivalent password. Such update can be done in any order. Moreover only one of the 2x 32-bits password can be changed, the other password keeping its previous value.

Note: During the RF write cycle time, Wt, there must be no modulation (neither 100% nor 10%), otherwise the ST25DV02K-W1/2 may not correctly program the data into the memory.

There is no anti-tearing mechanism during Write_Password command. For this reason, the RF Field must be stable and V_{CC} state (either ON or OFF) remains constant, during the whole Write_Password command. If those conditions are not ensured, the command may not complete properly, and could imply a loss/corruption of password content, with no recovery capability.

It is recommended to use Write_Password command in Addressed or Selected modes, in order to improve the system robustness. This allows to ensure that Password change is only applied to the concerned tag/UID.

Table 104. Write Password request format

Request SOF	Request_flags	Write password	IC Mfg code	UID (1)	Password number	Data	CRC16	Request EOF
-	8 bits	B1h	02h	64 bits	8 bits	32 bits	16 bits	-

1. *The field is optional.*

Request parameter:

- Request flags
- UID (optional)
- Password number:
  - 00h = PWD_PWM
  - 01h = PWD_AREA1
  - 02h = PWD_AREA2
  - 03h = PWD_CFG
  - other = Error
- Data

Table 105. Write Password response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- no parameter.

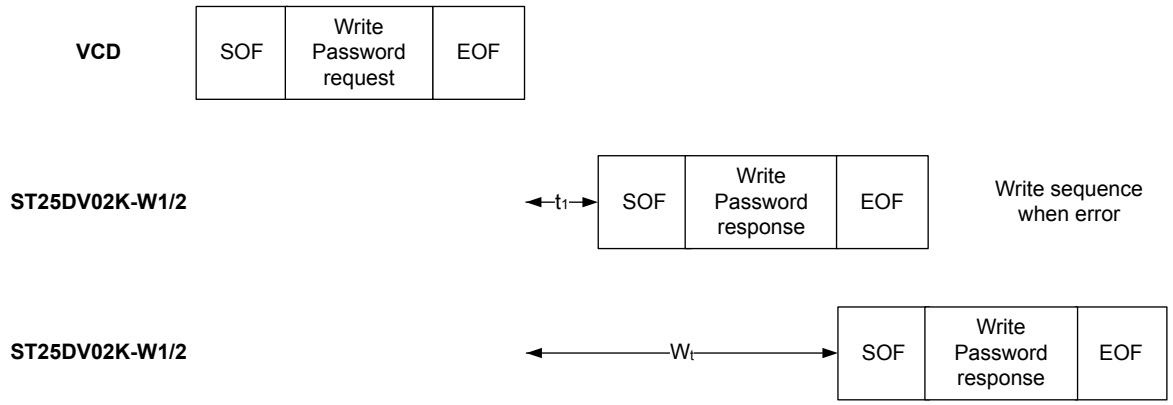
Table 106. Write Password response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 02h: command not recognized
  - 03h: command option not supported
  - 10h: the password number is incorrect
  - 12h: right not granted, previous Present_Password command not successfully
  - 13h: the specified block was not successfully programmed

Figure 28. Write Password frame exchange between VCD and ST25DV02K-W1/2



6.4.18 Present Password

On receiving the Present Password command, the ST25DV02K-W1/2 compares the requested password with the data contained in the request and reports if the operation has been successful in the response. Refer to Section 5.2 Data protection for details on password Management. After a successful command, the security session associated to the password is open as described in Section 5.2 Data protection. The Option_flag is not supported. The Inventory_flag must be set to.

Table 107. Present Password request format

Request SOF	Request_flags	Present Password	IC Mfg code	UID (1)	Password number	Password	CRC16	Request EOF
-	8 bits	B3h	02h	64 bits	8 bits	32 or 64 bits (2)	16 bits	-

1. *The field is optional.*
2. *64 bits password length only applies when AREA1 & AREA2 are merged in a single AREA.*

Request parameter:

- Request flags
- UID (optional)
- Password Number:
  - 00h: PWD_PWM --> 32-bits password,
  - 01h: PWD_AREA1 --> 32-bits password,
  - 01h: PWD_64 --> 64-bits password, in case of merged AREA1+AREA2,
  - 02h: PWD_AREA2 --> 32-bits password,
  - 03h: PWD_CFG --> 32-bits password,
  - Other: Error
- Password

Table 108. Present Password response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
-	8 bits	16 bits	-

Response parameter:

- No parameter. The response is sent back after the write cycle.

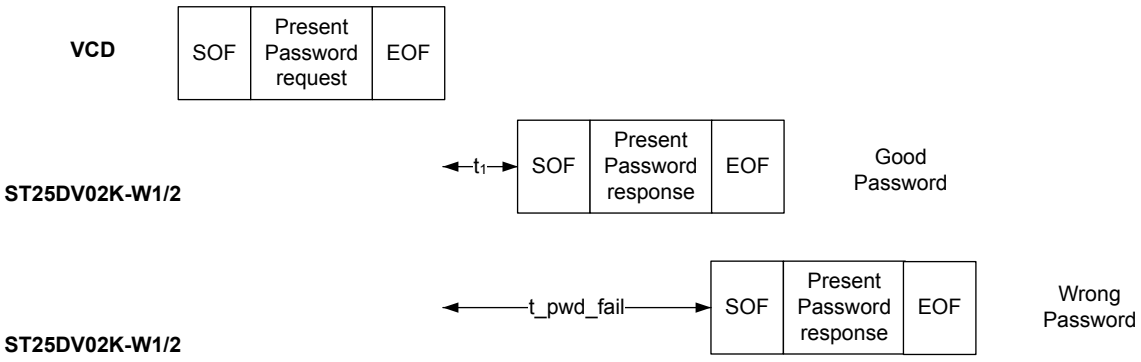
Table 109. Present Password response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
-	8 bits	8 bits	16 bits	-

Response parameter:

- Error code as Error_flag is set:
  - 02h: command not recognized
  - 03h: command option not supported
  - 0Fh: the present password is incorrect
  - 10h: the password number is incorrect

Figure 29. **Present Password frame exchange between VCD and ST25DV02K-W1/2**



7 Unique identifier (UID)

The ST25DV02K-W1/2 is uniquely identified by a 64-bit unique identifier (UID). This UID complies with ISO/IEC 15963 and ISO/IEC 7816-6. The UID is a read-only code and comprises:

- 8-bits with a value of E0h,
- the IC manufacturer code “ST 02h” on 8 bits (ISO/IEC 7816-6/AM1),
- a unique serial number on 48 bits.

Table 110. UID format

MSB				LSB
63 56	55 48	47 40	39 0	
0xE0	0x02	ST product code (1)	Unique serial number	

1. See *Table 44. UID access for ST product code value definition.*

With the UID, each ST25DV02K-W1/2 can be addressed uniquely and individually during the anticollision loop and for one-to-one exchanges between a VCD and an ST25DV02K-W1/2.

8 Device parameters

8.1 Maximum rating

Stressing the device above the rating listed in Table 111. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device, at these or any other conditions above those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 111. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
T_A	Ambient operating temperature	Range 6	- 40	85	°C
		Range 8	- 40	105	
T_{STG}	Storage temperature	SO8N, TSSOP8	-65	150	°C
T_{LEAD}	Lead temperature during soldering		(1)		°C
V_{MAX_1} (2)	RF input voltage amplitude peak to peak between AC0 and AC1, V_{SS} pin left floating	V_{AC0} - V_{AC1}	-	11	V
V_{MAX_2} (2)	AC voltage between AC0 and V_{SS}, or AC1 and V_{SS}	V_{AC0} - V_{SS} or V_{AC1} - V_{SS}	-0.5	5.5	V
V_{ESD}	Electrostatic discharge voltage (3) (human body model)	All pins	-	1.5	kV
V_{CC}	Power supply voltage range		-0.5	6.0	V
V_{PWM}	PWM output range		-0.5	6.0	V

1. *Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.*
2. *Based on characterization, not tested in production.*
3. *ANSI/ESDA/JEDEC JS-001-2012, C = 100 pF, R = 1500 Ω, R2 = 500 Ω)*

8.2 RF electrical parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device in RF mode.

The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 112. RF characteristics

Symbol	Parameter	Condition[1][2][3]	Min	Typ	Max	Unit
f_{CC}	External RF signal frequency	-	13.553	13.56	13.567	MHz
f_{SH}	Subcarrier frequency high	$f_{CC}/32$	-	423.75	-	kHz
f_{SL}	Subcarrier frequency low	$f_{CC}/28$	-	484.28	-	kHz
$MI_{CARRIER}$	10% carrier modulation index [4]	150 mA/m < H < 5 A/m	10	-	30	%
	100% carrier modulation index [5]		95	-	100	
t_{Boot_RF}	RF Boot time (minimum time from carrier generation to first data)	V_{CC} OFF, from $H_{FIELD\ MIN}$	-	-	1	ms
t_{RF_OFF}	RF OFF time	Chip reset	2	-	-	ms
t_1	Time for ST25DV02K-W1/2 response	-	318.6	320.9	323.3	µs
t_2	Time between commands	-	309	311.5	314	µs
t_3	Time before new EOF in case of no response	-	323.3	-	-	µs
W_t [6]	Time for Write operation (block/byte/bit)	1 Block	-	5.152	-	ms
t_{PWD_FAIL} [6]	Waiting time in case of wrong password	-	5.12	-	-	ms
C_{TUN} [5] [7]	Input capacitance	SO8N, f = 13.56 MHz	26.5	28.5	30.5	pF
V_{BACK}	ISO Backscattering minimum voltage	-	10	-	-	mV
T_{A-RF}	RF ambient operating temperature	-	-40	-	85	°C
V_{MIN_1} [4]	$(V_{AC0}-V_{AC1})_{Peak}$ = RF input voltage between AC0 and AC1. V_{SS} pin left floating	Write cmd, V_{CC} OFF	-	2.8	-	V_{PEAK}
V_{MIN_2} [4]	AC voltage between AC0 and V_{SS} or between AC1 and V_{SS}	Write cmd, V_{CC} OFF	-	2.6	-	V_{PEAK}
P_{MIN} [4] [8]	Minimum RF input power	Write cmd, V_{CC} OFF	-	120	-	µW
t_{RET}	Retention time	-	40	-	-	year
Cycling	Write cycles endurance	$T_A \leq 85$ °C	100 000	-	-	cycle

1. *T_A= -40 to 85 °C. Characterized only.*
2. *All timing characterizations were performed on a reference antenna with the following characteristics:*
   - *ISO antenna class1*
   - *Tuning frequency = 13.7 MHz*
3. *Measured with PWM OFF.*
4. *Characterized on bench.*
5. *Characterized at room temperature only, on wafer at POR Level.*
6. *Applies from VCD request EOF to V_{ICC} response SOF.*
7. *For design of reference antenna. Min and Max value are deduced from correlation with industrial tester limits.*
8. *Referenced at V_{SS}*

8.3 PWM electrical parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device related to PWM output.

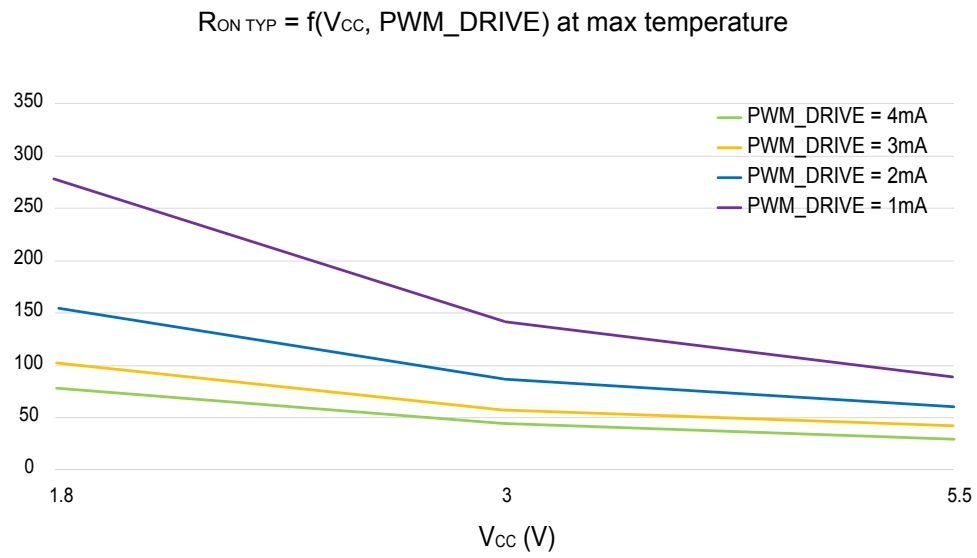
The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 113. PWM characteristics

Symbol	Parameter[1]	Condition[2]		Min	Typ	Max	Unit
V_{CC}	PWM power supply range			1.8	-	5.5	V
f_{PWM}	PWM output frequency			488.3	-	31250	Hz
t_{A_PWM}	PWM ambient operating temperature	Range 6		-40	-	85	°C
		Range 8		-40	-	105	
V_{OL}	Output low voltage level	V_{CC} = [1.8 V to 5.5 V], $I_O \leq I_{DRIVE}$		-	-	0.4	V
V_{OH}	Output high voltage level	V_{CC} = [1.8 V to 5.5 V], $I_O \leq I_{DRIVE}$		V_{CC} - 0.4	-	-	
R_{ON} [3]	Output impedance	PWM_CFG/PWMx_DRIVE = 00b		-	-	100	Ω
		PWM_CFG/PWMx_DRIVE = 01b		-	-	130	
		PWM_CFG/PWMx_DRIVE = 10b		-	-	200	
		PWM_CFG/PWMx_DRIVE = 11b		-	-	400	
		When PWMx is disabled		HiZ	-	-	
I_{CC}	Operating supply current [4]	No PWM enabled	V_{CC} = 5.5 V	-	-	260	uA
			V_{CC} = 3.0 V	-	-	210	
			V_{CC} = 1.8 V	-	-	180	
		1x PWM enabled	V_{CC} = 5.5 V	-	-	360	
			V_{CC} = 3.0 V	-	-	310	
			V_{CC} = 1.8 V	-	-	250	
		2x PWM enabled [5]	V_{CC} = 5.5 V	-	-	380	
			V_{CC} = 3.0 V	-	-	330	
			V_{CC} = 1.8 V	-	-	270	
t_{BOOT_PWM}	PWM boot time	From 50% V_{CC} rising edge to 90% PWM first pulse rising edge		-	-	3	ms
t_{PWM_UPD}	Time to update PWM output from RF	Upon valid RF command, From EOF RX to 1st PWM rising edge of the new setup		-	-	3	ms
t_{PWM_CFG}	Time to update PWM configuration from RF	Upon valid RF command, From EOF RX to new configuration ready		-	-	3	ms
PWM_{RES}	PWM resolution (LSB duration)	Across Process, V_{CC} and temperature variations, with RF field ON		56.25	62.5	68.75	ns
$f_{ACCURACY}$	PWM frequency accuracy	Across Process, VCC & Temperature variations with RF field ON		-	-	±10	%
$\alpha_{ACCURACY}$[2]	Duty cycle accuracy	α = 5%, VCC = 5V5, f_{PWM}=31.25kHz, $C_L \leq 150$ pF, RF field ON		-	-	1	%
Low_Freq	Threshold frequency for PWM coexistence mode			-	-	1	kHz

1. *Measured at temperature range 6*
2. *Applies to ST25DV02K-W1 (ST25DV02K-W2 values coming soon).*
3. *Refer to Figure 30 for RON TYP variations across VCC & PWM_CFG/PWMx_DRIVE setting*
4. *Without output stage power consumption, accross whole temperature ranges, RF field OFF.*
5. *Applies to ST25DV02K-W2.*

Figure 30. Variation of Typical values of RON, depending on V_{CC} and PWM_CFG/PWMx_DRIVE @ maximum temperature

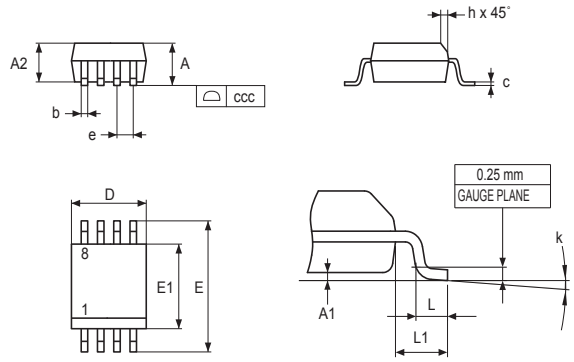


9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*.

9.1 SO8N package information

Figure 31. SO8N – 8 lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

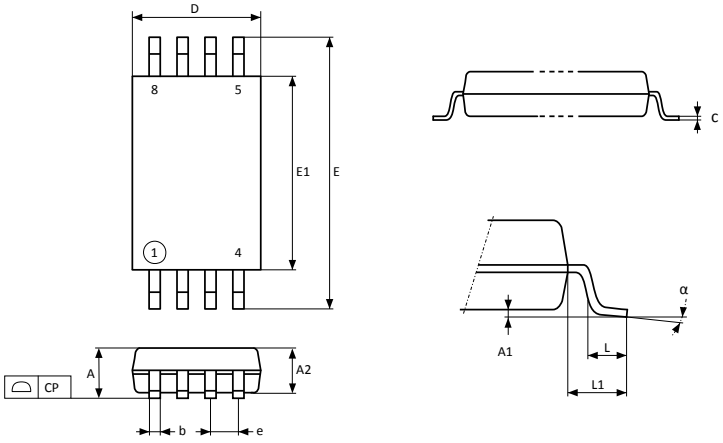
Table 114. SO8N – 8 lead 4.9 x 6 mm, plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*

9.2 TSSOP8 package information

Figure 32. TSSOP8 – 8 lead thin shrink small outline, 3 x 6.4 mm, 0.65 mm pitch, package outline



1. Drawing is not to scale.

Table 115. TSSOP8 – 8 lead thin shrink small outline, 3 x 6.4 mm, 0.65 mm pitch, package mechanical data

Symbol	millimeters			inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
CP	-	-	0.100	-	-	0.0039
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
α	0°	-	8°	0°	-	8°

1. *Values in inches are converted from mm and rounded to four decimal digits.*

10 Ordering information

Table 116. Ordering information scheme

Example: ST25DV 02K -W1 R 8 S 3

Device type

ST25DV = NFC/RFID tag based on ISO 15693 and NFC T5T

Memory size

02K = 2 Kbits

Features

W1 = 1x PWM output

W2 = 2x PWM outputs

Operating voltage

R = V_{CC} from 1.8 to 5.5 V

Device grade

8 = industrial: device tested with standard test flow over - 40 to 85 °C for RF and - 40 to 105 °C for PWM

Package

S = SO8N

T = TSSOP8

Capacitance

3 = 28.5 pF

Note: Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

11 List of acronyms

Table 117. **List of acronyms**

Acronym	Description
AFI	Application family identifier
CMD	Command
CRC	Cyclic redundancy check
DSFID	Data storage format identifier
EOF	End of frame
HZ	High impedance
Id	Identifier
NA	Not applicable
NFC	Near field communication
POR	Power on reset
PWD	Password
PWM	Pulse width modulation
RF	Radio frequency
RFU	Reserved for future usage
RO	Read only
RW	Read and write
SOF	Start of frame
UID	Unique identifier
VCD	Vicinity coupling device
VICC	Vicinity integrated circuit card
WO	Write only
X	Unknown

Revision history

Table 118. Document revision history

Date	Revision	Changes
14-Dec-2017	1	Initial release.
12-Jun-2018	2	Updated: • Features • Section 2.1 Pulse width modulation output (PWM1) • Section 2.2 Pulse width modulation output (PWM2) • Figure 8. PWM answer • Section 5.2.2 Passwords and security sessions • Section 6.4.17 Write Password • Table 111. Absolute maximum ratings • Table 112. RF characteristics • Table 113. PWM characteristics • Table 116. Ordering information scheme
25-Jun-2018	3	Updated: • Section 3.3 RF and PWM boots priority • Table 111. Absolute maximum ratings
10-Jul-2018	4	Changed the document scope from ST Restricted to public
14-Dec-2018	5	Updated: • Section 5.2.1 Data protection registers • Section 5.4 Device parameter registers Added: • Section 11 List of acronyms
30-Aug-2019	6	Updated document title, Section 1 Description and Section 5.1.2 Pulse width modulation feature description. Updated Figure 7. PWM output change and Figure 8. PWM answer. Updated Section 11 List of acronyms. Minor text edits across the whole document.

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