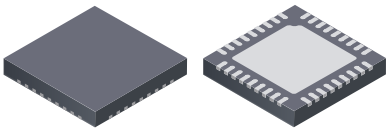
DMOS Dual Full-Bridge PWM Motor Driver

FEATURES AND BENEFITS

- 40 V output rating
- Two 3.2 A DC motor drivers
- Synchronous rectification
- Internal undervoltage lockout (UVLO)
- Thermal shutdown circuitry
- Crossover-current protection
- Very thin profile QFN package
- Overcurrent protection
- Low-power sleep mode
- 3.3 and 5 V compatible logic supply

Package: 36-pin QFN with exposed thermal pad
0.90 mm nominal height (suffix EV)



Not to scale

DESCRIPTION

The A5995 is designed to operate at voltages up to 40 V while driving two DC motors at currents up to 3.2 A. The A5995 includes a fixed off-time pulse-width modulation (PWM) regulator for current control. The DC motors are controlled using standard PHASE and ENABLE signals. Fast or slow current decay is selected via the MODE pin.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

Protection features include thermal shutdown with hysteresis, undervoltage lockout (UVLO), crossover-current and short-circuit protection. Special power-up sequencing is not required.

The A5995 is supplied in a leadless 6 mm × 6 mm × 0.9 mm, 36-pin QFN package with exposed power tab for enhanced thermal performance. The package is lead (Pb) free, with 100% matte-tin leadframe plating.

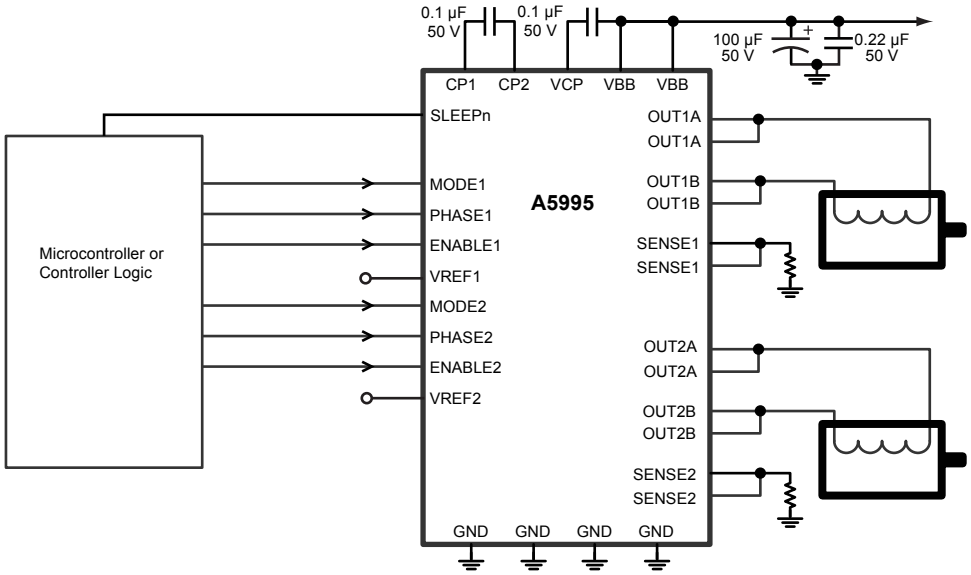


Figure 1:Typical Application Circuit

SELECTION GUIDE

Part Number	Packing
A5995GEVSR-T	6000 pieces per reel

ABSOLUTE MAXIMUM RATINGS

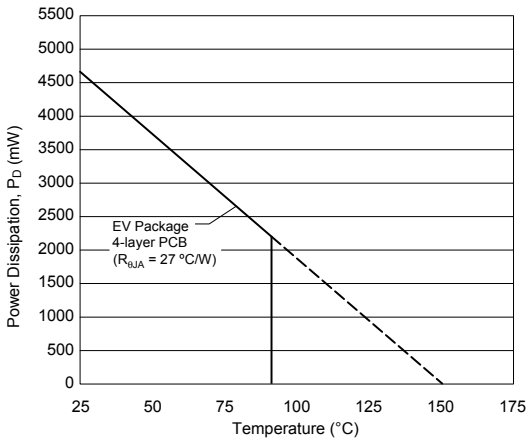
Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		–0.5 to 40	V
Output Current*	I_{OUT}	DC motor driver, continuous	3.2	A
Logic Input Voltage Range	V_{IN}		–0.3 to 7	V
SENSEx Pin Voltage	V_{SENSEx}		0.5	V
		Pulsed t_w < 1 µs	2.5	V
VREF*x* Pin Voltage	V_{REFx}		2.5	V
Operating Temperature Range	T_A	Range G	–40 to 105	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

* May be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a Junction Temperature of 150°C.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions	Min.	Units
Package Thermal Resistance	$R_{\theta JA}$	EV package, 4-layer PCB based on JEDEC standard	27	°C/W

Power Dissipation versus Ambient Temperature



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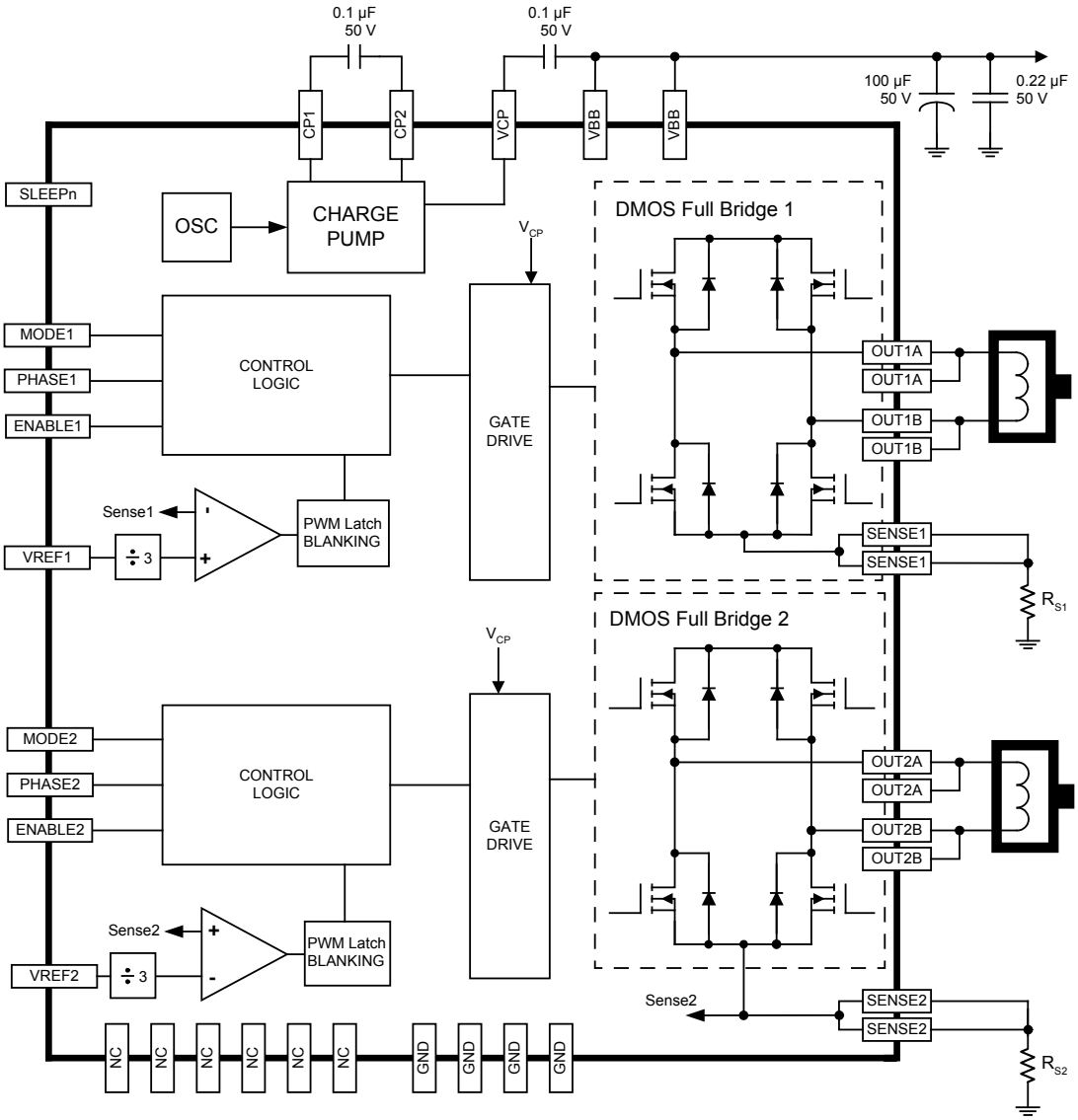
Functional Block Diagram



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ELECTRICAL CHARACTERISTICS[1]: **Valid at T_A = 25 °C, V_{BB} = 40 V, unless otherwise noted**

Characteristics	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Units
Load Supply Voltage Range	V_{BB}	Operating	8	–	40	V
Output On-Resistance	$R_{DS(on)}$	Source driver, I_{OUT} = –1.2 A, T_J = 25°C	–	250	300	mΩ
		Sink driver, I_{OUT} = 1.2 A, T_J = 25°C	–	240	300	mΩ
V_f, Outputs		I_{OUT} = 1.2 A	–	–	1.2	V
Output Leakage	I_{DSS}	Outputs, V_{OUT} = 0 to V_{BB}	–20	–	20	µA
VBB Supply Current	I_{BB}	I_{OUT} = 0 mA, outputs on, f_{PWM} = 50 kHz, duty cycle = 50%	–	–	23	mA
		Outputs off	–	11.7	14	mA
		Sleep mode	–10	< 1	10	µA
Output Driver Slew Rate	SR_{OUT}	10% to 90%	50	100	150	ns
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2	–	–	V
	$V_{IN(0)}$		–	–	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 0 to 5 V	–20	< 1	20	µA
Input Hysteresis	V_{hys}		150	300	500	mV
Sleep Rising Threshold	$V_{SLEEPn(r)}$		2.5	2.7	2.95	V
Sleep Falling Threshold	$V_{SLEEPn(f)}$		–	2.4	–	V
Sleep Hysteresis	$V_{SLEEPn(hys)}$		250	325	450	mV
Sleep Input Current	I_{SLEEPn}		–	100	150	µA
Propagation Delay Times	t_{pd}	PWM change to source on	550	700	1000	ns
		PWM change to source off	35	–	450	ns
		PWM change to sink on	550	700	1000	ns
		PWM change to sink off	35	–	450	ns
Crossover Delay	t_{CD}		250	425	1000	ns
Blank Time (DC motor driver)	t_{BLANK}		2.5	3.2	4	µs
VREF*x* Pin Input Voltage Range	V_{REFx}	Operating	0	–	1.5	V
VREF*x* Pin Reference Input Current	I_{REF}	V_{REF} = 1.5 V	–	–	±1	µA
Current Trip-Level Error	V_{ERR}	V_{REF} = 1.5 V	–5	–	5	%
Protection Circuits						
VBB UVLO Threshold	$V_{UV(VBB)}$	V_{BB} rising	7.3	7.6	7.9	V
VBB Hysteresis	$V_{UV(VBB)hys}$		400	500	600	mV
Overcurrent Protection Threshold	I_{OVP}		3.2	–	–	A
Thermal Shutdown Temperature	T_{JTSD}		155	165	175	°C
Thermal Shutdown Hysteresis	$T_{JTSDhys}$		–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

[2] Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

[3] $V_{ERR} = [(V_{REF}/3) – V_{SENSE}] / (V_{REF}/3)$.

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DC Control Logic

PHASE	ENABLE	MODE	$3 \times V_S > V_{REF}$	OUTA	OUTB	Function
1	1	1	false	H	L	Forward (slow decay SR)
1	1	0	false	H	L	Forward (fast decay SR)
0	1	1	false	L	H	Reverse (slow decay SR)
0	1	0	false	L	H	Reverse (fast decay SR)
X	0	1	X	L	L	Brake (slow decay SR)
1	0	0	X	L	H	Fast decay SR*
0	0	0	X	H	L	Fast decay SR*
X	1	1	true	L	L	OCL chop / slow decay SR
1	1	0	true	L	H	OCL chop / fast decay SR*
0	1	0	true	H	L	OCL chop / fast decay SR*

* To prevent reversal of current during fast decay SR – the outputs will go to the high-impedance state as the current gets near zero.

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FUNCTIONAL DESCRIPTION

Device Operation

The A5995 is designed to operate two DC motors. The currents in each of the full bridges, all N-channel DMOS, are regulated with fixed off-time pulse-width-modulated (PWM) control circuitry. The peak current in each full bridge is set by the value of an external current sense resistor, R_{Sx}, and a reference voltage, V_{REFx}.

Internal PWM Current Control

Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a user-specified value, I_{TRIP}. Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and R_{Sx}. When the voltage across the current sense resistor equals the voltage on the VREFx pin, the current sense comparator resets the PWM latch, which turns off the source driver.

The maximum value of current limiting is set by the selection of R_S and the voltage at the VREF input with a transconductance function approximated by:

$$I_{TripMax} = V_{REF} / (3 \times R_S)$$

Note: It is critical to ensure that the maximum rating of ±500 mV on each SENSEx pin is not exceeded.

Fixed Off-Time

The internal PWM current control circuitry uses a one-shot circuit to control the time the drivers remain off. The one-shot off-time, t_{off}, is internally set to 30 µs.

Blanking

This function blanks the output of the current sense comparator when the outputs are switched by the internal current control circuitry. The comparator output is blanked to prevent false detections of overcurrent conditions, due to reverse recovery currents of the clamp diodes, or to switching transients related to the capacitance of the load. DC motors require more blank time than stepper motors. The driver blank time, t_{BLANK}, is approximately 3 µs.

Phase Input (PHASEx)

The state of the PHASEx input determines the direction of rotation of the motor.

Control Logic

DC motor commutation is accomplished by applying a PWM signal together with the PHASE or ENABLE inputs. Fast or slow current decay during the off-time is selected via the MODE pin. Synchronous rectification is always active regardless of the state of the MODE pin.

Charge Pump (CP1 and CP2)

The charge pump is used to generate a gate supply greater than V_{BB} in order to drive the source-side DMOS gates. A 0.1 µF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1 µF ceramic capacitor is required between VCP and VBBx to act as a reservoir to operate the high-side DMOS devices.

Sleep Mode

To minimize power consumption when not in use, the A5995 can be put into Sleep Mode by bringing the SLEEPn pin low. Sleep Mode disables much of the internal circuitry, including the charge pump.

Overcurrent Protection

An overcurrent monitor protects the A5995 from damage due to output shorts. If a short is detected, the A5995 latches the fault and disables the outputs. The latched fault can only be cleared by cycling the power to VBB or by putting the device in Sleep Mode. During OCP events, Absolute Maximum Ratings may be exceeded for a short period of time before outputs are latched off.

Shutdown

In the event of a fault (excessive junction temperature, or low voltage on VCP), the outputs of the device are disabled until the fault condition is removed. At power-up, the undervoltage lockout (UVLO) circuit disables the drivers.

Synchronous Rectification

When a PWM off cycle is triggered by an internal fixed off-time cycle, load current will recirculate. The A5995 synchronous rectification feature will turn on the appropriate MOSFETs during the current decay. This effectively shorts the body diode with the low $R_{DS(on)}$ driver. This significantly lowers power dissipation. When a zero current level is detected, synchronous rectification is turned off to prevent reversal of the load current.

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MODE

Control input MODE is used to toggle between fast decay mode and slow decay mode for the DC driver. A logic high puts the device in slow decay mode. Synchronous rectification is always enabled when ENABLE is low.

Braking

Driving the device in slow decay mode via the MODE pin and applying an ENABLE chop command implements the Braking function. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts the motor-generated BEMF as long as the ENABLE chop mode is asserted. The maximum current can be approximated by V_{BEMF}/R_L. Care should be taken to ensure that the maximum ratings of the device are not exceeded in worst-case braking situations: high speed and high inertia loads.

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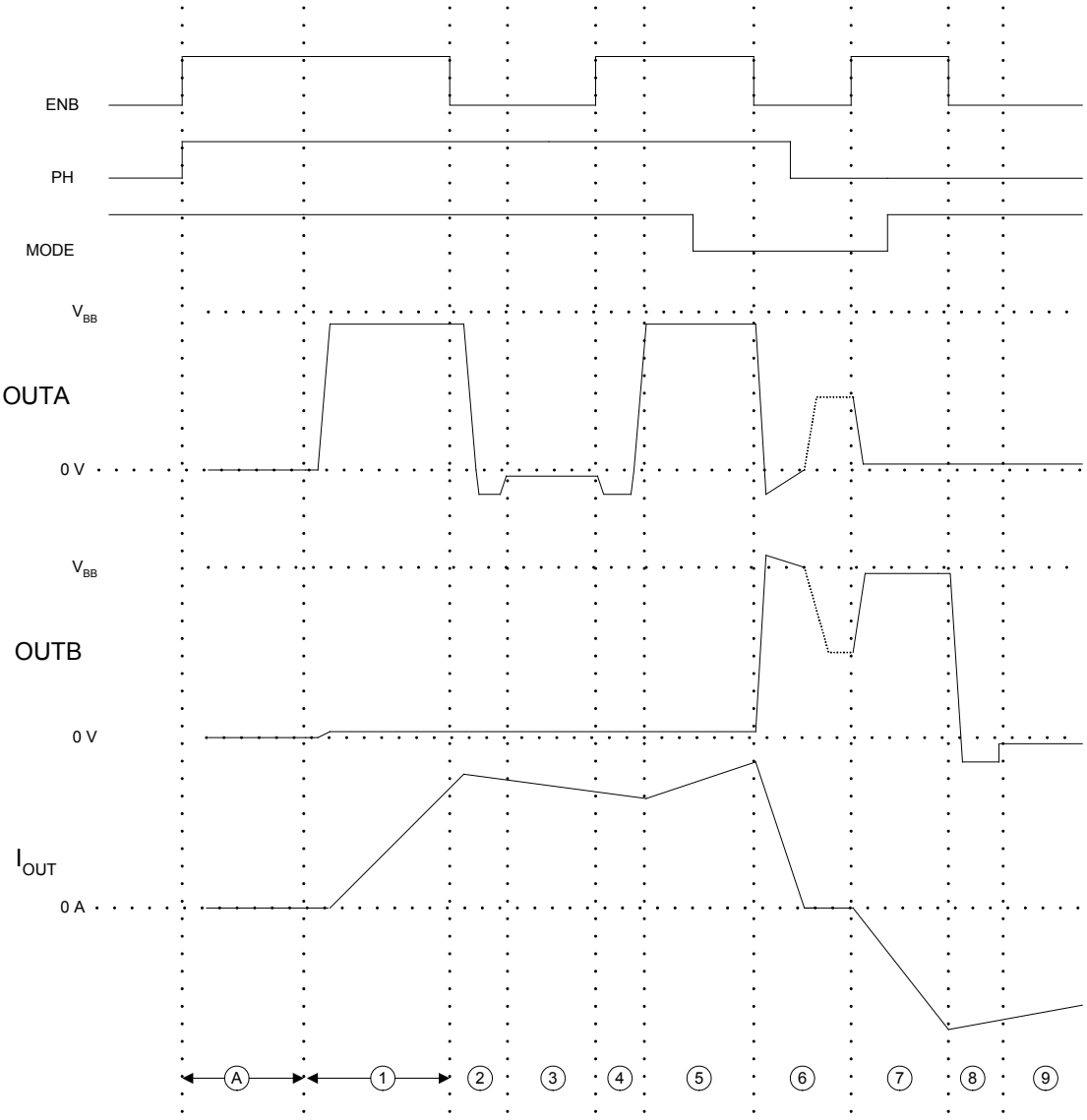
LOGIC TIMING DIAGRAM, DC DRIVER



(A) Charge Pump and VREG Power-up Delay (≈200 µs)

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APPLICATIONS INFORMATION

Motor Configurations

For applications that require either a stepper/DC motor driver or dual stepper motor driver, Allegro offers the A5989 and A5988. These devices are offered in the same QFN package as the A5995. The A5988 is capable of driving two bipolar stepper motors at output currents up to 1.2 A. The stepper control logic is industry-standard parallel communication. Refer to the Allegro website for datasheets and further information about those devices.

Layout

The printed circuit board should use a heavy groundplane. For optimum electrical and thermal performance, the A5995 must be soldered directly onto the board. On the underside of the A5995 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

Grounding

In order to minimize the effects of ground bounce and offset issues, it is important to have a low-impedance single-point ground, known as a *star ground*, located very close to the device. By making the connection between the exposed thermal pad and the groundplane directly under the A5995, that area becomes an ideal location for a star ground point.

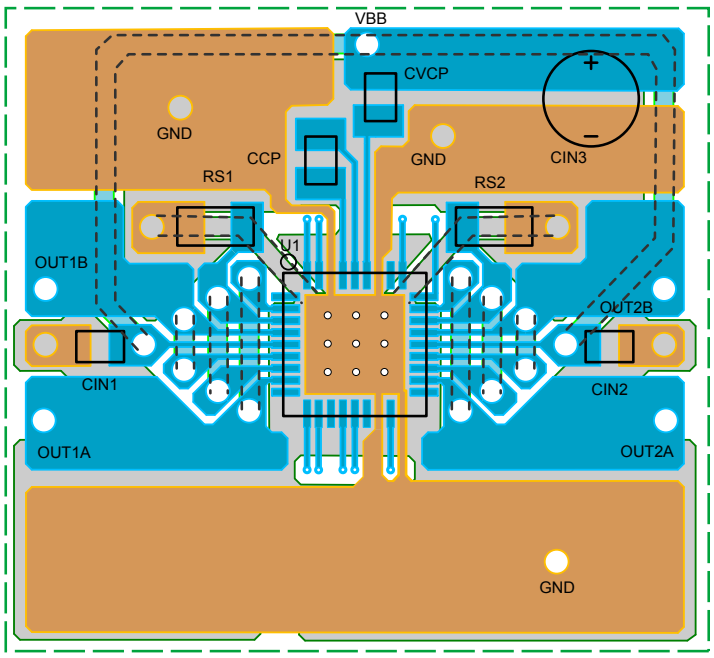
A low-impedance ground will prevent ground bounce during high-current operation and ensure that the supply voltage remains stable at the input terminal. The recommended PCB layout shown in the diagram below, illustrates how to create a star ground under the device, to serve both as low-impedance ground point and thermal path.

The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor should be closer to the pins than the bulk capacitor. This is necessary because the ceramic capacitor will be responsible for delivering the high-frequency current components.

Sense Pins

The sense resistors, RS*x*, should have a very low-impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. As shown in the layout below, the SENSE*x* pins have very short traces to the RS*x* resistors and very thick, low-impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.

Note: When selecting a value for the sense resistors, be sure not to exceed the maximum voltage on the SENSE*x* pins of ±500 mV.



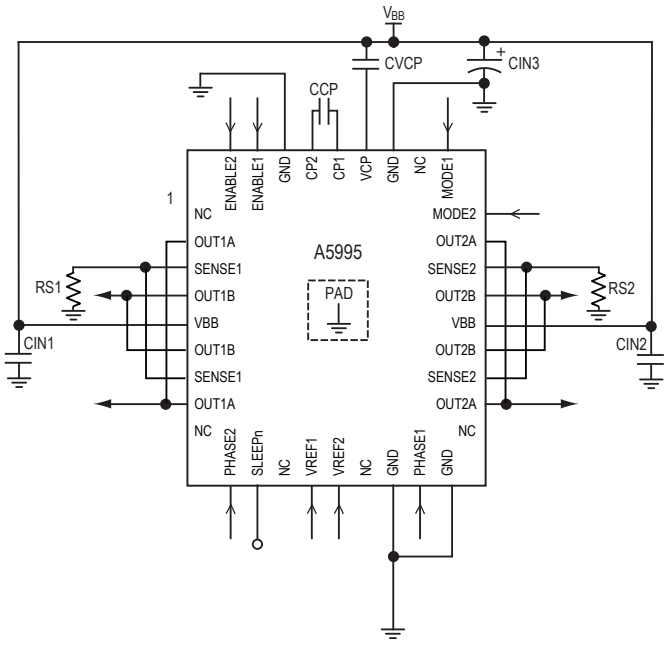


Figure 2: Printed circuit board layout with typical application circuit, shown at right. The copper area directly under the A5995 (U1) is soldered to the exposed thermal pad on the underside of the device. The thermal vias serve also as electrical vias, connecting it to the ground plane on the other side of the PCB , so the two copper areas together form the star ground.

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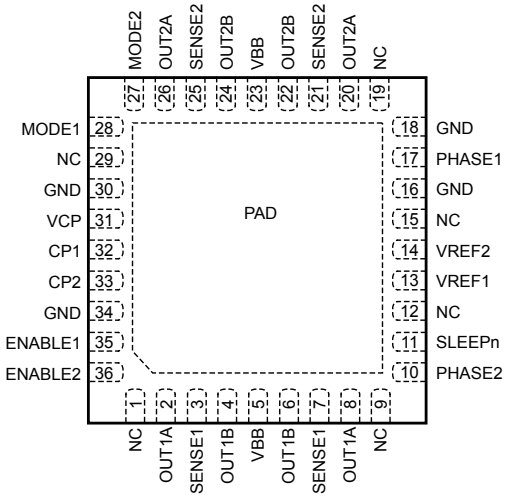
Pinout Diagram



Terminal List Table

Number	Name	Description
1	NC	No Connect
2	OUT1A	DMOS Full Bridge 1 Output A
3	SENSE1	Sense Resistor Terminal for Bridge 1
4	OUT1B	DMOS Full Bridge 1 Output B
5	VBB	Load Supply Voltage
6	OUT1B	DMOS Full Bridge 1 Output B
7	SENSE1	Sense Resistor Terminal for Bridge 1
8	OUT1A	DMOS Full Bridge 1 Output A
9	NC	No Connect
10	PHASE2	Control Input
11	SLEEPn	Active-Low Sleep Mode Input
12	NC	No Connect
13	VREF1	Analog Input
14	VREF2	Analog Input
15	NC	No Connect
16	GND	Ground
17	PHASE1	Control Input
18	GND	Ground
19	NC	No Connect
20	OUT2A	DMOS Full Bridge 2 Output A
21	SENSE2	Sense Resistor Terminal for Bridge 2
22	OUT2B	DMOS Full Bridge 2 Output B
23	VBB	Load Supply Voltage
24	OUT2B	DMOS Full Bridge 2 Output B
25	SENSE2	Sense Resistor Terminal for Bridge 2
26	OUT2A	DMOS Full Bridge 2 Output A
27	MODE2	Control Input
28	MODE1	Control Input
29	NC	No Connect
30	GND	Ground
31	V_{CP}	Reservoir Capacitor Terminal
32	CP_1	Charge Pump Capacitor Terminal
33	CP_2	Charge Pump Capacitor Terminal
34	GND	Ground
35	ENABLE1	Control Input
36	ENABLE2	Control Input
–	PAD	Exposed pad for enhanced thermal performance. Should be soldered to the PCB

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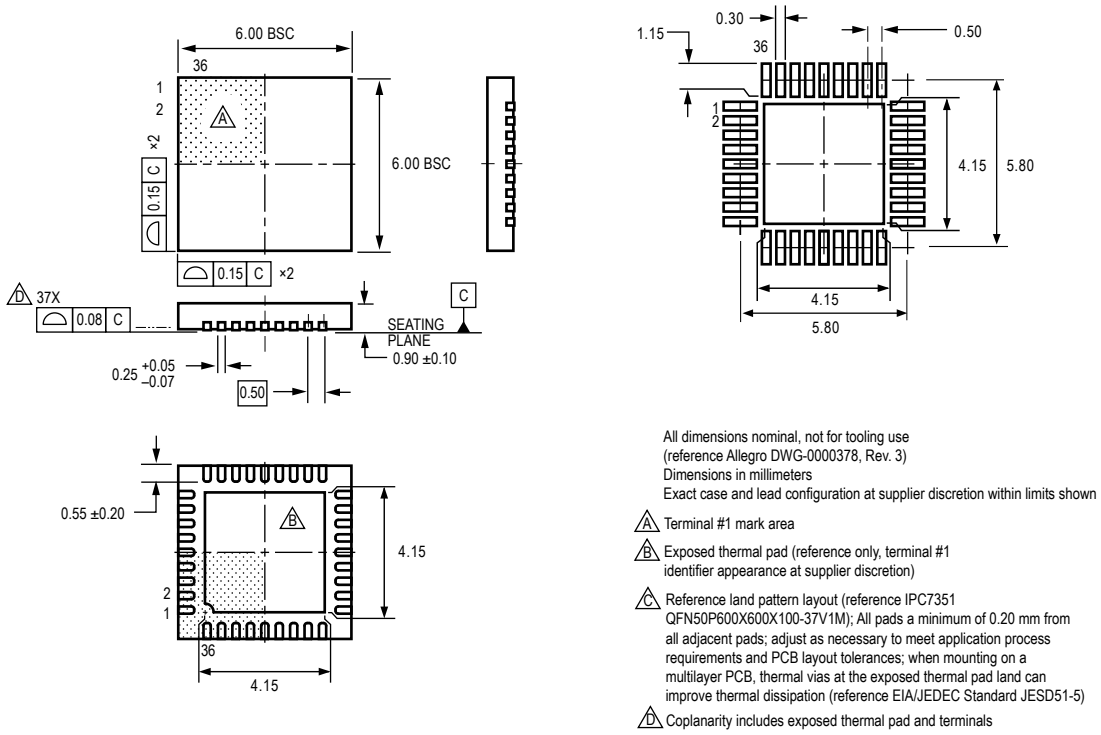
PACKAGE OUTLINE DRAWING



All dimensions nominal, not for tooling use
(reference Allegro DWG-0000378, Rev. 3)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P600X600X100-37V1M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

EV Package, 36-Pin QFN with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	June 20, 2016	Initial release
1	July 29, 2016	Updated Selection Guide table
2	April 20, 2020	Minor editorial updates
3	April 30, 2021	Updated Package Outline Drawing (page 11)

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