74HC126; 74HCT126

Quad buffer/line driver; 3-state

Rev. 5 — 12 July 2021

Product data sheet

1. General description

The 74HC126; 74HCT126 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs (nOE). A LOW on nOE causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- · High noise immunity
- · Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- · Inverting outputs
- · Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC126: CMOS levels
 - For 74HCT126: TTL levels
- · ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

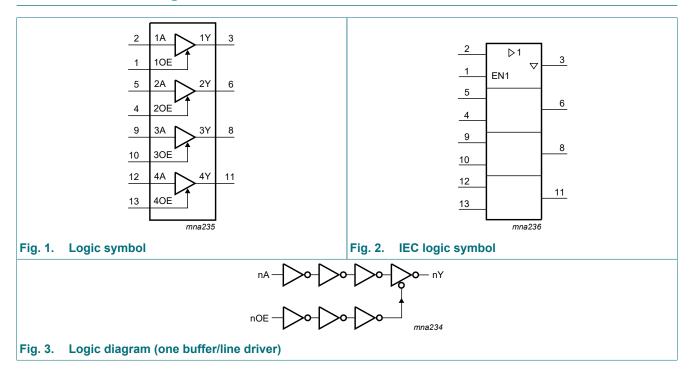
3. Ordering information

Table 1. Ordering information

Type number	Package				
	Temperature range	Name	Description	Version	
74HC126D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1	
74HCT126D			body width 3.9 mm		
74HC126PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1	
74HCT126PW			body width 4.4 mm		

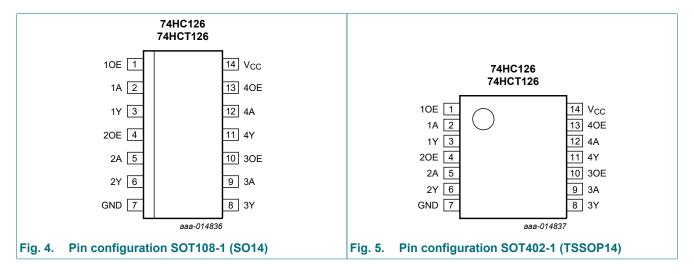


4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
10E, 20E, 30E, 40E	1, 4, 10, 13	data enable input (active HIGH)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nA	nY
Н	L	L
Н	Н	Н
L	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
Io	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$		-	±35	mA
I _{CC}	supply current			-	70	mA
I _{GND}	ground current			-70	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C. For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		74HC126	3	7	'4HCT12	6	Unit
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC12	6									
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 6.0 \text{ V}$; $V_O = V_{CC}$ or GND		±0.5	-	±5.0	-	±10	-	μΑ
I _{CC}	supply current			-	8.0	-	80	-	160	μΑ

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
Cı	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT1	26		'	'	'				1	'
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	8.0	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	Ι _Ο = -20 μΑ	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -6.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
OL	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	Ι _Ο = 20 μΑ	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μA
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC}$ - 2.1 V; $I_O = 0$ A; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V	-	100	360	-	450	-	490	μА
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit, see Fig. 8.

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	1
74HC12	6			'					-	
t _{pd}	propagation	nA to nY; see Fig. 6 [1]								
	delay	V _{CC} = 2.0 V	-	30	100	-	125	-	150	ns
		V _{CC} = 4.5 V	-	11	20	-	25	-	30	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	9	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	9	17	-	21	-	26	ns
t _{en}	enable time	nOE to nY; see Fig. 7 [1]								
		V _{CC} = 2.0 V	-	41	125	-	155	-	190	ns
		V _{CC} = 4.5 V	-	15	25	-	31	-	38	ns
		V _{CC} = 6.0 V	-	12	21	-	26	-	32	ns
t _{dis}	disable time	nOE to nY; see Fig. 7 [1]								
		V _{CC} = 2.0 V	-	41	125	-	155	-	190	ns
		V _{CC} = 4.5 V	-	15	25	-	31	-	38	ns
		V _{CC} = 6.0 V	-	12	21	-	26	-	32	ns

Symbol	Parameter	Conditions			25 °C		-40 °C to	o +85 °C	-40 °C to	Unit	
				Min	Тур	Max	Min	Max	Min	Max	
t _t	transition	see Fig. 6	[1]								
	time	V _{CC} = 2.0 V		-	14	60	-	75	-	90	ns
		V _{CC} = 4.5 V		-	5	12	-	15	-	18	ns
		V _{CC} = 6.0 V		-	4	10	-	13	-	15	ns
C _{PD}	power dissipation capacitance	per package; [2 $V_I = GND \text{ to } V_{CC}$		-	23	-	-	-	-	-	pF
74HCT1	26				l	'				-	
t _{pd}	propagation	nA to nY; see Fig. 6	[1]								
	delay	V _{CC} = 4.5 V		-	14	24	-	30	-	36	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	11	-	-	-	-	-	ns
t _{en}	enable time	nOE to nY; see Fig. 7; V _{CC} = 4.5 V	[1]	-	13	25	-	31	-	38	ns
t _{dis}	disable time	nOE to nY; see Fig. 7; V _{CC} = 4.5 V	[1]	-	18	28	-	35	-	42	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Fig. 6</u>	[1]	-	5	12	-	15	-	18	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V	[2]	-	24	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

 t_{en} is the same as t_{PZL} and t_{PZH} .

 t_{dis} is the same as t_{PLZ} and $t_{\text{PHZ}}.$

 $\begin{array}{ll} t_t \text{ is the same as } t_{THL} \text{ and } t_{TLH}. \\ \text{[2]} \quad C_{PD} \text{ is used to determine the dynamic power dissipation } (P_D \text{ in } \mu W). \end{array}$

 $P_D = C_{PD} x V_{CC}^2 x f_i x N + \Sigma (C_L x V_{CC}^2 x f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

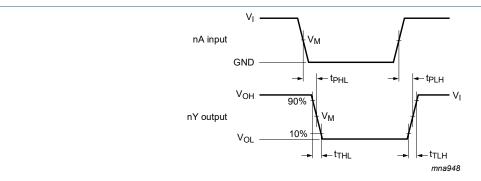
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

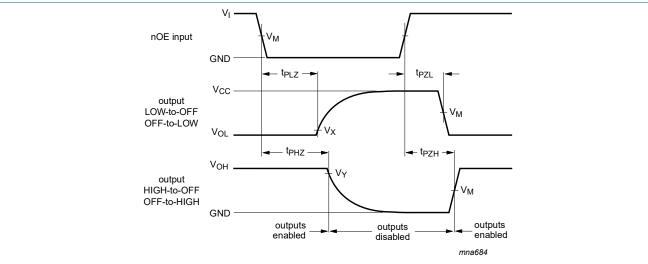
10.1. Waveforms and test circuit



Measurement points are given in <u>Table 8</u>.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Input (nA) to output (nY) propagation delays



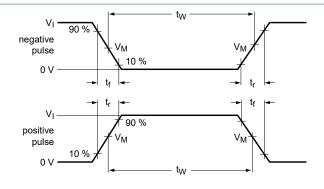
Measurement points are given in Table 8.

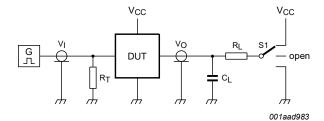
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Enable and disable times

Table 8. Measurement points

Туре	Input	Output	Output								
	V _M	V _M	V _X	V _Y							
74HC126	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}							
74HCT126	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}							





Test data is given in Table 9.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

 C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig. 8. Test circuit for measuring switching times

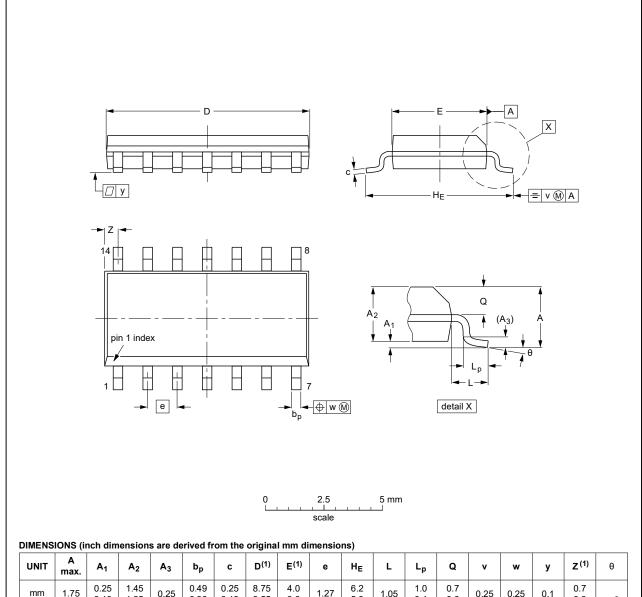
Table 9. Test data

Туре	Input		Load		S1 position				
	V_{l}	t _r , t _f	CL	R_L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t_{PZL} , t_{PLZ}		
74HC126	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}		
74HCT126	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}		

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

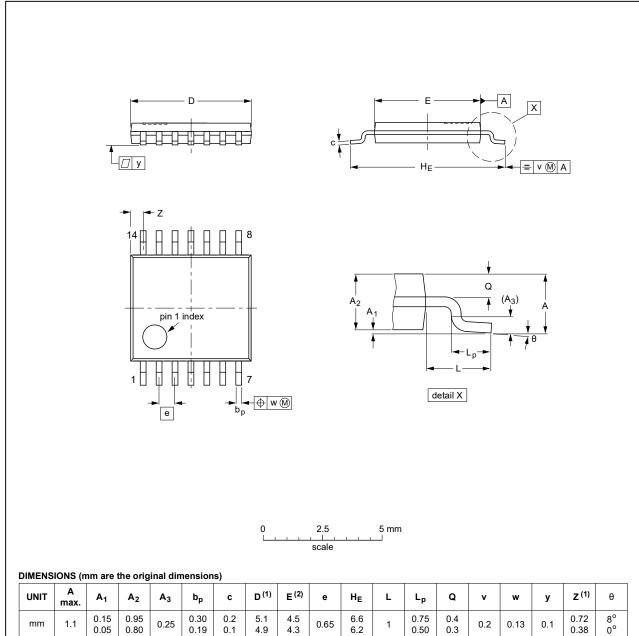
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Fig. 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT402-1		MO-153			99-12-27 03-02-18

Fig. 10. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Table 11. Revision history		I	I	
Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT126 v.5	20210712	Product data sheet	-	74HC_HCT126 v.4
Modifications:	Nexperia. Legal texts have Type numbers Section 2 upda	his data sheet has been redes we been adapted to the new co 74HC126DB and 74HCT126D ated. ating values for P _{tot} total powe	ompany name where DB (SOT337-1/SSOF	e appropriate. P14) removed.
74HC_HCT126 v.4	20151201	Product data sheet	-	74HC_HCT126 v.3
Modifications:	Type numbers	74HC126N and 74HCT126N ((SOT27-1) removed	
74HC_HCT126 v.3	20140922	Product data sheet	-	74HC_HCT126_CNV v.2
Modifications:	guidelines of N	his data sheet has been redes IXP Semiconductors. /e been adapted to the new co		·
74HC_HCT126_CNV v.2	19901201	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Functional diagram	2
5. Pinning information	2
5.1. Pinning	2
5.2. Pin description	3
6. Functional description	3
	•
7. Limiting values	3
 Limiting values Recommended operating conditions 	
-	4
8. Recommended operating conditions	4
8. Recommended operating conditions 9. Static characteristics	4 5
8. Recommended operating conditions 9. Static characteristics 10. Dynamic characteristics	4
8. Recommended operating conditions 9. Static characteristics 10.1. Waveforms and test circuit	4
8. Recommended operating conditions 9. Static characteristics 10. Dynamic characteristics 10.1. Waveforms and test circuit 11. Package outline	

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