General Description

The MAX7321 2-wire serial-interfaced peripheral features eight open-drain I/O ports with selectable internal pullups and transition detection. Any port may be used as a logic input or an open-drain output. Ports are overvoltage protected to +6V independent of supply voltage.

All I/O ports configured as inputs are continuously monitored for state changes (transition detection). State changes are indicated by the open-drain $\overline{INT}$ output. The interrupt is latched, allowing detection of transient changes. When the MAX7321 is subsequently accessed through the serial interface, any pending interrupt is cleared.

The open-drain outputs are rated to sink 20mA and are capable of driving LEDs.

The $\overline{RST}$ input clears the serial interface, terminating any I²C communication to or from the MAX7321.

The MAX7321 uses two address inputs with four-level logic to allow 16 I²C slave addresses. The slave address also determines the power-up logic state for the I/O ports, and enables or disables internal 40kΩ pullups in groups of four ports.

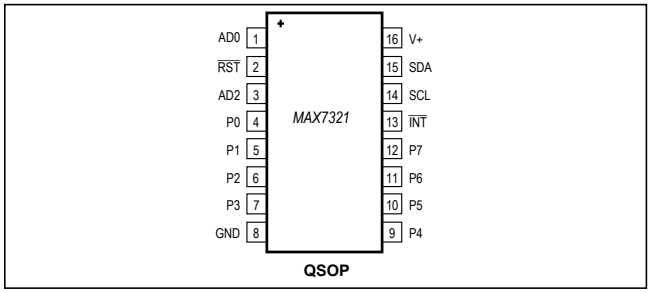
The MAX7321 is one device in a family of pin-compatible port expanders with a choice of input ports, open-drain I/O ports, and push-pull output ports (see Table 1).

The MAX7321 is available in 16-pin QSOP and TQFN packages, and is specified over the automotive temperature range (-40°C to +125°C).

Applications

- Cell Phones
- SAN/NAS
- Servers
- Notebooks
- Satellite Radio

Pin Configurations



Features

- 400kHz I²C Serial Interface
- +1.71V to +5.5V Operating Voltage
- 8 Open-Drain I/O Ports Rated to 20mA Sink Current
- I/O Ports Are Overvoltage Protected to +6V
- Any Port Can Be a Logic Input or an Open-Drain Output
- Selectable I/O Port Power-Up Default Logic States
- Transient Changes Are Latched, Allowing Detection Between Read Operations
- $\overline{INT}$ Output Alerts Change on Inputs
- AD0 and AD2 Inputs Select from 16 Slave Addresses
- Low 0.6µA (typ) Standby Current
- -40°C to +125°C Operating Temperature

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX7321AEE+	-40°C to +125°C	16 QSOP	—
MAX7321ATE+	-40°C to +125°C	16 TQFN-EP*	ADC

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Selector Guide

PART	INPUTS	INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS
MAX7319	8	Yes	—	—
MAX7320	—	—	—	8
MAX7321	Up to 8	—	Up to 8	—
MAX7322	4	Yes	—	4
MAX7323	Up to 4	—	Up to 4	4
MAX7328	Up to 8	—	Up to 8	—
MAX7329	Up to 8	—	Up to 8	—

Pin Configurations are continued at end of data sheet. Typical Application Circuit and Functional Diagram appear at end of data sheet.

19-3738; Rev 4; 7/14

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)

Supply Voltage V+ ..... -0.3V to +6V
SCL, SDA, AD0, AD2, $\overline{RST}$, $\overline{INT}$, P0–P7 ..... -0.3V to +6V
P0–P7 Sink Current 25mA
SDA Sink Current 10mA
$\overline{INT}$ Sink Current 10mA
Total V+ Current 50mA
Total GND Current 100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
16-Pin TQFN (derate 15.6mW/°C above +70°C) 1250mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow)
QSOP ..... +240°C
TQFN ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		1.71		5.50	V
Power-On Reset Voltage	V_{POR}	V+ falling			1.6	V
Standby Current (Interface Idle)	I_{STB}	SCL and SDA and other digital inputs at V+		0.6	1.5	µA
Supply Current (Interface Running)	I+	f_{SCL} = 400kHz; other digital inputs at V+		23	55	µA
Input High Voltage SDA, SCL, AD0, AD2, $\overline{RST}$, P0–P7	V_{IH}	V+ < 1.8V	0.8 x V+			V
		V+ ≥ 1.8	0.7 x V+			
Input Low Voltage SDA, SCL, AD0, AD2, $\overline{RST}$, P0–P7	V_{IL}	V+ < 1.8V			0.2 x V+	V
		V+ ≥ 1.8V			0.3 x V+	
Input Leakage Current SDA, SCL, AD0, AD2, $\overline{RST}$, P0–P7	I_{IH}, I_{IL}	SDA, SCL, AD0, AD2, $\overline{RST}$, P0–P7 at V+ or GND, internal pullup disabled	-0.2		+0.2	µA
Input Capacitance SDA, SCL, AD0, AD2, $\overline{RST}$, P0–P7				10		pF
Output Low Voltage P0–P7	V_{OL}	V+ = +1.71V, I_{SINK} = 5mA		90	180	mV
		V+ = +2.5V, I_{SINK} = 10mA		110	210	
		V+ = +3.3V, I_{SINK} = 15mA		130	230	
		V+ = +5V, I_{SINK} = 20mA		140	250	
Output Low Voltage SDA	V_{OLSDA}	I_{SINK} = 6mA			250	mV
Output Low Voltage $\overline{INT}$	V_{OLINT}	I_{SINK} = 5mA		130	250	mV
Port Input Pullup Resistor	R_{PU}		25	40	55	kΩ

Port and Interrupt $\overline{INT}$ Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Output Data Valid	t_{PPV}	$C_L \le 100pF$			4	µs
Port Input Setup Time	t_{PSU}	$C_L \le 100pF$	0			µs
Port Input Hold Time	t_{PH}	$C_L \le 100pF$	4			µs
$\overline{INT}$ Input Data Valid Time	t_{IV}	$C_L \le 100pF$			4	µs
$\overline{INT}$ Reset Delay Time from STOP	t_{IP}	$C_L \le 100pF$			4	µs
$\overline{INT}$ Reset Delay Time from Acknowledge	t_{IR}	$C_L \le 100pF$			4	µs

Timing Characteristics

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 2)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 3, 4)		$20 + 0.1C_b$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 3, 4)		$20 + 0.1C_b$	300	ns
Fall Time of SDA, Transmitting	$t_{F,TX}$	(Notes 3, 4)		$20 + 0.1C_b$	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 5)		50		ns
Capacitive Load for Each Bus Line	C_b	(Note 3)			400	pF
$\overline{RST}$ Pulse Width	t_W		500			ns
$\overline{RST}$ Rising to START Condition Setup Time	$t_{\overline{RST}}$		1			µs

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

Note 3: Guaranteed by design.

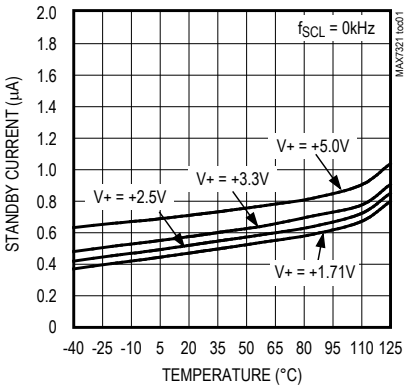
Note 4: C_b = total capacitance of one bus line in pF. $I_{SINK} \le 6mA$. t_R and t_F measured between 0.3 x V+ and 0.7 x V+.

Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

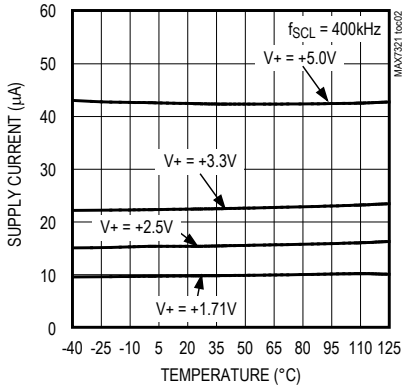
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

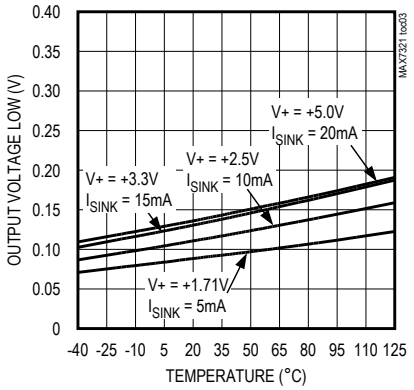
STANDBY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



OUTPUT VOLTAGE LOW vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN		
1, 3	15, 1	AD0, AD2	Address Inputs. Select device slave address with AD0 and AD2. Connect AD0 and AD2 to either GND, V+, SCL, or SDA to give four logic combinations (see Table 3).
2	16	$\overline{RST}$	Reset Input, Active Low. Drive $\overline{RST}$ low to clear the 2-wire interface.
4–7, 9–12	2–5, 7–10	P0–P7	Input/output Ports. P0 to P7 are open-drain I/Os.
8	6	GND	Ground
13	11	$\overline{INT}$	Interrupt Output. $\overline{INT}$ is an open-drain output.
14	12	SCL	I²C-Compatible Serial-Clock Input
15	13	SDA	I²C-Compatible Serial-Data I/O
16	14	V+	Positive Supply Voltage. Bypass V+ to GND with a ceramic capacitor of at least 0.047µF as close to the device as possible.
—	EP	EP	Exposed Pad. Connect exposed pad to GND.

Detailed Description

MAX7319–MAX7329 Family Comparison

The MAX7319–MAX7323 family consists of five pin-compatible, eight-port expanders. Each version is optimized for different applications. The MAX7328 and MAX7329 are industry standard parts.

The MAX7324–MAX7327 family consists of four pin-compatible, 16-port expanders that integrate the functions of the MAX7320 and one of either the MAX7319, MAX7321, MAX7322, or MAX7323.

Functional Overview

The MAX7321 is a general-purpose port expander operating from a +1.71V to +5.5V supply that provides eight open-drain I/O ports. Each open-drain output is rated to sink 20mA, and the entire device is rated to sink 100mA into all ports combined. The outputs drive loads connected to supplies up to +5.5V, independent of the MAX7321's supply voltage.

The MAX7321 is set to one of 16 I²C slave addresses (0x60 to 0x6F) using the address select inputs AD0 and AD2, and is accessed over an I²C serial interface up to 400kHz. The $\overline{RST}$ input clears the serial interface in

Table 1. MAX7319–MAX7329 Family Comparison

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	APPLICATION
8-PORT EXPANDERS						
MAX7319	110xxxx	8	Yes	—	—	Input-only versions: 8 input ports with programmable latching transition detection interrupt and selectable pullups. Offers maximum versatility for automatic input monitoring. An interrupt mask selects which inputs cause an interrupt on transitions, and transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7320	101xxxx	—	—	—	8	Output-only versions: 8 push-pull outputs with selectable power-up default levels. Push-pull outputs offer faster rise time than open-rain outputs, and require no pullup resistors.
MAX7321	110xxxx	Up to 8	—	Up to 8	—	I/O versions: 8 open-drain I/O ports with latching transition detection interrupt and selectable pullups. Open-drain outputs can level shift the logic-high state to a higher or lower voltage than V+ using external pullup resistors. Any port can be used as an input by setting the open-drain output to logic-high. Transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7322	110xxxx	4	Yes	—	4	4 input-only, 4 output-only versions: 4 input ports with programmable latching transition detection interrupt and selectable pullups; 4 push-pull outputs with selectable power-up default levels.

Table 1. MAX7319–MAX7329 Family Comparison (continued)

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	APPLICATION
MAX7323	110xxxx	Up to 4	—	Up to 4	4	4 I/O, 4 output-only versions: 4 open-drain I/O ports with latching transition detection interrupt and selectable pullups. 4 push-pull outputs with selectable power-up default levels.
MAX7328 MAX7329	0100xxx 0111xxx	Up to 8	—	Up to 8	—	8 open-drain I/O ports with nonlatching transition detection interrupt and pullups on all ports. All ports power up as inputs (or logic-high outputs). Any port can be used as an input by setting the open-drain output to logic-high.
16-PORT EXPANDERS						
MAX7324	101xxxx And 110xxxx	8	Yes	—	8	Software equivalent to a MAX7320 plus a MAX7319.
MAX7325		Up to 8	—	Up to 8	8	Software equivalent to a MAX7320 plus a MAX7321.
MAX7326		4	Yes	—	12	Software equivalent to a MAX7320 plus a MAX7322.
MAX7327		Up to 4	—	Up to 4	12	Software equivalent to a MAX7320 plus a MAX7323.

case of a bus lockup, terminating any serial transaction to or from the MAX7321.

Any port can be configured as a logic input by setting the port output logic-high (logic-high for an open-drain output is high impedance). When the MAX7321 is read through the serial interface, the actual logic levels at the ports are read back.

The open-drain ports offer latching transition detection when used as inputs. All input ports are continuously monitored for changes. An input change sets 1 of 8 flag bits that identify changed input(s). All flags are cleared upon a subsequent read or write transaction to the MAX7321.

A latching interrupt output ($\overline{INT}$) is programmed to flag logic changes on ports used as inputs. Data changes on any input port forces $\overline{INT}$ to a logic-low. Changing the I/O port level through the serial interface does not cause an interrupt. The interrupt output $\overline{INT}$ is deasserted when the MAX7321 is next accessed through the serial interface.

Internal pullup resistors to V+ are selected by the address select inputs (AD0 and AD2). Pullups are enabled on the input ports in groups of four (see Table 3).

Use the slave address selection to ensure that I/O ports used as inputs are logic-high on power-up. I/O ports with internal pullups enabled default to a logic-high output state. Ports with internal pullups disabled default to a logic-low output state. Output port power-up logic states are selected by the address select inputs AD0 and AD2. Ports default to logic-high or logic-low on power-up in groups of four (see Table 3).

Initial Power-Up

On power-up, the transition detection logic is reset, and $\overline{INT}$ is deasserted. The transition flags are cleared to indicate no data changes. The power-up default states of the eight I/O ports are set according to the I²C slave address selection inputs, AD0 and AD2 (Table 3). **For I/O ports used as inputs, ensure that the default states are logic-high so that the I/O ports power up in the high-impedance state. All I/O ports configured with pullups enabled also have a logic-high power-up state.**

Power-On Reset

The MAX7321 contains an integral power-on reset (POR) circuit that ensures all registers are reset to a known state on power-up. When V+ rises above V_{POR} (1.6V max), the POR circuit releases the registers and 2-wire interface for normal operation. When V+ drops to less than V_{POR}, the MAX7321 resets all register contents to the POR defaults (Table 3).

Table 2. Read and Write Access to Eight-Port Expander Family

PART	I²C SLAVE ADDRESS	INPUTS	INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	I²C DATA WRITE	I²C DATA READ
MAX7319	110xxxx	8	Yes	—	—	<I7–I0 interrupt mask>	<I7–I0 port inputs> <I7–I0 transition flags>
MAX7320	101xxxx	—	—	—	8	<O7–O0 port outputs>	<O7-O0 port inputs>
MAX7321	110xxxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs> <P7–P0 transition flags>
MAX7322	110xxxx	4	Yes	—	4	<O7, O6 outputs, I5–I2 interrupt mask, O1, O0 outputs>	<O7, O6, I5–I2, O1, O0 port inputs> <0, 0, I5–I2 transition flags, 0, 0>
MAX7323	110xxxx	Up to 4	—	Up to 4	4	<port outputs>	<O7, O6, P5–P2, O1, O0 port inputs> <0, 0, P5–P2 transition flags, 0, 0>
MAX7328	0100xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>
MAX7329	0111xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>

$\overline{\text{RST}}$ Input

The $\overline{\text{RST}}$ input voids any I²C transaction involving the MAX7321, forcing the MAX7321 into the I²C STOP condition. A reset does not affect the $\overline{\text{INT}}$ interrupt output.

Standby Mode

When the serial interface is idle, the MAX7321 automatically enters standby mode, drawing minimal supply current.

Slave Address, Power-Up Default Logic Levels, and Input Pullup Selection

Address inputs AD0 and AD2 determine the MAX7321 slave address, set the power-up I/O state for the ports, and select which inputs have pullup resistors. Internal pullups and power-up default states are set in groups of four (Table 3). The MAX7319, MAX7321, MAX7322, and MAX7323 use a different range of slave addresses (110xxxx) than the MAX7320 (101xxxx) (Table 2).

The MAX7321 slave address is determined on each I²C transmission, regardless of whether the transmission is actually addressing the MAX7321. The MAX7321 distinguishes whether address inputs AD2 and AD0 are connected to SDA or SCL instead of fixed logic levels V+ or GND during this transmission. This means that the MAX7321 slave address can be configured dynamically in the application without cycling the device supply.

On initial power-up, the MAX7321 cannot decode address inputs AD0 and AD2 fully until the first I²C transmission. AD0 and AD2 initially appear to be connected to V+ or GND. This is important because the address selection is used to determine the power-up logic state and whether pullups are enabled. However, at power-up, the I²C SDA and SCL bus interface lines are high impedance at the pins of every device (master or slave) connected to the bus, including the MAX7321. This is guaranteed as part of the I²C specification. Therefore, address inputs AD2 and AD0 that are connected to SDA or SCL normally appear at power-up to be connected to V+. The power-up logic uses AD0 to select the power-up state and whether pullups are enabled for ports P3–P0, and AD2 for ports P7–P4. The rule is that a logic-high, SDA, or SCL connection selects the pullups and sets the default logic state to high. A logic-low deselects the pullups and sets the default logic state to low (Table 3). The port configuration is correct on power-up for a standard I²C configu ration, where SDA or SCL are pulled up to V+ by the external I²C pullup resistors.

Table 3. MAX7321 Address Map

PIN CONNECTION		DEVICE ADDRESS							40kΩ INPUT PULLUP ENABLES							
AD2	**AD0**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**I7**	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**
SCL	GND	1	1	0	0	0	0	0	Y	Y	Y	Y	—	—	—	—
SCL	V+	1	1	0	0	0	0	1	Y	Y	Y	Y	Y	Y	Y	Y
SCL	SCL	1	1	0	0	0	1	0	Y	Y	Y	Y	Y	Y	Y	Y
SCL	SDA	1	1	0	0	0	1	1	Y	Y	Y	Y	Y	Y	Y	Y
SDA	GND	1	1	0	0	1	0	0	Y	Y	Y	Y	—	—	—	—
SDA	V+	1	1	0	0	1	0	1	Y	Y	Y	Y	Y	Y	Y	Y
SDA	SCL	1	1	0	0	1	1	0	Y	Y	Y	Y	Y	Y	Y	Y
SDA	SDA	1	1	0	0	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y
GND	**GND**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**—**	**—**	**—**	**—**	**—**	**—**	**—**	**—**
GND	**V+**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**—**	**—**	**—**	**—**	**Y**	**Y**	**Y**	**Y**
GND	SCL	1	1	0	1	0	1	0	—	—	—	—	Y	Y	Y	Y
GND	SDA	1	1	0	1	0	1	1	—	—	—	—	Y	Y	Y	Y
V+	**GND**	**1**	**1**	**0**	**1**	**1**	**0**	**0**	**Y**	**Y**	**Y**	**Y**	**—**	**—**	**—**	**—**
V+	**V+**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**Y**	**Y**	**Y**	**Y**	**Y**	**Y**	**Y**	**Y**
V+	SCL	1	1	0	1	1	1	0	Y	Y	Y	Y	Y	Y	Y	Y
V+	SDA	1	1	0	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y

There are circumstances where the assumption that SDA = SCL = V+ on power-up is not true (e.g., in applications in which there is legitimate bus activity during power-up). Also, if SDA and SCL are terminated with pullup resistors to a different supply voltage than the MAX7321's supply voltage, and if that pullup supply rises later than the MAX7321's supply, then SDA or SCL may appear at power-up to be connected to GND. In such applications, use the four address combinations that are selected by connecting address inputs AD2 and AD0 to V+ or GND (shown in **bold** in Table 3). These selections are guaranteed to be correct at power-up, independent of SDA and SCL behavior. If one of the other 12 address combinations is used, an unexpected combination of pullups might be asserted until the first I²C transmission (to any device, not necessarily the MAX7321) is put on the bus, and an unexpected combination of ports may initialize as logic-low outputs instead of inputs or logic-high outputs.

Port Inputs

I/O port inputs switch at the CMOS-logic levels, as determined by the expander's supply voltage, and are overvoltage tolerant to +6V, independent of the expander's supply voltage.

I/O Port Input Transition Detection

All I/O ports configured as inputs are monitored for changes since the expander was last accessed through the serial interface. The state of the input ports is stored in an internal "snapshot" register for transition monitoring. The snapshot is continuously compared with the actual input conditions, and if a change is detected for any port, $\overline{INT}$ is asserted to signal a state change. An internal transition flag is set for that port. The input is sampled (internally latched into the snapshot register) and the old transition flags cleared during the I²C acknowledge of every MAX7321 read and write access. The previous port transition flags are read through the serial interface as the second byte of a 2-byte read sequence.

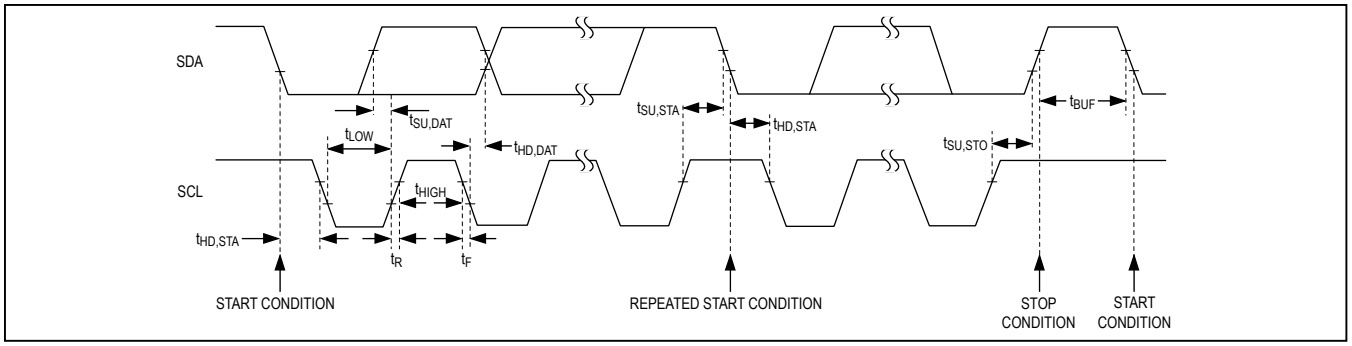


Figure 1. 2-Wire Serial Interface Timing Details

Serial Interface

Serial Addressing

The MAX7321 operates as a slave that sends and receives data through an I2C interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). The master initiates all data transfers to and from the MAX7321 and generates the SCL clock that synchronizes the data transfer (Figure 1).

SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition sent by a master, followed by the MAX7321's 7-bit slave address plus R/$\overline{W}$ bit, 1 or more data bytes, and finally a STOP condition (Figure 2).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 2).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 3).

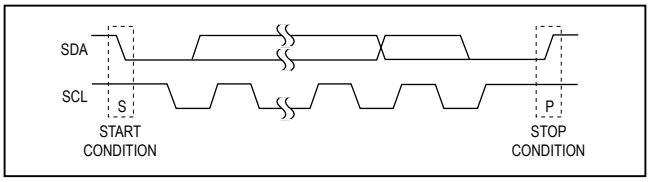


Figure 2. START and STOP Conditions

Acknowledge

The acknowledge bit is a clocked 9th bit the recipient uses to acknowledge receipt of each byte of data (Figure 4). Each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7321, the MAX7321 generates the acknowledge bit because the device is the recipient. When the MAX7321 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX7321 has a 7-bit-long slave address (Figure 5). The eighth bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command, and high for a read command.

The first (A6), second (A5), and third (A4) bits of the MAX7321 slave address are always 1, 1, and 0. Connect AD2 and AD0 to GND, V+, SDA, or SCL to select slave address bits A3, A2, A1, and A0. The MAX7321 has 16 possible slave addresses (Table 3), allowing up to 16 MAX7321 devices on an I2C bus.

Accessing the MAX7321

The MAX7321 is accessed through an I²C interface. The transition flags are cleared, and $\overline{INT}$ is deasserted each time the device acknowledges the I²C slave address.

A **single-byte read** from the MAX7321 returns the status of the eight I/O ports.

A **2-byte read** returns first the status of the eight I/O ports (as for a single-byte read), followed by the transition flags.

A **multibyte read** (more than 2 bytes before the I²C STOP bit) repeatedly returns the port data, alternating with the transition flags. As the port data is resampled for each transmission, and the transition flags are reset each time, a multibyte read continuously returns the current data and identifies any changing ports.

If a port data change occurs during the read sequence, $\overline{INT}$ is reasserted after the I²C STOP bit. The MAX7321 does not generate another interrupt during a single-byte or multibyte read.

Port data is sampled during the preceding I²C acknowledge bit (the acknowledge bit for the I²C slave address in the case of a single-byte or 2-byte read).

A **single-byte write** to the MAX7321 sets the logic state of all eight I/O ports.

A **multibyte write** to the MAX7321 repeatedly sets the logic state of all eight I/O ports.

Reading from the MAX7321

A read from the MAX7321 starts with the master transmitting the MAX7321's slave address with the R/$\overline{W}$ bit set high. The MAX7321 acknowledges the slave address, and samples the ports during the acknowledge bit. $\overline{INT}$ deasserts during the slave address acknowledge.

Typically, the master reads 1 or 2 bytes from the MAX7321, each byte being acknowledged by the master upon reception with the exception of the last byte.

When the master reads 1 byte from the MAX7321 and subsequently issues a STOP condition (Figure 6), the MAX7321 transmits the current port data, clears the change flags, and resets the transition detection. $\overline{INT}$ deasserts during the slave acknowledge. The new snapshot data is the current port data transmitted to the master; therefore, port changes ocurring during the transmission are detected. $\overline{INT}$ remains high until the STOP condition.

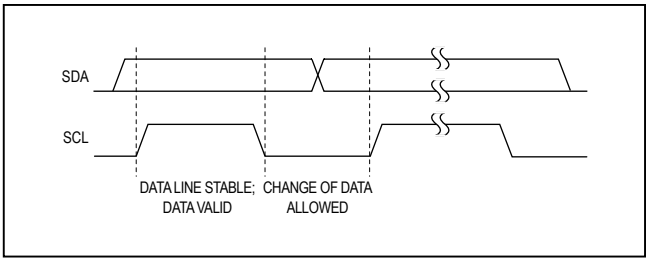


Figure 3. Bit Transfer

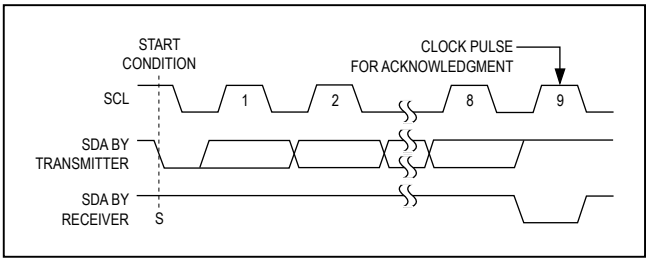


Figure 4. Acknowledge

The master can read 2 bytes from the MAX7321 and then issue a STOP condition (Figure 7). In this case, the MAX7321 transmits the current port data, followed by the change flags. The change flags are then cleared, and transition detection resets. $\overline{INT}$ goes high (high impedance if an external pullup resistor is not fitted) during the slave acknowledge. The new snapshot data is the current port data transmitted to the master; therefore, port changes occurring during the transmission are detected. $\overline{INT}$ remains high until the STOP condition.

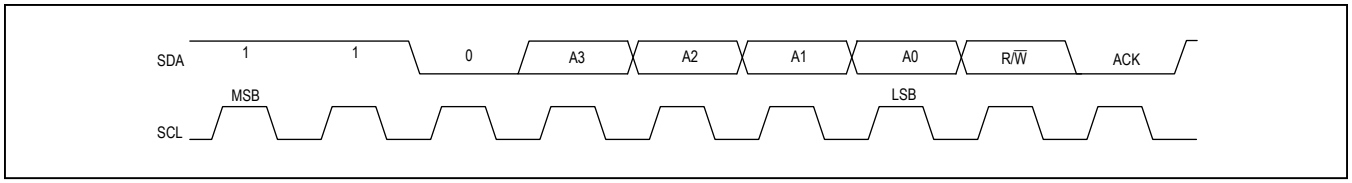


Figure 5. Slave Address

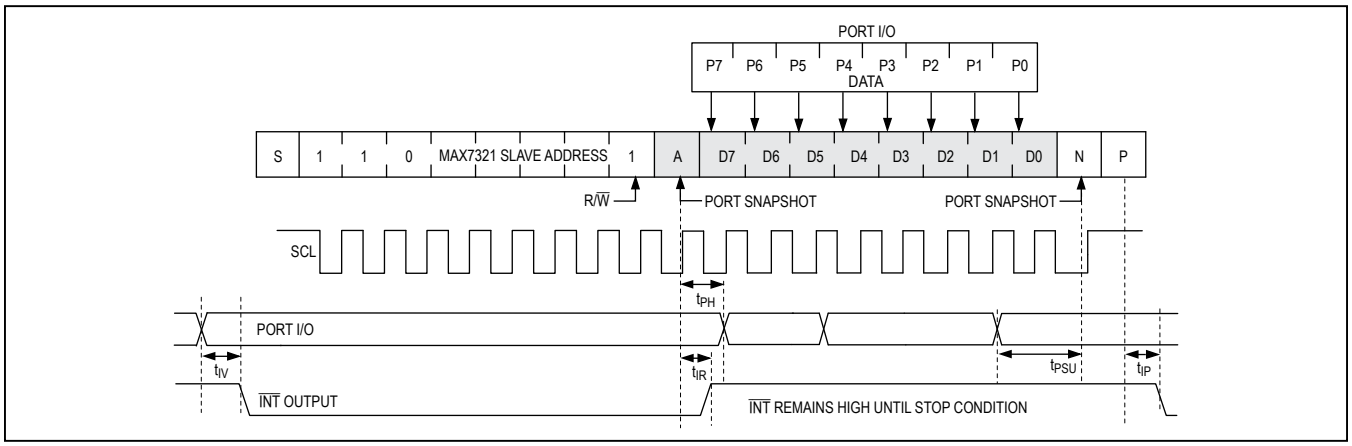


Figure 6. Reading the MAX7321 (1 Data Byte)

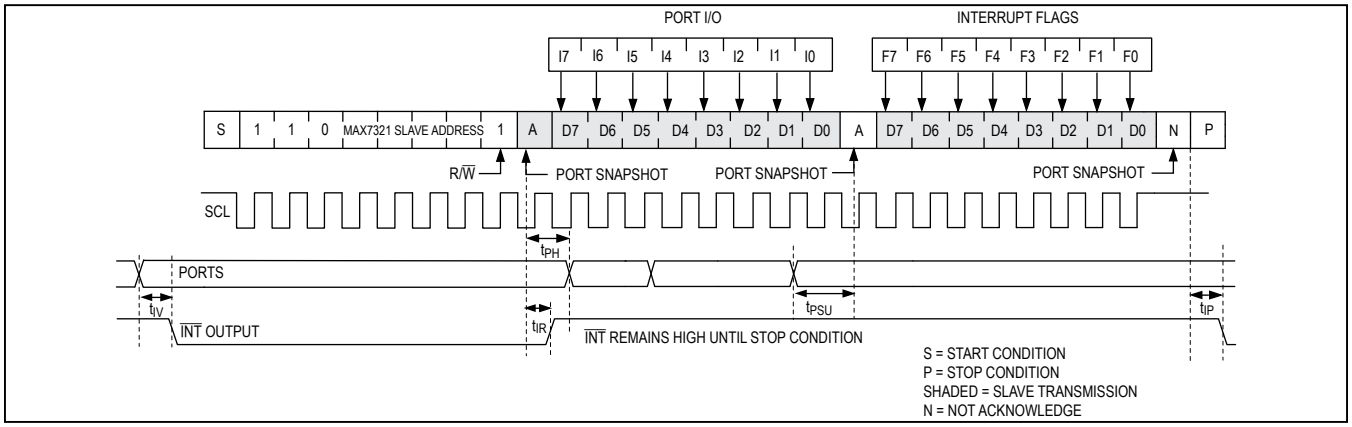


Figure 7. Reading the MAX7321 (2 Data Bytes)

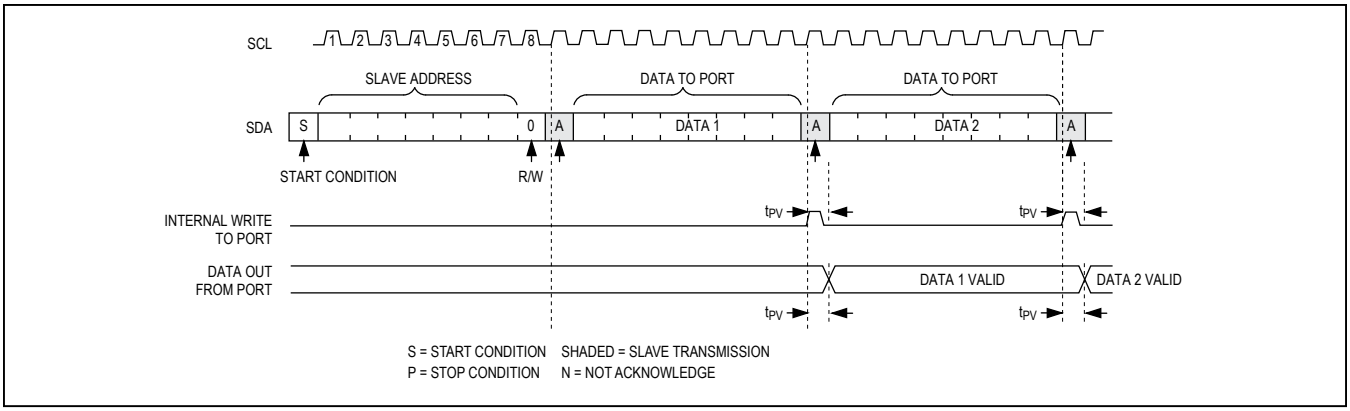


Figure 8. Writing to the MAX7321

Writing to the MAX7321

A write to the MAX7321 starts with the master transmitting the MAX7321's slave address with the R/$\overline{W}$ bit set low. The MAX7321 acknowledges the slave address, and samples the ports (takes a snapshot) during acknowledge. $\overline{INT}$ goes high (high impedance if an external pullup resistor is not fitted) during the slave acknowledge. Typically, the master proceeds to transmit 1 or more bytes of data. The MAX7321 acknowledges these subsequent bytes of data and updates the I/O ports with each new byte until the master issues a STOP condition (Figure 8).

Applications Information

Port Input and I2C Interface Level Translation from Higher or Lower Logic Voltages

The MAX7321's SDA, SCL, AD0, AD2, $\overline{RST}$, $\overline{INT}$, and I/O ports P0–P7 are overvoltage protected to +6V independent of V+. This allows the MAX7321 to operate from a lower supply voltage, such as +3.3V, while the I²C interface and/or any of the eight I/O ports are driven as inputs driven from a higher logic level, such as +5V.

The MAX7321 can operate from a higher supply voltage, such as +3V, while the I²C interface and/or some of the I/O ports (P0–P7) are driven from a lower logic level, such as +2.5V. Apply a minimum voltage of 0.7 x V+ to assert a logic-high on any I/O port (e.g., a MAX7321 operating from a +5V supply may not recognize a +3.3V nominal logic-high). One solution for input-level translation is to drive MAX7321 I/Os from open-drain outputs. Use a pullup resistor to V+ or a higher supply to ensure a high logic voltage greater than 0.7 x V+.

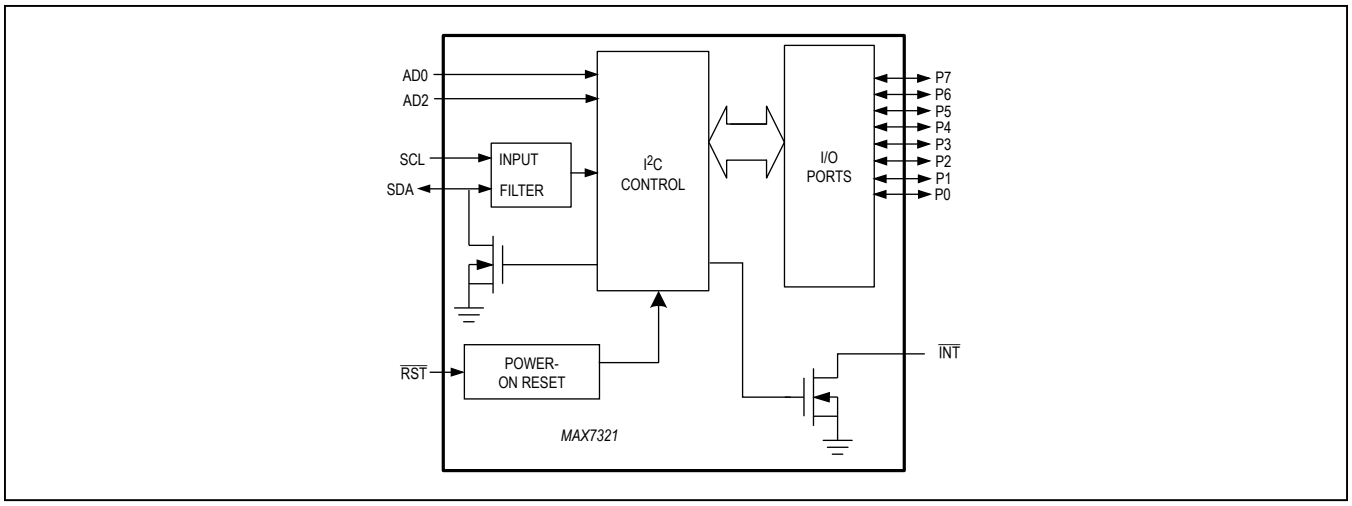
Port-Output Port-Level Translation

The open-drain output architecture allows for level translation to higher or lower voltages than the MAX7321's supply. Use an external pullup resistor on any output to convert the high-impedance logic-high condition to a positive voltage level. The resistor can be connected to any voltage up to +6V, and the resistor value chosen to ensure no more than 20mA is sunk in the logic-low condition. For interfacing CMOS inputs, a pullup resistor value of 220kΩ is a good starting point. Use a lower resistance to improve noise immunity, in applications where power consumption is less critical, or where a faster rise time is needed for a given capacitive load.

Each of the I/O ports (P0–P7) has a protection diode to GND (Figure 9). When a port is driven to a voltage lower than GND, the protection diode clamps the voltage to a diode drop below GND.

Each of the P0–P7 I/O ports also has a 40kΩ (typ) pullup resistor that can be enabled or disabled. When a port is driven to a voltage higher than V+, the body diode of the pullup enable switch conducts and the 40kΩ pullup resistor is enabled. When the MAX7321 is powered down (V+ = 0), each I/O port appears as a 40kΩ resistor in series with a diode connected to zero. I/O ports are protected to +6V under any of these circumstances (Figure 9).

Functional Diagram



Driving LED Loads

When driving LEDs, a resistor must be fitted in series with the LED to limit the LED current to no more than 20mA. Connect the LED cathode to the MAX7321 port, and the LED anode to V+ through the series current-limiting resistor (R_{LED}). Set the port output low to illuminate the LED. Choose the resistor value according to the following formula:

$$R_{LED} = (V_{SUPPLY} - V_{LED} - V_{OL})/I_{LED}$$

where:

R_{LED} is the resistance of the resistor in series with the LED (Ω).

V_{SUPPLY} is the supply voltage used to drive the LED (V).

V_{LED} is the forward voltage of the LED (V).

V_{OL} is the output-low voltage of the MAX7321 when sinking I_{LED} (V).

I_{LED} is the desired operating current of the LED (A).

For example, to operate a 2.2V red LED at 10mA from a +5V supply:

$$R_{LED} = (5 - 2.2 - 0.07)/0.010 = 270\Omega.$$

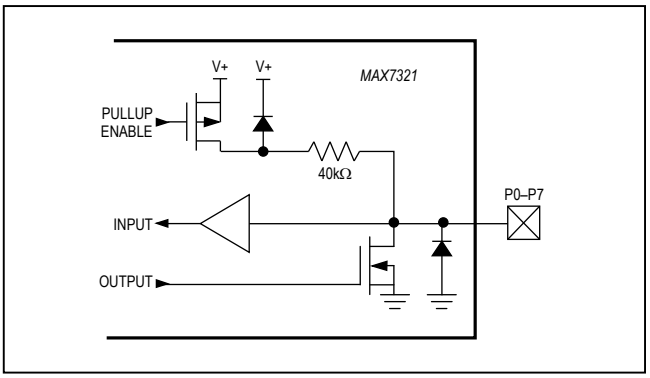


Figure 9. MAX7321 I/O Structure

Driving Load Currents Higher than 20mA

The MAX7321 can be used to drive loads, such as relays, that draw more than 20mA by paralleling outputs. Use at least one output per 20mA of load current; for example, a 5V, 330mW relay draws 66mA, and therefore, requires four paralleled outputs. Any combination of outputs can be used as part of a load-sharing design because any combination of ports can be set or cleared at the same time by writing the MAX7321. Do not exceed a total sink current of 100mA for the device.

The MAX7321 must be protected from the negative voltage transient generated when switching off inductive loads (such as relays), by connecting a reverse-biased diode across the inductive load. Choose the peak current for the diode to be greater than the inductive load's operating current.

Power-Supply Considerations

The MAX7321 operates with a supply voltage of +1.71V to +5.5V over the -40°C to +125°C temperature range. Bypass the supply to GND with a ceramic capacitor of at least 0.047µF as close as possible to the device. For the TQFN version, additionally connect the exposed pad to GND.

Issue: I²C Flag Clearing Deassertion Anomaly

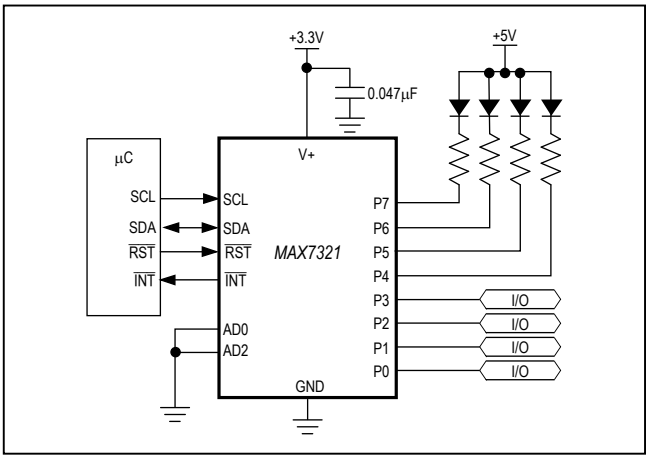
Description of Problem

The MAX7321 clears data stored in the interrupt flag and deasserts the corresponding interrupt when an I²C master reads any I²C slave on the same bus.

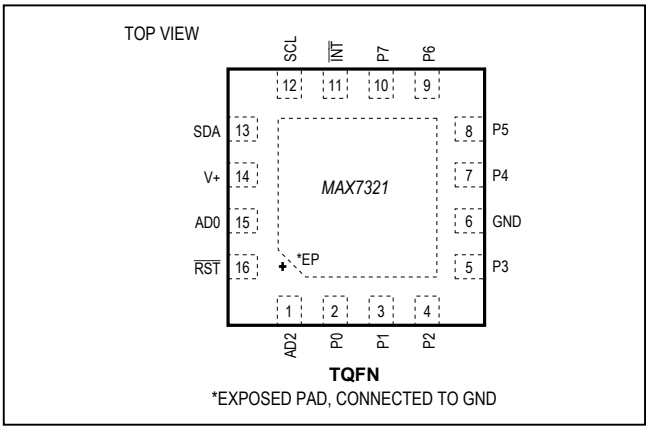
Workaround

To keep the interrupt flag data valid, the user must read the MAX7321 device BEFORE any other device on the I²C bus, after a pending interrupt. This limits the bus to only one MAX7321 device.

Typical Application Circuit



Pin Configurations (continued)



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+4	21-0055	90-0167
16 TQFN-EP	T1633+4	21-0136	90-0031

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/05	Initial release	—
1	4/06	Updates to data sheet	1–17
2	7/13	Added the *I²C Flag Clearing Deassertion Anomaly* section	14
3	5/14	No /V OPNs; removed automotive reference from *Applications* section	1
4	7/14	Revised the *Issue: I²C Flag Clearing Deassertion Anomaly* section	14

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