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Kind regards,

Team Nexperia

# PBLS1501Y; PBLS1501V

15 V PNP BISS loadswitch

Rev. 02 — 24 August 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Low  $V_{CEsat}$  PNP transistor and NPN resistor-equipped transistor in one package.

Table 1. Product overview

Type number	Package	
	NXP	JEITA
PBLS1501Y	SOT363	SC-88
PBLS1501V	SOT666	-

### 1.2 Features

- Low  $V_{CEsat}$  (BISS) transistor and resistor-equipped transistor in one package
- Low 'threshold' voltage ( $< 1$  V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

### 1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

### 1.4 Quick reference data

Table 2. Quick reference data

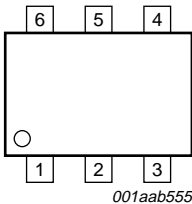
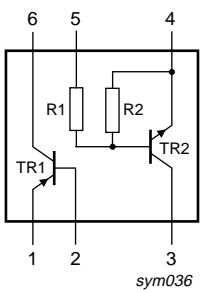
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR1; PNP: low <math>V_{CEsat}</math> transistor</b>						
$V_{CEO}$	collector-emitter voltage	open base	-	-	-15	V
$I_C$	collector-current (DC)		-	-	-500	mA
$R_{CEsat}$	equivalent on-resistance	$I_C = -500$ mA; $I_B = -50$ mA	-	300	500	m $\Omega$
<b>TR2; NPN: resistor-equipped transistor</b>						
$V_{CEO}$	collector-emitter voltage	open base	-	-	50	V

**Table 2. Quick reference data ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_o$	output current (DC)		-	-	100	mA
R1	bias resistor 1 (input)		1.54	2.2	2.86	k $\Omega$
R2/R1	bias resistor ratio		0.8	1	1.2	

## 2. Pinning information

**Table 3. Discrete pinning**

Pin	Description	Simplified outline	Symbol
1	emitter TR1	 <p>001aab555</p>	 <p>sym036</p>
2	base TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	collector TR1		

## 3. Ordering information

**Table 4. Ordering information**

Type number	Package		Version
	Name	Description	
PBLS1501Y	SC-88	plastic surface mounted package; 6 leads	SOT363
PBLS1501V	-	plastic surface mounted package; 6 leads	SOT666

## 4. Marking

**Table 5. Marking**

Type number	Marking code <sup>[1]</sup>
PBLS1501Y	*C1
PBLS1501V	C1

[1] \* = -: made in Hong Kong  
 \* = t: made in Malaysia  
 \* = W: made in China

## 5. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Transistor TR1: PNP</b>					
$V_{CBO}$	collector-base voltage	open emitter	-	-15	V
$V_{CEO}$	collector-emitter voltage	open base	-	-15	V
$V_{EBO}$	emitter-base voltage	open collector	-	-6	V
$I_C$	collector current (DC)		-	-500	mA
$I_{CM}$	peak collector current	$t_p \leq 1 \text{ ms}; \delta \leq 0.02$	-	-1	A
$I_B$	base current (DC)		-	-50	mA
$I_{BM}$	peak base current	$t_p \leq 1 \text{ ms}; \delta \leq 0.02$	-	-100	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$	[1]	200	mW
<b>Transistor TR2: NPN</b>					
$V_{CBO}$	collector-base voltage	open emitter	-	50	V
$V_{CEO}$	collector-emitter voltage	open base	-	50	V
$V_{EBO}$	emitter-base voltage	open collector	-	10	V
$V_I$	input voltage				
	positive		-	+12	V
	negative		-	-10	V
$I_O$	output current (DC)		-	100	mA
$I_{CM}$	peak collector current		-	100	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$	[1]	200	mW
<b>Per device</b>					
$P_{tot}$	total power dissipation		-	300	mW
$T_{stg}$	storage temperature		-65	+150	$^\circ\text{C}$
$T_j$	junction temperature		-	150	$^\circ\text{C}$
$T_{amb}$	ambient temperature		-65	+150	$^\circ\text{C}$

[1] Device mounted on a FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint.

## 6. Thermal characteristics

**Table 7. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per device</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
	SOT363		[1]	-	416	K/W
	SOT666		[1][2]	-	416	K/W

[1] Device mounted on a FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint.

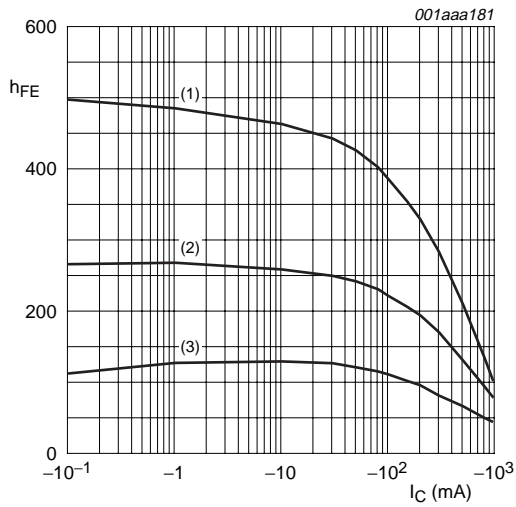
[2] Reflow soldering is the only recommended soldering method.

## 7. Characteristics

**Table 8. Characteristics**
*T<sub>amb</sub> = 25 °C unless otherwise specified*

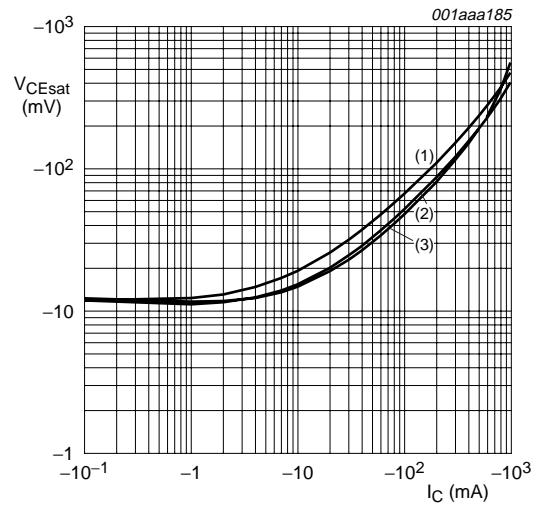
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Transistor TR1: PNP</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -15 V; I <sub>E</sub> = 0 A	-	-	-100	nA
		V <sub>CB</sub> = -15 V; I <sub>E</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	-50	μA
I <sub>CES</sub>	collector-emitter cut-off current	V <sub>CE</sub> = -15 V; V <sub>BE</sub> = 0 V	-	-	-100	nA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A	-	-	-100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -2 V; I <sub>C</sub> = -10 mA	200	-	-	
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -100 mA	[1] 150	-	-	
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -500 mA	[1] 90	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -10 mA; I <sub>B</sub> = -0.5 mA	-	-	-25	mV
		I <sub>C</sub> = -200 mA; I <sub>B</sub> = -10 mA	-	-	-150	mV
		I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA	[1] -	-	-250	mV
R <sub>CEsat</sub>	equivalent on-resistance	I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA	[1] -	300	500	mΩ
V <sub>BEsat</sub>	base-emitter saturation voltage	I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA	[1] -	-	-1.1	V
V <sub>BEon</sub>	base-emitter turn-on voltage	V <sub>CE</sub> = -2 V; I <sub>C</sub> = -100 mA	[1] -	-	-0.9	V
f <sub>T</sub>	transition frequency	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -100 mA; f = 100 MHz	100	280	-	MHz
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = -10 V; I <sub>E</sub> = I <sub>e</sub> = 0 A; f = 1 MHz	-	-	10	pF
<b>Transistor TR2: NPN</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A	-	-	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A	-	-	1	μA
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	50	μA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A	-	-	2	mA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 20 mA	30	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 0.5 mA	-	-	150	mV
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 1 mA	-	1.2	0.5	V
V <sub>I(on)</sub>	on-state input voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 20 mA	2	1.6	-	V
R1	bias resistor 1 (input)		1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = 10 V; I <sub>E</sub> = I <sub>e</sub> = 0 A; f = 1 MHz	-	-	2.5	pF

[1] Pulse test: t<sub>p</sub> ≤ 300 μs; δ ≤ 0.02



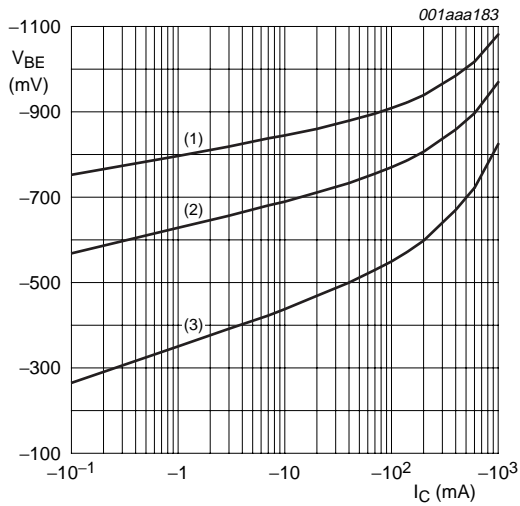
$V_{CE} = -2 V$   
 (1)  $T_{amb} = 150^\circ C$   
 (2)  $T_{amb} = 25^\circ C$   
 (3)  $T_{amb} = -55^\circ C$

**Fig 1. TR1(PNP): DC current gain as a function of collector current; typical values**



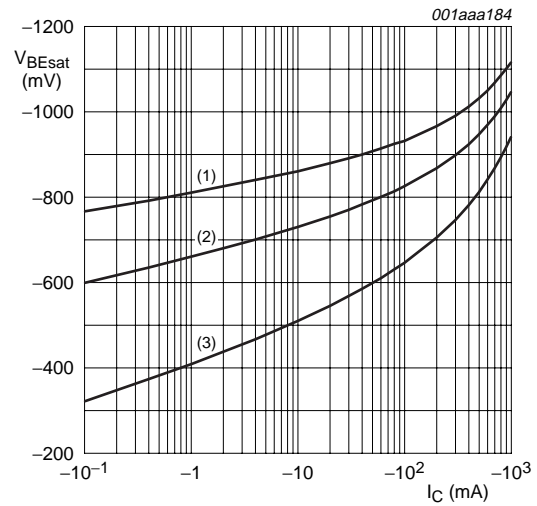
$I_C/I_B = 20$   
 (1)  $T_{amb} = 150^\circ C$   
 (2)  $T_{amb} = 25^\circ C$   
 (3)  $T_{amb} = -55^\circ C$

**Fig 2. TR1(PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



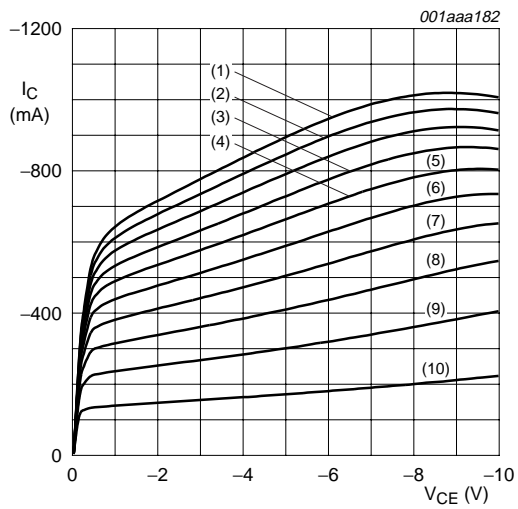
$V_{CE} = -2 V$   
 (1)  $T_{amb} = -55^\circ C$   
 (2)  $T_{amb} = 25^\circ C$   
 (3)  $T_{amb} = 150^\circ C$

**Fig 3. TR1(PNP): Base-emitter voltage as a function of collector current; typical values**



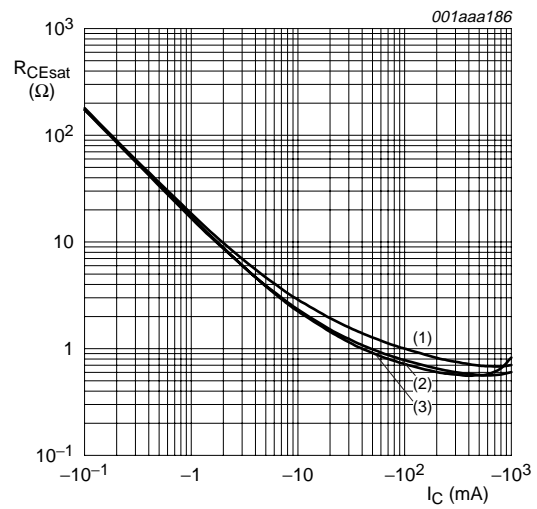
$I_C/I_B = 20$   
 (1)  $T_{amb} = 150^\circ C$   
 (2)  $T_{amb} = 25^\circ C$   
 (3)  $T_{amb} = -55^\circ C$

**Fig 4. TR1(PNP): Base-emitter saturation voltage as a function of collector current; typical values**



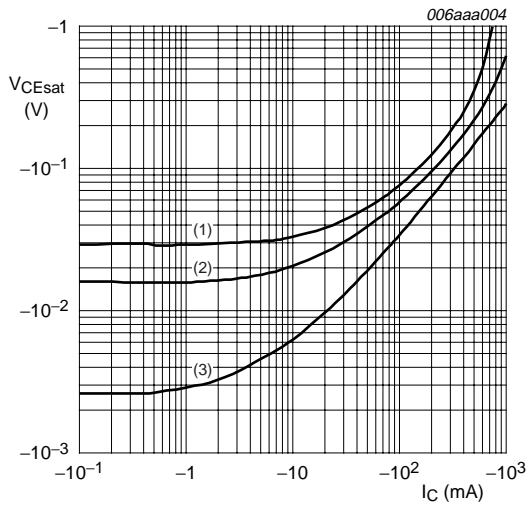
- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1)  $I_B = -7.0\text{ mA}$
  - (2)  $I_B = -6.3\text{ mA}$
  - (3)  $I_B = -5.6\text{ mA}$
  - (4)  $I_B = -4.9\text{ mA}$
  - (5)  $I_B = -4.2\text{ mA}$
  - (6)  $I_B = -3.5\text{ mA}$
  - (7)  $I_B = -2.8\text{ mA}$
  - (8)  $I_B = -2.1\text{ mA}$
  - (9)  $I_B = -1.4\text{ mA}$
  - (10)  $I_B = -0.7\text{ mA}$

**Fig 5. TR1(PNP): Collector current as a function of collector-emitter voltage; typical values**



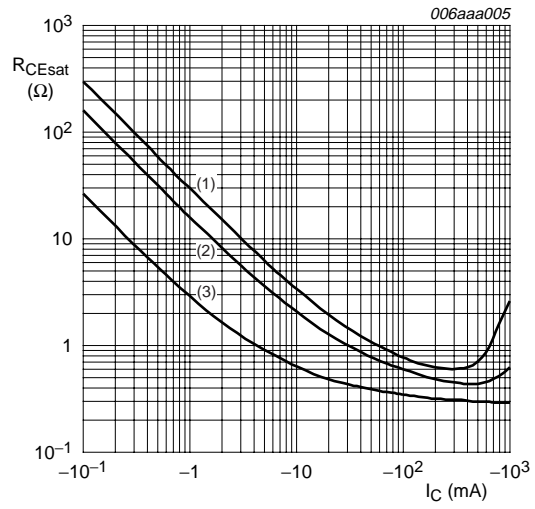
- $I_C/I_B = 20$
- (1)  $T_{amb} = -55\text{ }^{\circ}\text{C}$
  - (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
  - (3)  $T_{amb} = 150\text{ }^{\circ}\text{C}$

**Fig 6. TR1(PNP): Equivalent on-resistance as a function of collector current; typical values**



- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1)  $I_C/I_B = 100$
  - (2)  $I_C/I_B = 50$
  - (3)  $I_C/I_B = 10$

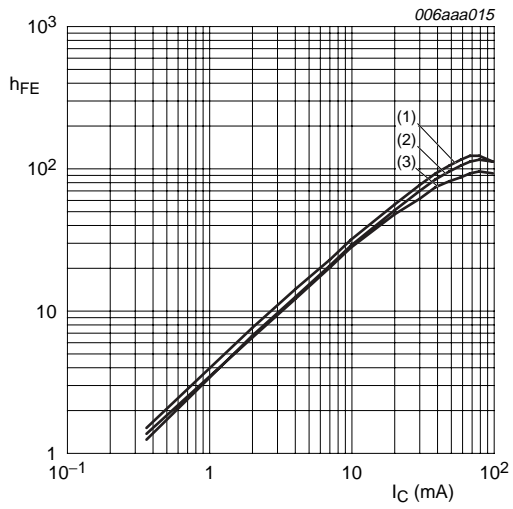
**Fig 7. TR1(PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1)  $I_C/I_B = 100$
  - (2)  $I_C/I_B = 50$
  - (3)  $I_C/I_B = 10$

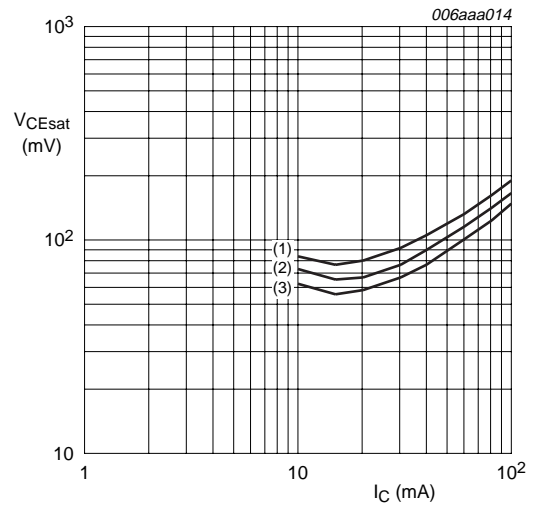
**Fig 8. TR1(PNP): Equivalent on-resistance as a function of collector current; typical values**





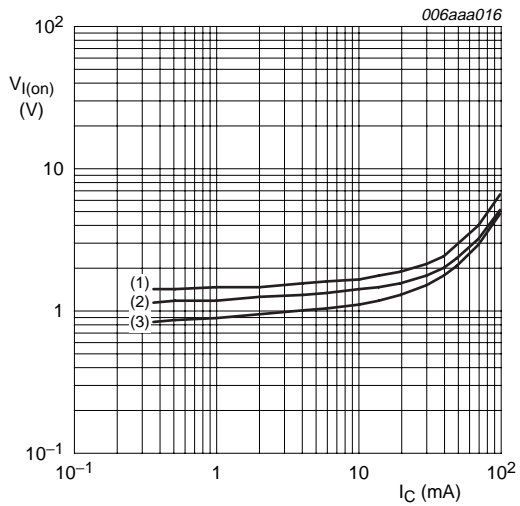
- $V_{CE} = 5\text{ V}$
- (1)  $T_{amb} = 150^\circ\text{C}$
  - (2)  $T_{amb} = 25^\circ\text{C}$
  - (3)  $T_{amb} = -40^\circ\text{C}$

Fig 9. TR2(NPN): DC current gain as a function of collector current; typical values



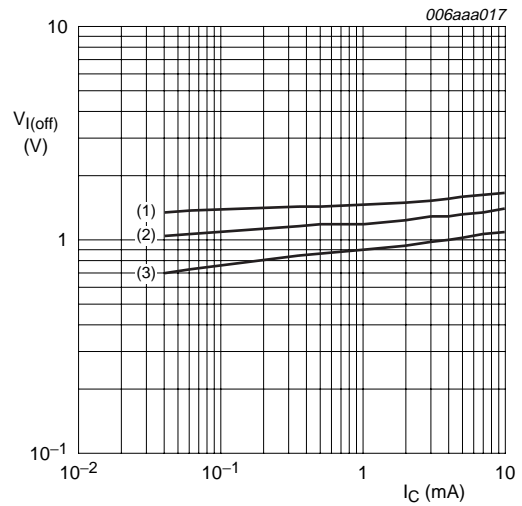
- $I_C/I_B = 20$
- (1)  $T_{amb} = 100^\circ\text{C}$
  - (2)  $T_{amb} = 25^\circ\text{C}$
  - (3)  $T_{amb} = -40^\circ\text{C}$

Fig 10. TR2(NPN): Collector-emitter saturation voltage as a function of collector current; typical values



- $V_{CE} = 0.3\text{ V}$
- (1)  $T_{amb} = -40^\circ\text{C}$
  - (2)  $T_{amb} = 25^\circ\text{C}$
  - (3)  $T_{amb} = 100^\circ\text{C}$

Fig 11. TR2(NPN): On-state input voltage as a function of collector current; typical values



- $V_{CE} = 5\text{ V}$
- (1)  $T_{amb} = -40^\circ\text{C}$
  - (2)  $T_{amb} = 25^\circ\text{C}$
  - (3)  $T_{amb} = 100^\circ\text{C}$

Fig 12. TR2(NPN): Off-state input voltage as a function of collector current; typical values

**8. Package outline**

Plastic surface-mounted package; 6 leads

SOT363

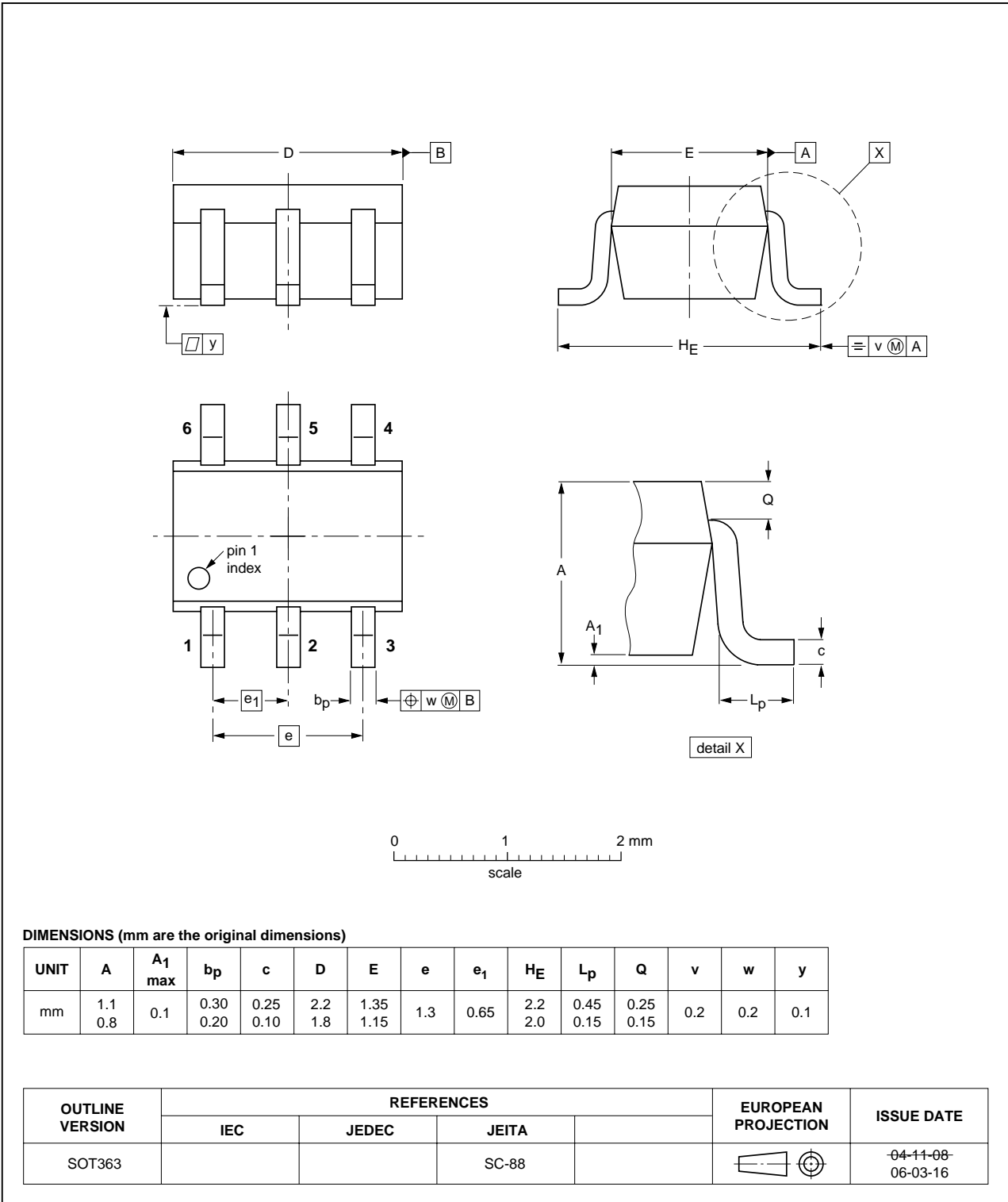


Fig 13. Package outline SOT363 (SC-88)

Plastic surface-mounted package; 6 leads

SOT666

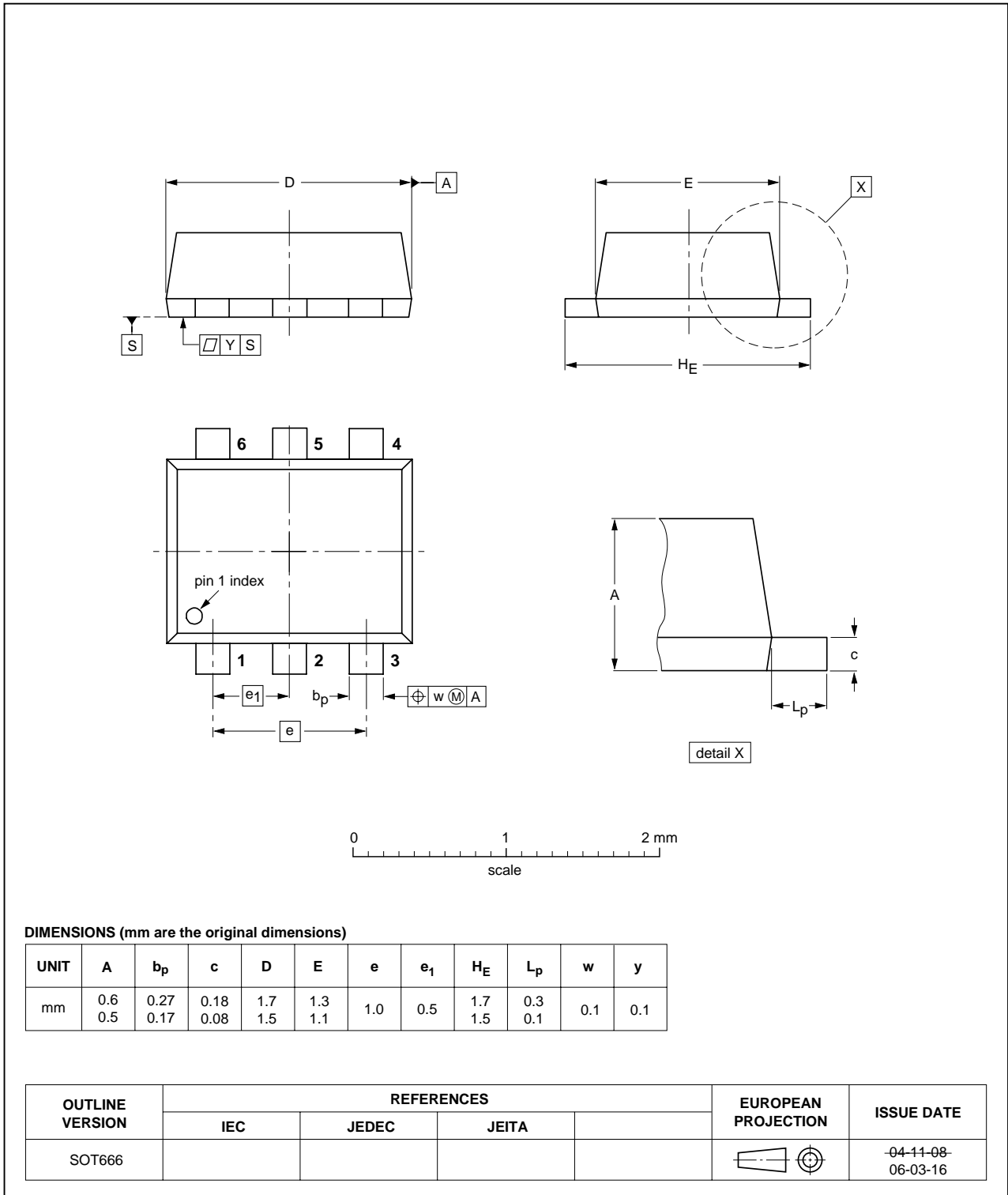


Fig 14. Package outline SOT666

## 9. Packing information

**Table 9. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

Type number	Package	Description	Packing quantity		
			3000	4000	10000
PBLS1501Y	SOT363	4 mm pitch, 8 mm tape and reel; T1	<sup>[2]</sup> -115	-	-135
		4 mm pitch, 8 mm tape and reel; T2	<sup>[3]</sup> -125	-	-165
PBLS1501V	SOT666	4 mm pitch, 8 mm tape and reel	-	-115	-

[1] For further information and the availability of packing methods, see [Section 12](#).

[2] T1: normal taping

[3] T2: reverse taping

## 10. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBL1501Y_PBL1501V_2	20090824	Product data sheet	-	PBL1501Y_PBL1501V_1
Modifications:		<ul style="list-style-type: none"><li>This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.</li><li><a href="#">Table 3 "Discrete pinning"</a>: amended</li><li><a href="#">Figure 13 "Package outline SOT363 (SC-88)"</a>: updated</li><li><a href="#">Figure 14 "Package outline SOT666"</a>: updated</li></ul>		
PBL1501Y_PBL1501V_1	20041105	Product data sheet	-	-

## 11. Legal information

### 11.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



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