1. MAX V Device Family Overview

MV51001-1.2

The MAX® V family of low cost and low power CPLDs offer more density and I/Os per footprint versus other CPLDs. Ranging in density from 40 to 2,210 logic elements (LEs) (32 to 1,700 equivalent macrocells) and up to 271 I/Os, MAX V devices provide programmable solutions for applications such as I/O expansion, bus and protocol bridging, power monitoring and control, FPGA configuration, and analog IC interface.

MAX V devices feature on-chip flash storage, internal oscillator, and memory functionality. With up to 50% lower total power versus other CPLDs and requiring as few as one power supply, MAX V CPLDs can help you meet your low power design requirement.

This chapter contains the following sections:

Feature Summary

The following list summarizes the MAX V device family features:

- Low-cost, low-power, and non-volatile CPLD architecture
- Instant-on (0.5 ms or less) configuration time
- Standby current as low as 25 µA and fast power-down/reset operation
- Fast propagation delay and clock-to-output times
- Internal oscillator
- Emulated RSDS output support with a data rate of up to 200 Mbps
- Emulated LVDS output support with a data rate of up to 304 Mbps
- Four global clocks with two clocks available per logic array block (LAB)
- User flash memory block up to 8 Kbits for non-volatile storage with up to 1000 read/write cycles
- Single 1.8-V external supply for device core
- MultiVolt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V logic levels
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors
- Schmitt triggers enabling noise tolerant inputs (programmable per pin)

- I/Os are fully compliant with the PCI-SIG® PCI Local Bus Specification, revision 2.2 for 3.3-V operation
- Hot-socket compliant
- Built-in JTAG BST circuitry compliant with IEEE Std. 1149.1-1990

Table 1–1 lists the MAX V family features.

Table 1–1. MAX V Family Features

Feature	5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
LEs	40	80	160	240	570	1,270	2,210
Typical Equivalent Macrocells	32	64	128	192	440	980	1,700
User Flash Memory Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192	8,192
Global Clocks	4	4	4	4	4	4	4
Internal Oscillator	1	1	1	1	1	1	1
Maximum User I/O pins	54	79	79	114	159	271	271
t_{PD1} (ns) *(1)*	7.5	7.5	7.5	7.5	9.0	6.2	7.0
f_{CNT} (MHz) *(2)*	152	152	152	152	152	304	304
t_{SU} (ns)	2.3	2.3	2.3	2.3	2.2	1.2	1.2
t_{CO} (ns)	6.5	6.5	6.5	6.5	6.7	4.6	4.6

Notes to Table 1–1:

(1) t_{PD1} represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.

(2) The maximum global clock frequency, f_{CNT}, is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.

MAX V devices accept 1.8 V on their VCCINT pins. The 1.8-V V_{CCINT} external supply powers the device core directly. MAX V devices operate internally at 1.8 V. The supported MultiVolt I/O interface voltage levels (V_{CCIO}) are 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

MAX V devices are available in two speed grades: –4 and –5, with –4 being the fastest. For commercial applications, speed grades –C4 and –C5 are available. For industrial and automotive applications, speed grade –I5 and –A5 are available, respectively. These speed grades represent the overall relative performance, not any specific timing parameter.

For propagation delay timing numbers within each speed grade and density, refer to the *DC and Switching Characteristics for MAX V Devices* chapter.

MAX V devices are available in space-saving FineLine BGA (FBGA), Micro FineLine BGA (MBGA), plastic enhanced quad flat pack (EQFP), and thin quad flat pack (TQFP) packages (refer to Table 1–2 and Table 1–3). MAX V devices support vertical migration within the same package (for example, you can migrate between the 5M570Z, 5M1270Z, and 5M2210Z devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide

the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

Table 1–2. MAX V Packages and User I/O Pins ***(Note 1)***

Device	64-Pin MBGA	64-Pin EQFP	68-Pin MBGA	100-Pin TQFP	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	324-Pin FBGA
5M40Z	30	54	—	—	—	—	—	—
5M80Z	30	54	52	79	—	—	—	—
5M160Z	—	54	52	79	79	—	—	—
5M240Z	—	—	52	79	79	114	—	—
5M570Z	—	—	—	74	74	114	159	—
5M1270Z	—	—	—	—	—	114	211	271
5M2210Z	—	—	—	—	—	—	203	271

Note to Table 1–2:

(1) Device packages under the same arrow sign have vertical migration capability.

Table 1–3. MAX V Package Sizes

Package	64-Pin MBGA	64-Pin EQFP	68-Pin MBGA	100-Pin TQFP	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	324-Pin FBGA
Pitch (mm)	0.5	0.4	0.5	0.5	0.5	0.5	1	1
Area (mm^2)	20.25	81	25	256	36	484	289	361
Length × width (mm × mm)	4.5 × 4.5	9 × 9	5 × 5	16 × 16	6 × 6	22 × 22	17 × 17	19 × 19

Integrated Software Platform

The Quartus II software provides an integrated environment for HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, and programming of MAX V devices.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

You can debug your MAX V designs using In-System Sources and Probes Editor in the Quartus II software. This feature allows you to easily control any internal signal and provides you with a completely dynamic debugging environment.

For more information about the In-System Sources and Probes Editor, refer to the *Design Debugging Using In-System Sources and Probes* chapter of the *Quartus II Handbook*.

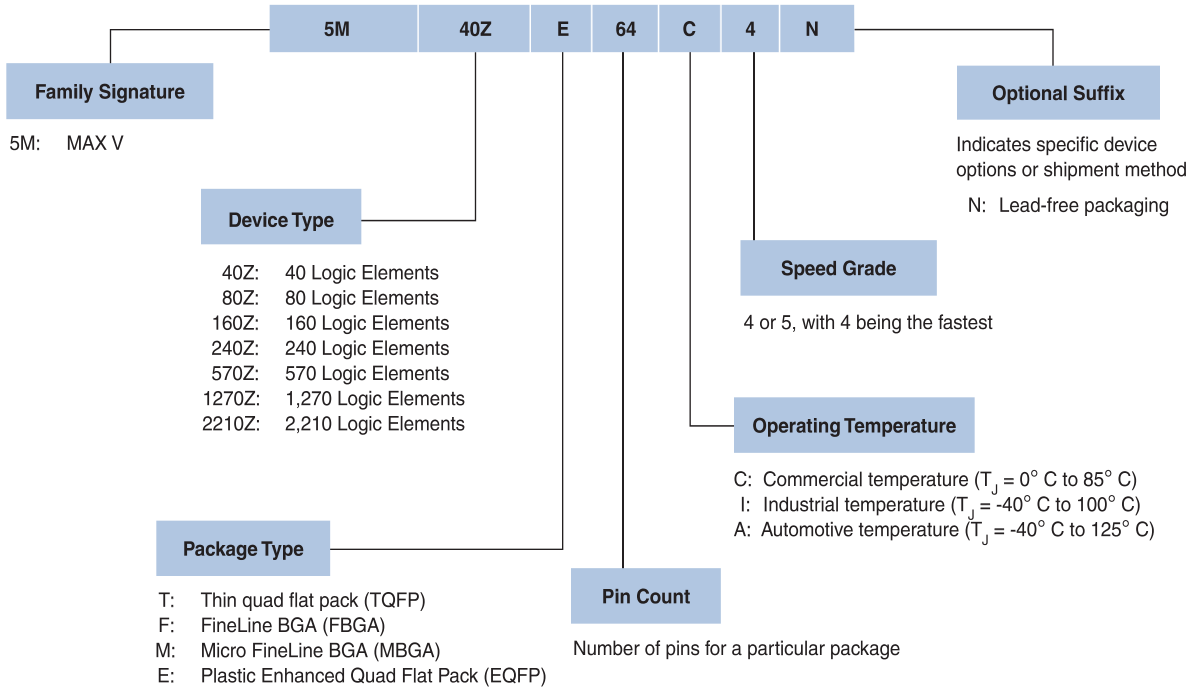
Device Pin-Outs

For more information, refer to the MAX V Device Pin-Out Files page.

Ordering Information

Figure 1–1 shows the ordering codes for MAX V devices.

Figure 1–1. MAX V Device Packaging Ordering Information



Document Revision History

Table 1–4 lists the revision history for this chapter.

Table 1–4. Document Revision History

Date	Version	Changes
May 2011	1.2	■ Updated Figure 1–1. ■ Updated Table 1–3.
January 2011	1.1	Updated “Feature Summary” section.
December 2010	1.0	Initial release.