PIC18(L)F24/25K42

PIC18(L)F24/25K42 Silicon Errata and Data Sheet Clarification

The PIC18(L)F24/25K42 devices that you have received conform functionally to the current Device Data Sheet (DS40001869**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F24/25K42 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18(L)F24/25K42 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID<13:0>(1), (2)	Revision ID for Silicon Revision
		A1
PIC18F24K42	6CA0h	A001
PIC18LF24K42	6DE0h	A001
PIC18F25K42	6C80h	A001
PIC18LF25K42	6DC0h	A001

Note 1: The Revision ID is located in addresses 3FFFFCh-3FFFFDh and Device ID is located in addresses 3FFFFEh-3FFFFFh.

2: Refer to the *"PIC18(L)F24/25K42 Memory Programming Specification"* (DS40001836) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)
				A1
Direct Memory Access (DMA)	Hard Stop	1.1	Stopping DMA transfers by clearing EN (DMAxCON0 register).	X
Analog-to-Digital Converter (ADC)	ADC RC Oscillator	2.1	ADC RC Oscillator not functional.	X
UART	Flow Control PPS	3.1	Flow control affected by PPS.	X
UART	Flow Control Transmit Driver	3.2	Flow control transmit driver enable (TXDE) is low true.	X
UART	DALI Mode Auto-Baud	3.3	DALI mode always auto-bauds on the Start bit.	X
UART	DMX Mode Make After Break	3.4	Make after Break period is less than required by the DMX specification.	X
UART	RXIDL Status Bit	3.5	RXIDL remains clear after auto-baud overflow.	X
UART	TXMTIF Interrupt Flag	3.6	TXMTIF flag is delayed by two instruction cycles.	X
I^2C	Multi-Master Mode Transmission	4.1	Multi-Master mode transmission.	X
I^2C	10-bit Master Mode Reception	4.2	Automatic restart in 10-bit Master reception.	X
I^2C	NACKIF Interrupt Flag	4.3	Operation of NACKIF Flag.	X
I^2C	Auto-Count	4.4	Auto-count feature in 10-bit Master Reception mode.	X
I^2C	TXIF Interrupt Flag	4.5	TXIF flag is set for 7/10 bit reads when ADBDIS = 1.	X
Program Flash Memory	Endurance of PFM Cell for LF Devices	5.1	Endurance of the PFM cell is lower than specified.	X
Signal Measurement Timer (SMT)	MFINTOSC Clock Sources into SMT	6.1	MFINTOSC clock sources into the SMT are not functional.	X
Electrical Specifications	SMBus 2.0	7.1	SMBus 2.0 logic levels.	X
Electrical Specifications	SMBus 3.0	7.2	SMBus 3.0 logic levels.	X
Electrical Specifications	Nonvolatile Memory (NVM) Endurance for LF Devices	7.3	NVM self-writes on LF devices may not work properly at specified voltage levels and temperatures.	X
Electrical Specifications	Fixed Voltage Reference (FVR) Accuracy	7.4	FVR output tolerance may be higher than specified at temperatures below -20°C.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: Direct Memory Access (DMA)

1.1 Hard Stop

When a DMA transaction is stopped in the middle of the transfer (XIP bit is set) by clearing the Enable bit (hard-stop), the destination address can be written to with `0x00`. This only happens if the very next cycle (after clearing enable) can provide the DMA access to the SRAM bus.

Work around

Clearing the DGO bit before hard-stop will prevent the destination being written to with `0x00`.

Affected Silicon Revisions

A1							
X							

2. Module: Analog-to-Digital Converter (ADC)

2.1 ADC RC Oscillator

Incorrect ADC operation when using clock supplied from dedicated FRC Oscillator (i.e., CS bit is set in ADCON0 register).

Work around

Use ADC clock supplied by FOSC for ADC operation.

Affected Silicon Revisions

A1							
X							

3. Module: UART

3.1 Flow Control PPS

Unimplemented PPS input selections for UART1 and UART2 may interfere with hardware flow control when that feature is enabled.

Work around

Set SFRs 0x3AE7 and 0x3AEA to 0x18.

Affected Silicon Revisions

A1							
X							

3.2 Flow Control Transmit Driver

The TXDE output is active-low whereas the DE input of RS-485 transceivers need a active-high signal to enable the transmit drivers.

Work around

Use PPS to route TXDE to a pin and then use a CLC module to input and invert the signal on that pin and use PPS to output that CLC to another pin.

Affected Silicon Revisions

A1							
X							

3.3 DALI Mode Auto-Baud

The auto-baud feature is always enabled in DALI mode regardless of the value of the ABDEN control bit. This will adversely affect data reception when the mid-bit transition of the Manchester data is offset by more than 14%.

Work around

None.

Affected Silicon Revisions

A1							
X							

3.4 DMX Mode Make After Break

In DMX Console mode the MAB period is 8 µs. The specification requires a minimum of 12 µs.

Work around

The UART uses only the BREAK time to determine the start of a new frame. Therefore, the short MAB period does not affect DMX operation when using this UART as equipment and no work-around is required. However, equipment using other devices for reception may be affected, in which case, 8-bit Asynchronous mode must be used with software control of all of the DMX Console operations.

Affected Silicon Revisions

A1							
X							

3.5 RXIDL Status Bit

The RXIDL bit properly stays low until the 5th rising edge after auto-baud starts. If auto-baud overflows and is subsequently cleared by software, then RXIDL improperly remains low until the 5th rising edge.

Work around

If RXIDL is low after an auto-baud overflow then cycle the RXEN or ON bit to restore normal operation.

Affected Silicon Revisions

A1							
X							

3.6 TXMTIF Interrupt Flag

The TXMTIF flag goes low two instruction cycles after the TXB register is written. The bit cannot be polled or interrupt enabled immediately after writing the TXB register.

Work around

Allow at least two instruction cycles after writing TXB before enabling the TXMTIF interrupt or starting to poll the TXMTIF flag.

Affected Silicon Revisions

A1							
X							

4. Module: I^2C

4.1 Multi-Master Mode Transmission

When the I^2C is configured in Multi-Master mode and is operating in Slave Transmission mode, writes to the transmit buffer will set the S (Start) bit in I2CxCON0 register. When the bus becomes free (i.e., BFRE = 1) after slave transmission is complete then the Multi-Master behaves as a master and initiates a transaction. The master will either send the content of address buffer (ADBDIS = 0) or transmit buffer (ADBDIS = 1).

Work around

Clear the Start bit just before the Stop condition of slave transmission occurs, this prevents a false addressing sequence on the I^2C Bus.

Affected Silicon Revisions

A1							
X							

4.2 10-Bit Master Mode Reception

When ADBDIS = 1, user software writes to the transmit buffer with the slave address. After the addressing sequence is complete, the user software writes the read address to the transmit buffer while the master is paused for restart (i.e., MDR = 1 & I2CCNT = 0 & MMA = 1). However, a restart does not occur when the transmit buffer is written to.

Work around

The user has to load the transmit buffer and additionally set the S (Start) bit to initiate the restart sequence.

Affected Silicon Revisions

A1							
X							

4.3 NACKIF Interrupt Flag

The NACKIF flag is set on the slave even if the master transmits a non-matching slave address.

Work around

Enable NACKIE only when SMA = 1 to avoid unwanted interrupts.

Affected Silicon Revisions

A1							
X							

4.4 Auto-Count

When the ACNT bit I2CxCON2 register is set before the master transmits the high address byte. Then the MDR bit is set after the 8th SCL pulse, preventing the completion of the addressing sequence.

Work around

Set the ACNT bit after the addressing sequence is complete and when the master is paused for restart (i.e., MDR = 1 & I2CCNT = 0 & MMA = 1).

Affected Silicon Revisions

A1							
X							

4.5 TXIF Interrupt Flag

When ADBDIS = 1, the address is sent through the transmit buffer. Even if it is a read address, the TXIF flag is set as the data was moved out of the transmit buffer.

Work around

For I^2C Master read, ignore TXIF flag if ADBDIS = 1.

Affected Silicon Revisions

A1							
X							

5. Module: Program Flash Memory

5.1 Endurance of PFM Cell for LF Devices

The Flash memory cell endurance specification (Parameter MEM30) for PIC18LF24/25K42 devices is 1K cycles.

Work around

None.

Affected Silicon Revisions

A1							
X							

6. Module: Signal Measurement Timer (SMT)

6.1 MFINTOSC Clock Sources into SMT

The Signal Measurement Timer does not operate when MFINTOSC is selected as the clock source (i.e., CSEL = 0b100 and 0b101). The MFINTOSC does not start up automatically.

Work around

User software needs to manually enable the MFINTOSC by setting the MFOEN bit in the OSCCEN register. The MFINTOSC will remain enabled as long as the MFOEN bit is set.

Affected Silicon Revisions

A1							
X							

7. Module: Electrical Specifications

7.1 SMBus 2.0

The SMBus 2.0 V_{IL} specification (Parameter D304) at 125°C is 0.7V.

Work around

None.

Affected Silicon Revisions

A1							
X							

7.2 SMBus 3.0

The SMBus 3.0 V_{IL} specification (Parameter D305) is temperature and V_{DD} dependent. Refer to the table below.

Temperature	V_{DD}	D305 SMBus 3.0 V_{IL} Specification
-40°C	1.8V	0.6V
-40°C	5.5V	0.8V
25°C	1.8V	0.6V
25°C	5.5V	0.8V
85°C	1.8V	0.6V
85°C	5.5V	0.7V
125°C	1.8V	0.5V
125°C	5.5V	0.7V

Work around

None.

Affected Silicon Revisions

A1							
X							

7.3 Nonvolatile Memory (NVM) for LF Devices

Performing self-writes through NVMREG access on LF version devices may not work at V_{DD} <2.0V and temperatures between -40°C and 25°C.

Work around

None.

Affected Silicon Revisions

A1							
X							

7.4 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001869**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (01/2017)

Initial release of this document.

Rev B Document (07/2017)

Added Module 6: SMT and Module 7: Electrical Specifications for LF Devices Only to Silicon Errata Issues. Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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ISBN: 978-1-5224-1899-3

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