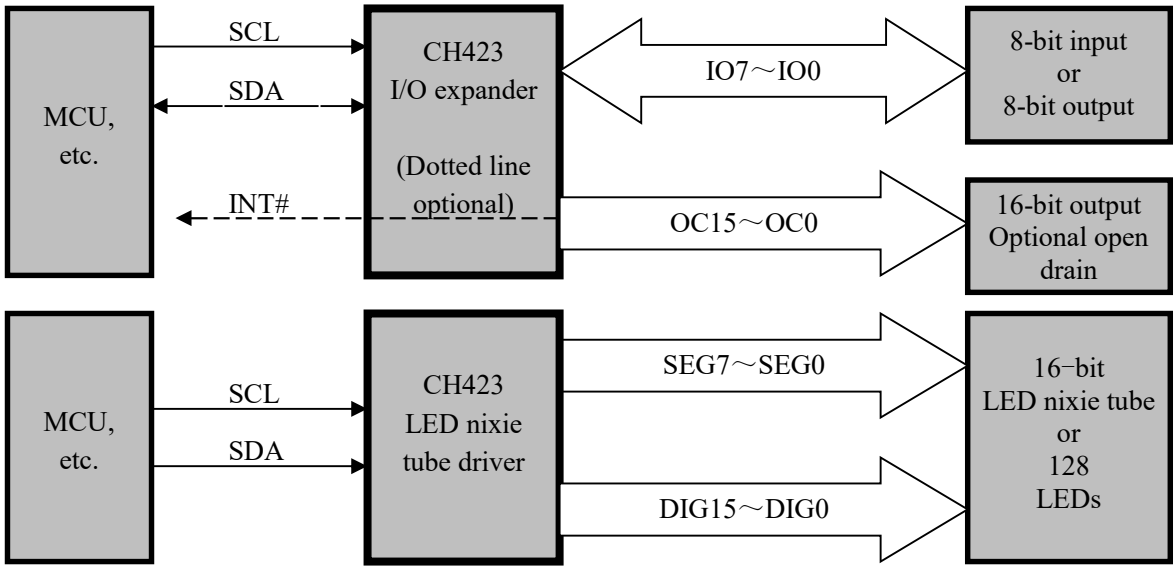
Two-wire Remote I/O Expander CH423

Datasheet
Version: 2A
http://wch.cn

1. Overview

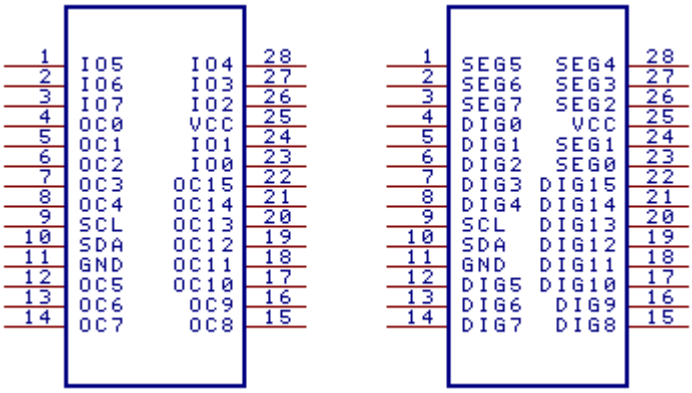
CH423 is a general remote I/O expander for the two-wire serial interface. CH423 provides 8 bidirectional I/O pins and 16 general purpose output pins, and supports input level change interrupt. CH423 has a built-in current drive circuit, which can drive 24 LEDs statically or 128 LEDs dynamically (equivalent to 16 LED nixie tubes). CH423 exchanges data with MCU through the two-wire serial interface.



2. Features

- 8 general purpose I/O pins, GPIOs, and 16 general purpose output pins, GPOs, are expanded remotely through a two-wire serial interface.
- Built-in current driving stage, continuous drive current not less than 15mA, OC pin output 1/16 pulse sinking current not less than 120mA.
- The static display drive mode supports 24 LEDs or 3 common anode LED nixie tubes.
- The time-sharing dynamic scanning display driving mode supports 128 LEDs or 16-bit common cathode LED nixie tubes, and supports brightness control.
- Bidirectional I/O pins have the function of input level change interrupt in the input mode, and the interrupt output is active at low level.
- 16 general purpose output pins can choose push-pull output or open-drain output.
- Support 3 to 5V supply voltage and low power sleep, can be woken up by input level change.
- High speed two-wire serial interface, clock speed from 0 to 1MHz, compatible with two-wire I^2C bus, saving pins.
- Provide DIP28S and SOP28 lead-free packages, compatible with RoHS.

3. Package



Package	Body size		Lead pitch		Description	Part No.
SOP28	7.62mm	300mil	1.27mm	50mil	Standard 28-pin patch	CH423S
DIP28S SK-DIP28	7.62mm	300mil	2.54mm	100mil	Skinny 28-pin dual in-line	CH423A

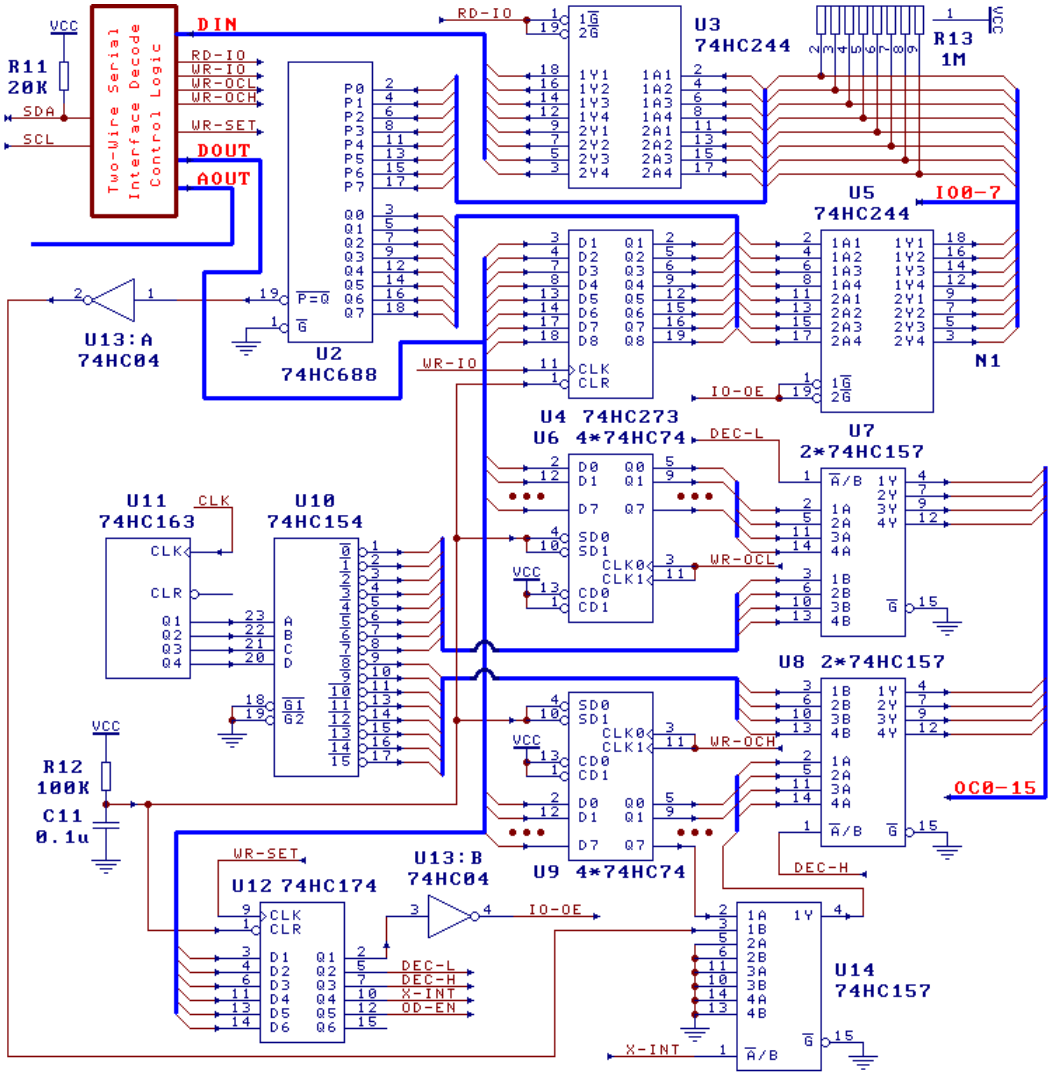
Note: CH423D in SDIP28 package (with 1.78mm lead pitch) has been discontinued. Select the patch package first.

4. Pin definitions

Pin No.	Pin Name	Pin Type	Pin description
25	VCC	Power	Positive power, continuous current not less than 150mA
11	GND	Power	Common ground, continuous current not less than 150mA
23,24,26, 27,28,1,2,3	IO0～IO7	Three-state output and input	Bidirectional input and output, built-in weak pull-up resistor Segment drive of common cathode LED nixie tube during dynamic scanning, active at high level
4～8、 12～22	OC0～ OC15	Push-pull or open-drain output	General-purpose output, optional open-drain output, active at low level Word drive of common cathode LED nixie tube during dynamic scanning, active at low level
10	SDA	Open-drain output and input	Data input and output of two-wire serial interface, built-in pull-up resistor
9	SCL	Input	Data clock of two-wire serial interface

5. Functional specification

5.1. Internal circuit principle (for function interpretation, excluding dynamic drive, for reference only)



5.2. General description

For data in this manual, those ending with B are binary numbers and those ending with H are hexadecimal numbers. Otherwise, they are decimal numbers. The bit marked as x indicates that the bit can be any value.

MCU (also CPU, DSP, microprocessor, MCU or other controller) controls CH423 chip through two-wire serial interface. The two-wire serial interface of CH423 is realized by hardware, and MCU can frequently carry out high-speed operation through the serial interface, without reducing the working efficiency of CH423.

5.3. Bidirectional I/O pins

The pins IO7-IO0 of CH423 are bidirectional I/O pins, the default direction is the input direction, and they are used to input the current state of external pins. When they are set to the output direction, high and low levels can be output to drive LEDs or expand I/O.

In the dynamic scan display drive mode, the pins IO7-IO0 can be used to drive the pins of each segment for the LED nixie tube. As the drive current of each segment can be limited inside CH423, the segment current limiting resistor externally connected in series can be eliminated.

5.4. General-purpose output pins

The pins OC15-OC0 of CH423 are push-pull or open-drain output pins, and are push-pull output pins by

default.

After the open-drain output mode is selected, there are only two states of "low level output" and "no output". High level cannot be output, and the default is "no output".

In dynamic scan display drive mode, the pins OC15-OC0 can be used to drive each common terminal of the common cathode LED nixie tube, and can absorb large sinking current in pulse mode.

If only 8-bit LED nixie tube is driven, the remaining 8 general-purpose output pins can still be used for GPO.

5.5. Level change interrupt

If the input level change interrupt is allowed, OC15 pin of CH423 will act as an interrupt request output pin, active at low level.

When the pins IO7-IO0 of CH423 are used for input, they support input level change interrupt. Input level change means that the current state input from the pins IO7-IO0 is detected to be different from the data in the output register (U4 in the figure) written in advance to the pins IO7-IO0. If the above change is detected (U2 is a comparator in the figure), CH423 will output active low interrupt through OC15 pin until MCU rewrites into the output register of the pins IO7-IO0. Moreover, when the new value is the same as the current state input from the pins IO7-IO0, OC15 pin of CH423 is restored to high level or does not output.

5.6. Power on reset

CH423 has built-in power on reset circuits (R12 and C11 in the figure), which are used to restore the internal registers to the default state when the chip is just powered on. For example, after each power-on, the bidirectional I/O pin is in the input state and the general-purpose output pin is in the high level state.

5.7. Serial interface

CH423 has a two-wire serial interface realized by hardware, including two main signal lines: serial data clock input line SCL, serial data input and output line SDA.

SDA is a quasi-bidirectional signal line with pull-up resistors, and is at high level by default. SDA is used for serial data input and output. The high level represents bit data 1, and the low level represents bit data 0. The sequence of serial data input is that the high bit is at the front and the low bit is at the back.

The SCL is the input signal line, which is at high level by default. SCL is used to provide a serial clock, CH423 inputs data from SDA on its rising edge and outputs data from SDA on its falling edge.

SDA falling edge occurring during the SCL high level period is defined as the start signal of the serial interface, and SDA rising edge occurring during the SCL high level period is defined as the stop signal of the serial interface. CH423 receives and analyzes the command only after detecting the start signal. Therefore, when I/O pin resources of MCU are short, SCL pin can be shared with other interface circuits while SDA pin state is unchanged. Both SCL and SDA pins can be shared with other interface circuits if it is possible to ensure that SDA pin changes only when SCL pin is at low level.

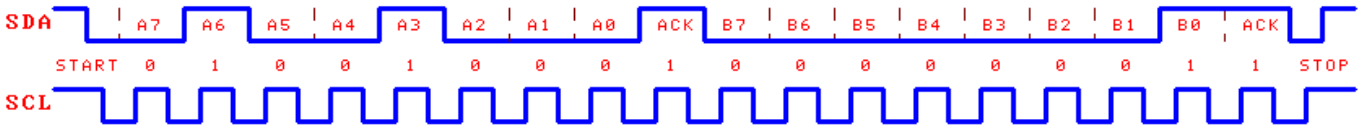
The communication process between MCU and CH423 is always divided into six steps. According to the operation direction of MCU, it is divided into two types: write operation for output data and read operation for input data. For the specific process, please refer to Example Program.

Write operation consists of six steps: output start signal, output byte 1, response 1, output byte 2, response 2 and output stop signal. Among them, the start signal and the stop signal are as mentioned above, response 1 and response 2 are always fixed to 1, output byte 1 and output byte 2 respectively contain 8 data bits, namely, one byte of data.

Read operation consists of six steps: output start signal, output byte 1, response 1, input byte 2, response 2

and output stop signal. Among them, the start signal and the stop signal are as mentioned above, response 1 and response 2 are always fixed to 1, output byte 1 and input byte 2 respectively contain 8 data bits, namely, one byte of data.

The following figure shows an example of write operation. The byte 1 is 01001000B, namely, 48H; the byte 2 is 00000001B, namely, 01H.



5.8. Dynamic drive LED nixie tube

CH423 can drive 16 common cathode LED nixie tubes directly and dynamically. After the pins on the same segments of all LED nixie tubes are connected in parallel (segments A-G and decimal point), they are connected with the segment drive pins IO7-IO0 of CH423 through 8 current limiting resistor R1-R8 connected in series. The common cathodes of the LED nixie tube are driven by the pins OC15-OC0 of CH423 respectively. The resistor RN8 connected with the segment pins in series is used to limit and balance the segment drive current. At the supply voltage of 5V, the series resistance 270Ω often corresponds to the segment current 10mA. CH423 can be connected to an 8×16 matrix LED array or 128 independent LEDs, or support a common anode LED nixie tube through an external inverting driver, or support a large size LED nixie tube through an external high-power tube. Refer to the method in CH452 data manual.

CH423 has sixteen 8-bit data registers (equivalent to sixteen U4 in the figure), which are used to store 16 word data, corresponding to 16 LED nixie tubes or 16 groups of LEDs, 8 LEDs in each group. The bits 7-0 of the word data in the data register correspond to the decimal points and segments G-A of 8 LED nixie tubes respectively. For LED array, the data bit of each word data uniquely correspond to an LED. When the data bit is 1, the segment of the corresponding LED nixie tube or LED will be on; when the data bit is 0, the segment of the corresponding LED nixie tube or LED will be off. For example, the bit 0 of the third data register is 1, so the segment A of the corresponding third LED nixie tube is on. The following diagram shows the segment name of the LED nixie tube.

6. Operation commands

The operation commands of CH423 are divided into 6 groups. Start signal, stop signal, response 1 and response 2 are the same for each command, except that the data of output bytes 1 and byte 2 are different and that byte 2 is transmitted in different direction. Byte 1 is used for two-wire serial port control logic, or used for generating addresses (AOUT bus in figure), and byte 2 is used for input and output data (DIN and DOUT buses in figure).

6.1. System parameter setting command (WR-Set Control Line in Figure)

The output byte 1 of this command is 01001000B, namely 48H; the command supports seven system parameters, and the output byte 2 is [SLEEP][INTENS][OD_EN][X_INT][DEC_H][DEC_L][IO_OE]B.

Set System Parameter command is used to set the system-level parameters of CH423 (written to U12 in the figure): output enable IO_OE of bidirectional I/O pins IO7-IO0, dynamic scan enable DEC_L of output pins

OC7-OC0, dynamic scan enable DEC_H of OC15-OC8, input level change interrupt enable X_INT, open-drain output enable OD_EN of output pins OC15-OC0, dynamic display driver brightness control INTENS, low power sleep control SLEEP. After power-on reset, the above parameters are 0 by default.

IO_OE is used to control the three-state output of bidirectional I/O pins IO7-IO0. When it is 0, the output is disabled (it is used for input through U3 in the figure); when it is 1, the output is enabled (U5 output in the figure).

DEC_L is used to control the dynamic scan enable of output pins OC7-OC0. When it is 0, OC7-OC0 are used for general output of I/O extension (select U6 in the figure). When it is 1, OC7-OC0 are controlled by the timing scan counter after decoding (select U10 in the figure). At the same time, one of the pins OC7-OC0 is selected to output the low level, the rest of the pins do not output and are used to realize the time-sharing display drive.

DEC_H is used to control the dynamic scan enable of output pins OC15-OC8. When it is 0, OC15-OC8 are used for general output of I/O extension (select U9 in the figure). When it is 1, OC15-OC8 are controlled by the timing scan counter after decoding (select U10 in the figure). At the same time, one of the pins OC15-OC8 is selected to output the low level, the rest of the pins do not output and are used to realize the time-sharing display drive.

X_INT is used to enable an input level change interrupt (control U14 in the diagram). A level change interrupt is disabled when it is 0, and an output level change interrupt is allowed from the pin OC15 when it is 1 and DEC_H is 0 (generated by U2 comparison in the diagram).

OD_EN is used to enable the open-drain output of the pins OC15-OC0. When it is 0, OC15-OC0 are push-pull output pins (outputting low level and high level); when it is 1, OC15-OC0 are open-drain output pins (only outputting low level or not outputting).

INTENS is used to control the brightness of the dynamic display driver, which contains two-bit data and has 4 combinations: data 00B, 01B and 10B respectively set the duty cycle of the display driver to 4/4, 1/4 and 2/4, and enable the internal segment drive current limiter. Data 11B sets the display drive duty cycle to 4/4, but the internal segment drive current limiter is disabled, so the external segment pin is required to be connected with the current limit resistors R1-R8 in series.

SLEEP is used to put CH423 into a low-power sleep state, so as to save power. CH423 in low-power sleep state can be woken up by any of the following two events. The first event is input level change, that is, the current state input by the pins IO7-IO0 is different from the data in the output register (U4 in the figure) previously written into the pins IO7-IO0. The second event is receiving of next operation command sent by MCU. When CH423 is waken up, SLEEP bit is automatically reset to 0. Sleep and Wake Up operations do not affect other working states of CH423. If CH423 is woken up by the former event, it will also generate a level change interrupt.

For example, when the output byte 2 is 17H, the pins OC15-OC0 dynamically drive 16 LED nixie tubes in the open-drain mode; when the output byte 2 is 03H, only the pins OC7-OC0 dynamically drive 8 LED nixie tubes, and the remaining pins OC15-OC8 are still used for general-purpose output GPO; when the output byte 2 is 05H, only the pins OC15-OC8 dynamically drive 8 LED nixie tubes, and the remaining pins OC7-OC0 are still used for the general-purpose output GPO.

This command does not affect the data in the output registers of the pins and the internal data buffer.

6.2. Set low 8-bit general output command (WR-OCL Control Line in Figure)

The output byte 1 of this command is 44H, and the output byte 2 is [OC_L_DAT]B, namely, 8-bit data from 00H to 0FFH, to write the output register of the output pins OC7-OC0 (U6 in the figure). If 0 is written, the pin will output low level; if 1 is written, the pin will output high level.

6.3. Set high 8-bit general output command (WR-OCH Control Line in Figure)

The output byte 1 of this command is 46H, and the output byte 2 is [OC_H_DAT]B, namely, 8-bit data from 00H to 0FFH, to write the output register of the output pins OC715-OC8 (U9 in the figure). If 0 is written, the pin will output low level; if 1 is written, the pin will output high level.

6.4. Set bidirectional I/O command (WR-IO Control Line in Figure)

The output byte 1 of this command is 60H, 62H, 64H, 66H, 68H, 6AH, 6CH, 6EH, 70H, 72H, 74H, 76H, 78H, 7AH, 7CH and 7EH, where bits 4-1 are the address, which can be ignored; the output byte 2 is [IO_DAT]B, namely, 8-bit data from 00H to 0FFH, to write the output register of bidirectional I/O pins IO7-IO0 (U4 in the figure). If IO_OE is 1, output will be allowed; if 0 is written, the pin will output low level; if 1 is written, the pin will output high level.

6.5. Load word data command (used for LED nixie tube automatic dynamic display driver, the command code is the same as Set Bidirectional I/O Command)

The byte 1 of the command is 011[DIG_ADDR]0B, i.e. 60H, 62H, 64H, 66H, 68H, 6AH, 6CH, 6EH, 70H, 72H, 74H, 76H, 78H, 7AH, 7CH and 7EH; byte 2 is [DIG_DATA]B, i.e. the value between 00H and 0FFH.

"Load Word Data Command" is used to write the word data DIG_DATA to the data register at the specified address DIG_ADDR. DIG_ADDR specifies the address of the data register through 4-bit data. Data 0000B-1111B specify the addresses 0-15 respectively, corresponding to 16 LED nixie tubes driven by the pins OC0-OC15. DIG_DATA is 8-bit word data. For example, command data 01100000B and 01111001B means that word data 79H is written into the first data register so that the LED nixie tube driven by the pin OC0 will display E.

The data in CH423 internal data register is uncertain after power on reset, so the data in the data register shall be cleared or the data to be displayed shall be directly loaded before the display is started. The reset process does not affect the data in the data register.

6.6. Read bidirectional I/O command (RD-IO Control Line in Figure)

The output byte 1 of this command is 01001101B, namely, 4DH; the input byte 2 is the current pin state of bidirectional I/O pins IO7-IO0.

Read Bidirectional I/O Command is used to get the current state of the pins IO7-IO0. When IO_OE is 0, the input state will be gotten, otherwise the output state will be gotten. The command is read operation, only command with data return. MCU must first release SDA pin (three-state output is disabled or pulled up to the high level), and then CH423 outputs the current pin state from SDA pin.

When CH423 is used for the LED nixie tube display driver, the external 8 key input states can be read after the display is temporarily turned off.

7. Parameters

7.1. Absolute maximum ratings

Operating in critical ratings or exceeding the absolute maximum ratings may cause the chip to work abnormally or even be damaged.

Symbol	Parameter description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)	-0.5	6.0	V

VIO	Voltage on the input or output pins	-0.5	VCC+0.5	V
IMoc	Continuous drive current on single OC pin	0	30	mA
IMocp	1/16 pulse drive current on single OC pin	0	150	mA
IMio	Continuous drive current on single IO pin	-25	25	mA
IMall	Total continuous drive current on all IO pins Or total continuous drive current on all OC pins	0	160	mA

7.2. Electrical characteristics

Test conditions: TA=25℃, VCC=5V; if VCC=3.3V, the current in the table shall be multiplied by 40%.

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VCC	Supply voltage	2.9	5	5.3	V
ICC	Operating current	0.1	80	120	mA
ICCs5	Static current at 5V (SCL and SDA are at high level)		0.4	0.9	mA
ICCs3	Static current at 3.3V (SCL and SDA are at high level)		0.1	0.3	mA
VIL	Low level input voltage of SCL and SDA pins	-0.5		0.8	V
VIH	High level input voltage of SCL and SDA pins	2.0		VCC+0.5	V
VILio	Low level input voltage of IO pin	-0.5		0.6	V
VIHio	High level input voltage of IO pin	1.9		VCC+0.5	V
VOLoc	Low level output voltage of OC pins (-100mA)		0.6	0.8	V
VOLoc	Low level output voltage of OC pins (-30mA)		0.2	0.3	V
VOHoc	High level output voltage of OC pins (5mA)	VCC-0.5			V
VOLio	Low level output voltage of IO pins (-15mA)			0.5	V
VOHio	High level output voltage of IO pins (20mA)	VCC-0.5			V
VOL	Low level output voltage of SDA pin (-4mA)			0.5	V
IUP1	Input weak pull-up current of IO pin	1	5	10	uA
IUP2	Input pull-up current of SDA pin	150	250	400	uA
VR	Default voltage threshold of power on reset	2.3	2.6	2.9	V

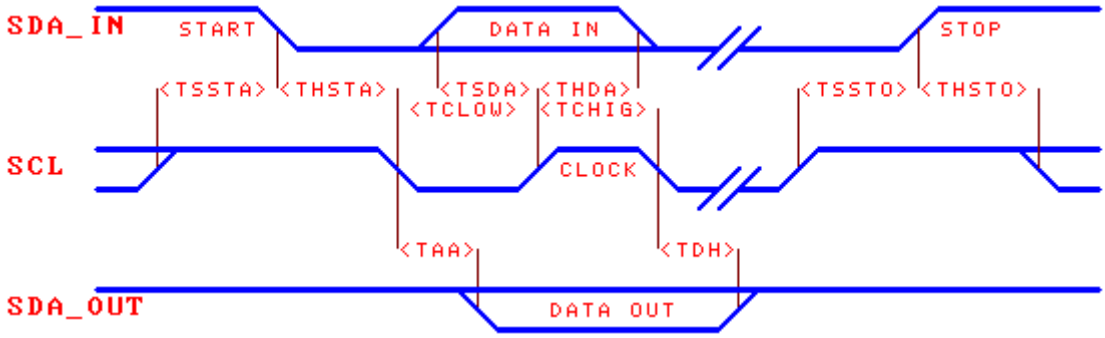
7.3. Timing parameters

Test conditions: TA=25℃, VCC=5V, Refer to the Attached Drawing.

(Note: The unit of measurement in this table is nanosecond, namely, 10^{-9} seconds. If the maximum value is not indicated, the theoretical value can be infinite.)

Symbol	Parameter description	Min.	Typ.	Max.	Unit
TPR	Reset time generated during power on detection	15	30	80	mS
TSSTA	Setup time of SDA falling edge start signal	100			nS

THSTA	Hold time of SDA falling edge start signal	100			nS
TSSTO	Setup time of SDA rising edge stop signal	100			nS
THSTO	Hold time of SDA rising edge stop signal	100			nS
TCLOW	Low level width of SCL clock signal	100			nS
TCHIG	High level width of SCL clock signal	100			nS
TSDA	Setup time of SDA input data to SCL rising edge	30			nS
THDA	Hold time of SDA input data to SCL rising edge	10			nS
TAA	Delay SDA output data to SCL falling edge	3		30	nS
TDH	Delay of invalid SDA output data to SCL falling edge	3		40	nS
Rate	Average data transmission rate	0		1M	bps

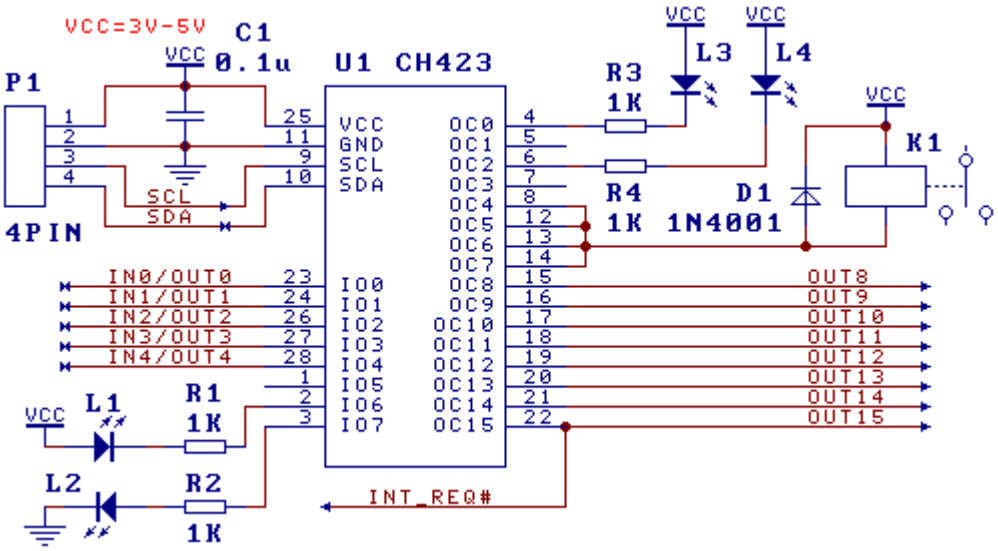


8. Application

8.1. Remote I/O extension

CH423 is connected to the external MCU through two-wire serial interfaces SCL and SDA, and the capacitor C1 is used for power supply decoupling.

The pins IO7-IO0 of CH423 can be used for input or output. In the figure, the pins IO6 and IO7 are used to drive two-polarity LED. The pins OC15-OC0 pins of CH423 can only be used for output. In order to get a larger continuous current drive capability, the open-drain output can be enabled, and the pins OC4, OC5, OC6 and OC7 can be connected in parallel according to the figure to drive the relay K1.

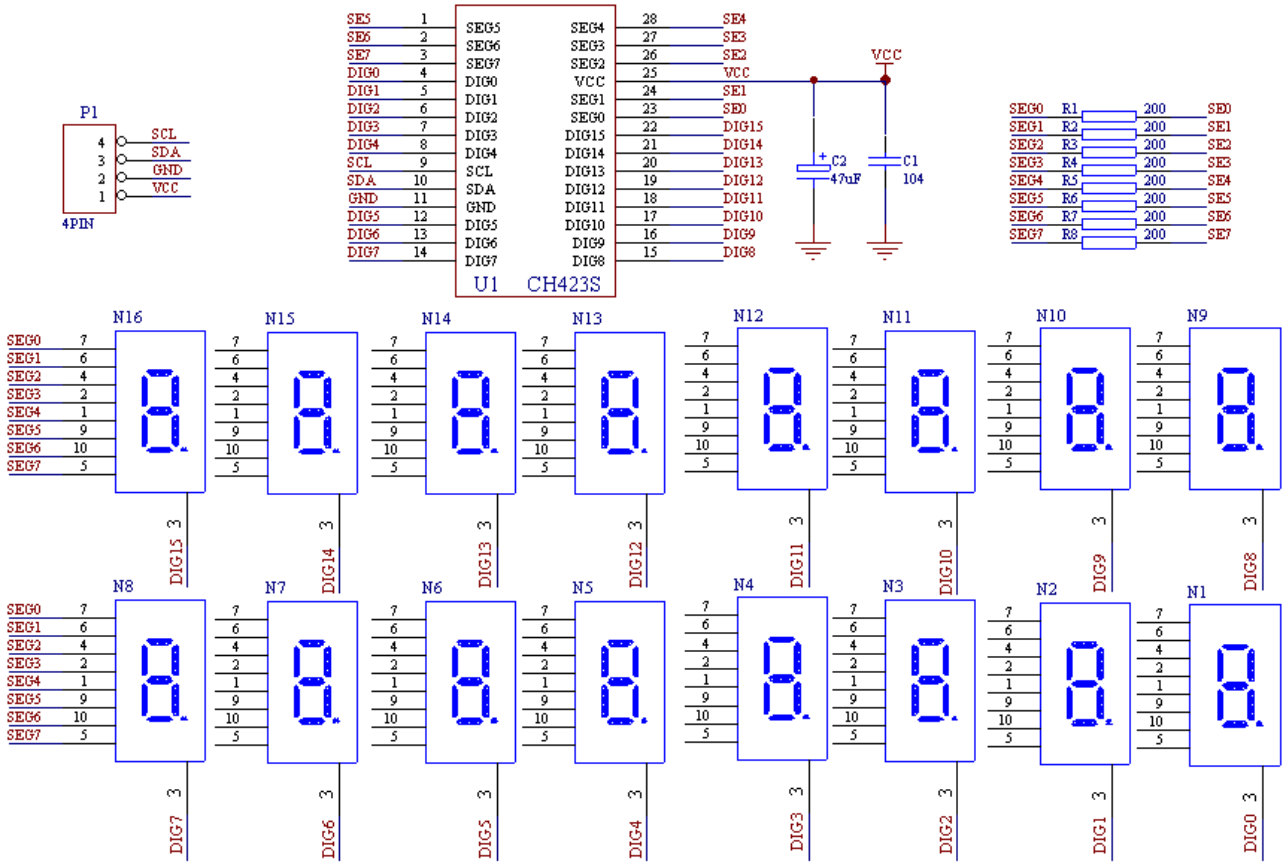


8.2. Dynamic display drive

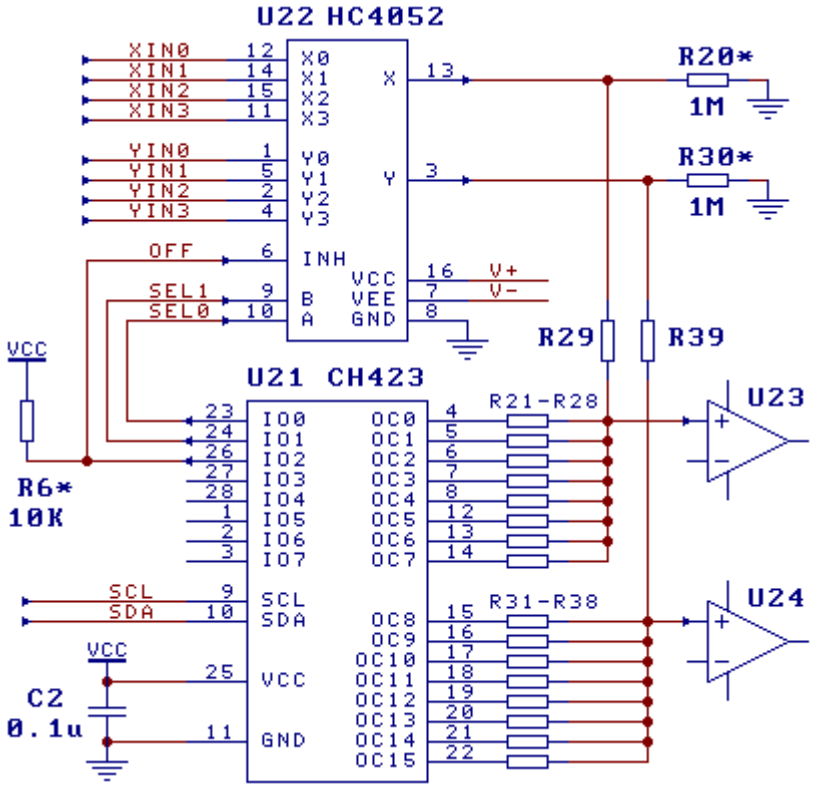
The dynamic display drive mode of CH423 is used to drive 128 LEDs or 16 common cathode LED nixie tubes. The pins IO7-IO0 respectively drive the pins of each segment for the common cathode LED nixie tubes (the LED nixie tubes are connected in parallel), and the pins OC15-OC0 respectively drive the common terminal of the common cathode LED nixie tubes. After MCU loads all the word data, the control bits DEC_L and DEC_H are turned on, and CH423 automatically performs time-sharing dynamic display scan.

If only 8 LED nixie tubes are required to be driven, only one of the control bits DEC_L or DEC_H can be turned on, and the remaining 8 general-purpose output pins can still be used for general output.

CH423 can internally limit the segment drive current, so the current limiting resistors R1-R8 connected to the segment pins can be eliminated.



8.3. Digital potentiometer



The OC pin of CH423 in the open-drain output mode is a low-resistance open-drain output pin, has the on resistance less than 10Ω, and can be used as an analog switch with one end grounded. After multiple OC pins are connected with their respective external resistors and combined for turn-on, a digital programmable resistor with one end grounded can be formed.

For example, 9 external resistors can form a digital potentiometer, and a maximum of 256 resistances can be gotten after any parallel combination of 8 resistors, from which no less than 32 effective resistances can be selected (meeting the requirement that the resistances increase in a certain way). The figure below shows a double-channel digital potentiometer consisting of 18 external resistors. MCU controls resistors R21-R28 to be independently ON to ground through CH423 to get a programmable pull-down resistor with 256-level resistance. After the pull-down resistor divides voltage with R29, a programmable voltage division output is generated and provided to the operational amplifier U23 of the latter stage, realizing the function of the digital potentiometer. R31-R39 in the figure constitute another channel.

U22 in the figure is a one-of-four analog switch. MCU controls the analog switch through CH423 to select the input channel, and then 9 resistors R21-R29 perform the programmable voltage division output. The optional pull-up resistor R6 in the figure is used to set the analog switch U22 to the off state by default during power on reset. The optional resistors R20 and R30 in the figure are used to prevent the output signals from being suspended when both the analog switch U22 and CH423 are turned off.

The resistance of each voltage division resistor in the figure shall be determined according to actual needs, for example, 4.7KΩ is selected for R29 (R39), 220Ω, 470Ω, 1KΩ, 2.2KΩ, 4.7KΩ, 10KΩ, 22KΩ and 47KΩ are selected for R21-R28 (R31-R38) respectively, the minimum voltage division output is 2.4% (when all OC pins are off), the maximum voltage division output is 100% (when all OC pins are off), and the adjusting range is about 40 times.

8.4. Anti-interference (Important)

As CH423 has high drive current, high glitch voltage will be generated on the power supply. Therefore, if the

PCB wiring of the power line or ground wire is not reasonable, it may affect the stability of MCU or CH423. Solutions to power interference:

① It is recommended to use shorter and thicker power line and ground wire, especially when CH423 and MCU are arranged on two PCBs;

② The power supply decoupling capacitor is connected in parallel close to the CH423 between the positive and negative power supplies, at least one 0.1uF capacitor and one electrolytic capacitor.

For external interference when the signal line is long, refer to the following figure for solution:

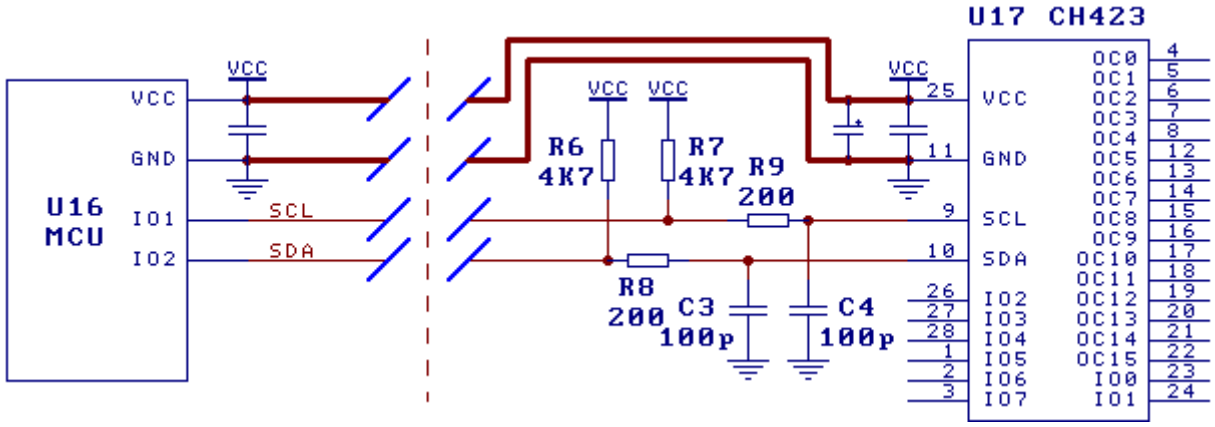
① At the pin end close to CH423 on the signal line, add the capacitors C3 and C4 with the capacitance of 47pF to 470pF. If the capacitance is higher, the transmission speed of the communication interface for MCU will be lower.

② Optionally add the resistors R8 and R9 with resistance of 100-470Ω;

③ Reduce the transmission speed between MCU and CH423 (because of added resistance and capacitance);

④ If it is driven by a quasi-bidirectional I/O pin (such as standard MCS51 MCU), it will be suggested to add resistors R6 and R7 with resistance of 500Ω to 10KΩ to strengthen the pull-up capacity of the quasi-bidirectional I/O pin for MCS-51 MCU, so as to keep good digital signal waveform during long distance transmission; pull-up resistors R6 and R7 are not required for short signal lines, and pull-up resistors R6 and R7 are not required for bidirectional I/O pins driven by totem pole.

In addition, for the application environment with strong interference, MCU can refresh CH423 every a few seconds, including reloading the output registers of the I/O pins and resetting system parameters.



8.5. Interface program of MCU

The website provides part of C programming language and ASM assembly interface program for MCU.