PIR sensor control chip

Outline

- SP010 is a CMOS chip designed to human infrared sensor control integrated circuits; it is a kind of high-performance sensor signal processing integrated circuit (IC) which together with PIR sensor and outward elements to constituent PIR switch. It can automatically and quickly open such devices as incandescent lamps, fluorescent lamps, buzzers, automatic valves, electric fans, dryers and automatic hand-washing facilities. IC is especially suitable for enterprises, hotels, shopping malls, warehouses, passages or corridors of houses, automatic lights, lighting systems and alarm systems.

- It can use PHOTO transistor or CDS application. The chip is equipped with amplifiers, comparator, timer, control circuits, system oscillator, and output timing oscillator. Its PIR sensor detects infrared power variation induced by the motion of a human body and transforms it to a voltage variation. If PIR output voltage variation conforms to the criteria, then the lamp is turned on with an adjustable duration.

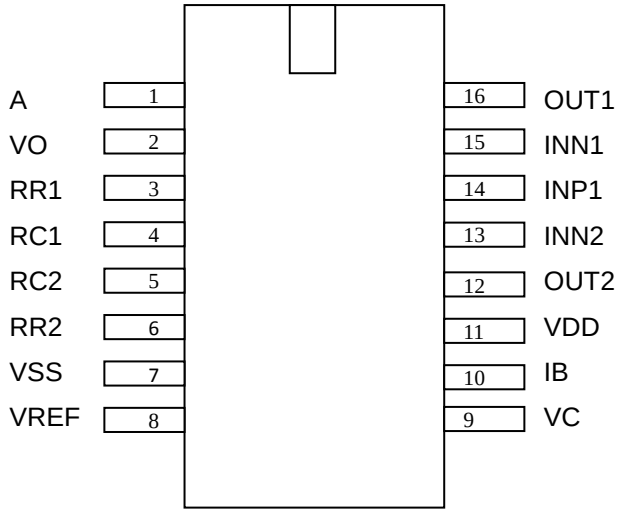
Characteristic

- Voltage operating range：1.8V ～ 6.0V
- Low power CMOS technology（ideal for battery operated PIR devices）
- It also compatible with SP010
- CMOS high input impedance operational amplifiers
- Bi-directional level detector / Excellent noise immunity
- Built-in Power up disable & output pulse control logic
- Dual mode : retriggerable & non-retriggerable
- Package for 16 SOP

Applications

- Human infrared sensor lights
- Automatic energy-efficient lighting occasions like garden, garage, hallway, stairs
- Monitoring, alarm, doorbell system like home, shops, offices, factories
- Automatic switching system like exhaust fans, ceiling fans

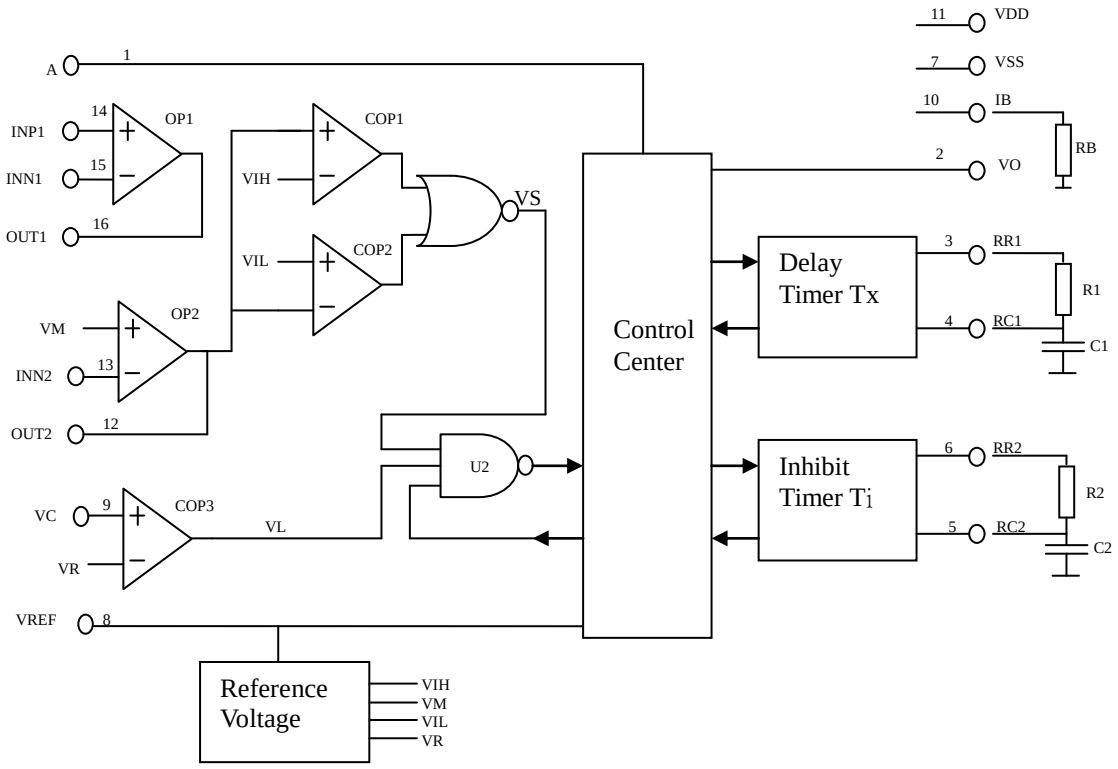
IC Pin diagram and description



SP010

Pin name	Pin Description
A	Retriggerable & non-retriggerable mode select (A = 0 : non- retriggerable , A = 1 : retriggerable)
VO	Detector output pin (active high)
RR1	Output pulse width control (Tx)
RC1	Output pulse width control (Tx)
RC2	Trigger inhibit control (Ti)
RR2	Trigger inhibit control (Ti)
VSS	Ground
VREF	RESET & voltage reference input
VC	Trigger disable input (VC > 0.2VDD = enable ; VC < 0.2VDD = disabled)
IB	Op-amp input bias current setting (RB connect to VSS , RB about = 1.5MΩ)
VDD	Supply voltage (1.8V ~ 6.0V)
OUT2	2nd stage Op-amp output
INN2	2nd stage Op-amp inverting input
INP1	1 st stage Op-amp non-inverting input
INN2	1 st stage Op-amp inverting input
OUT1	1 st stage Op-amp output

IC Internal functional diagram



Electrical Characteristics

- **Limiting values**

Parameter	Symbol	Condition	Rating	Unit
Operating Temperature	T_{OP}	—	-10～+70	℃
Storage Temperature	T_{STG}	—	-65～+150	℃
Supply Voltage	VIN	Ta=25°C	VSS-0.5～VSS+6.5	V
Input Voltage	V_I	Ta=25°C	VSS-0.5～VIN+6.0	V
Note：VSS symbolizes for system ground				

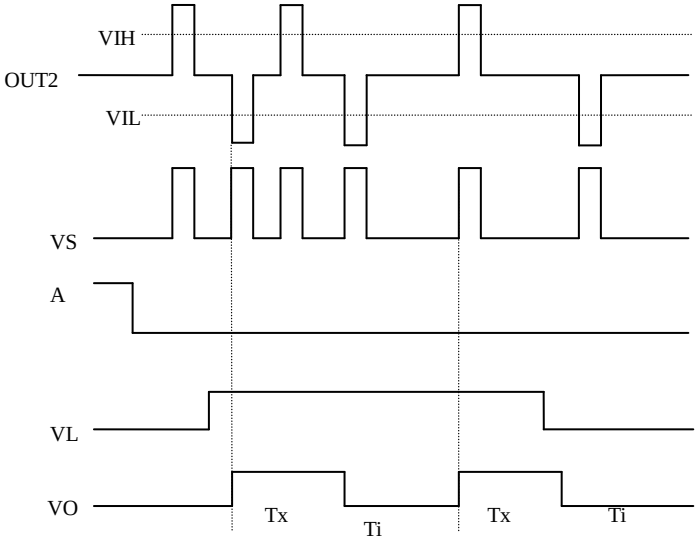
- **DC / AC characteristics：（Test condition at room temperature 25℃）**

Parameter	Symbol	Test Conditions		Values			Unit
				Min	Typ	Max	
Operating Voltage	VDD	—		1.8	-	6	V
Operating Current	IDD	Output no load	RB=1.5MΩ @VDD=3V	-	45	60	uA
			RB=2.0MΩ @VDD=3V	-	40	55	
			RB=1.5MΩ @VDD=5V	-	75	100	
			RB=2.0MΩ @VDD=5V	-	65	90	
Input voltage	VOS	VDD=5V		-		50	mV
Input current	IOS	VDD=5V		-		50	nA
Open loop gain	AVN	VDD=5V RL=1.5MΩ		60		-	dB
common-mode rejection ratio	CMRR	VDD=5V RL=1.5MΩ		60		-	dB
OP output Hi	VYH	VDD=5V RL=500KΩ & 1/2VDD		4.25		-	V
OP output Low	VYL			-		0.75	V
VC input Hi	VKH	VREF=VDD=5V		1.1		-	V
VC input Low	VRL			-		0.9	V
VO output Hi	VOH	VDD=5V IOH=0.5mA		4	4.8	-	V
VO output Low	VOL	VDD=5V IOL=0.1mA		-	0.1	0.4	V
A input Hi	VAH	VDD=5V		3.5		-	V
A input Low	VAL	VDD=5V		-		1.5	V

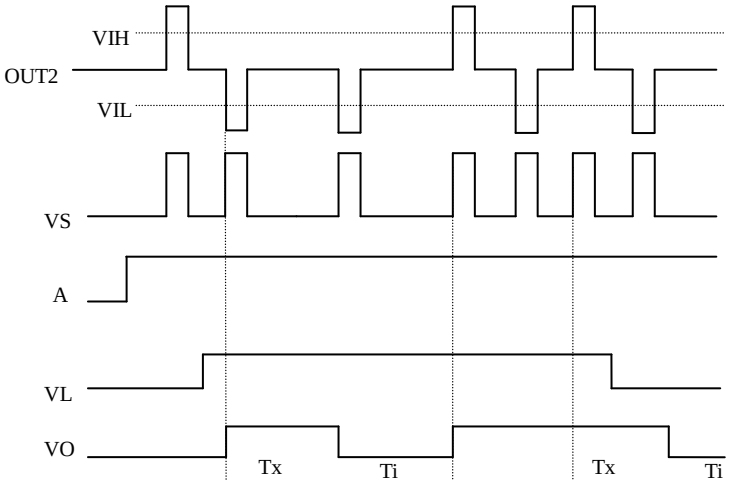
Note： Resistance RB reference basic application circuit

Function Description

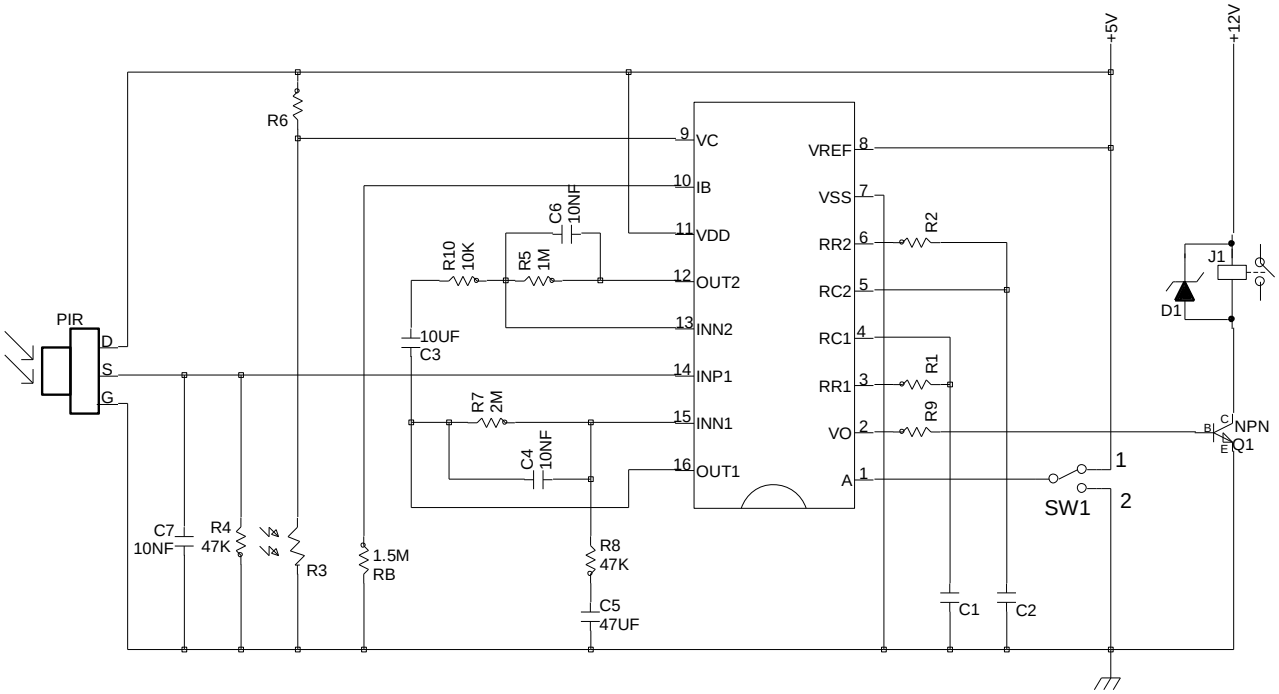
Non-retrigerrable waveform（A＝0）



Retrigerrable waveform（A＝1）



Basic Application Circuit



Tx The delay time and output resistors, capacitors follows：

（Test conditions are not considered stable PIR trigger time, the actual delay time due to steady time increases of PIR application circuit becomes longer）

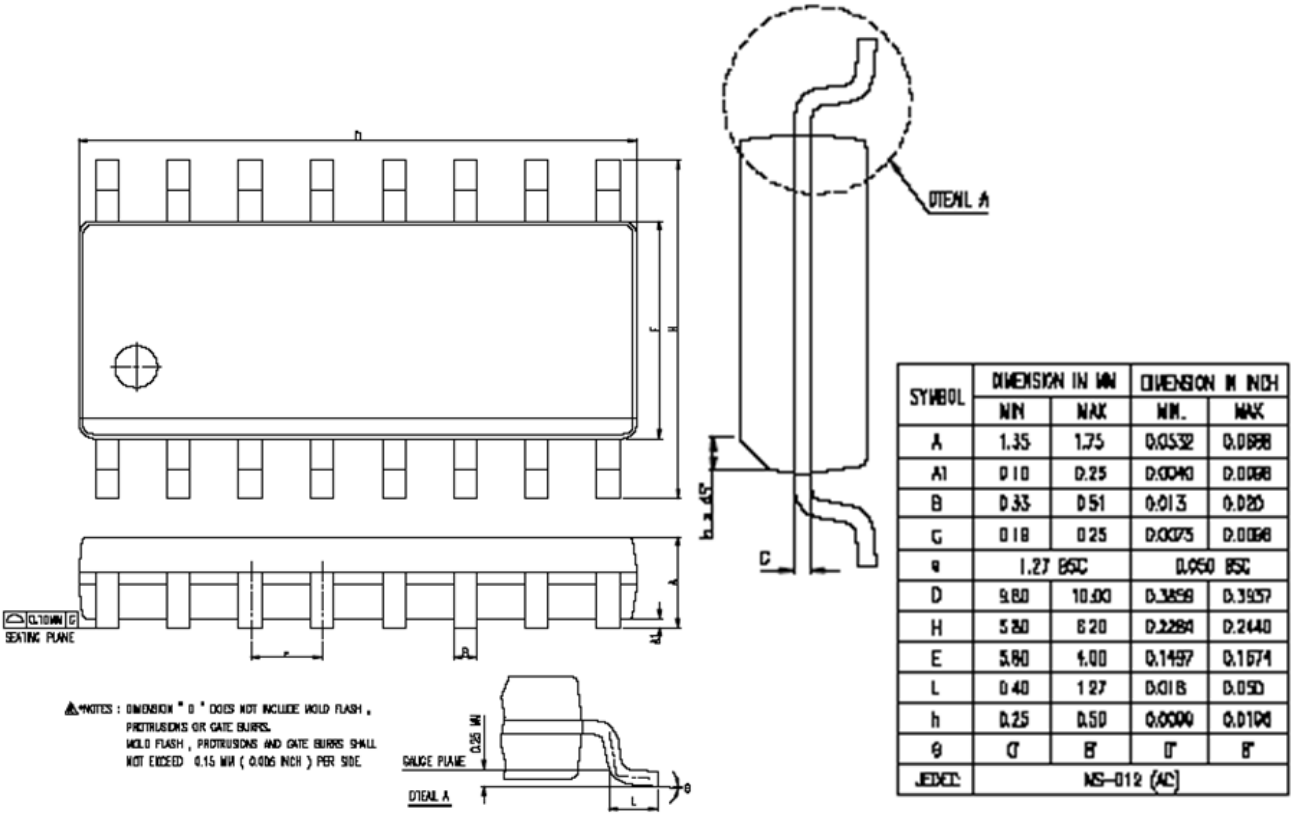
RR1RC1 — Delay time TX 。TX ≈ 49152R1C1。

RR2RC2 — Inhibit time 。TI ≈ 48R2C2。

RR1RC1 — delay time TX TX ≈ 49152R1C1				**RR2RC2** — inhibit tome TI TI ≈ 48R2C2			
C1	R1	VDD=5V Tx	VDD=3.3V Tx	C2	R2	VDD=5V TI	VDD=3.3V TI
0.01uF	22KΩ	7.1 sec	5.7 sec	0.1uF	300KΩ	1.1 sec	1.0 sec
0.01uF	47KΩ	15 sec	12 sec	0.1uF	430KΩ	1.6 sec	1.3 sec
0.01uF	100KΩ	31 sec	25 sec	0.1uF	620KΩ	2.3 sec	2.0 sec
0.01uF	200KΩ	62 sec	49 sec	0.1uF	1MΩ	3.7 sec	3.1 sec
0.01uF	330KΩ	102 sec	80 sec				
0.01uF	680KΩ	209 sec	164 sec				
0.01uF	1MΩ	308 sec	242 sec				

Descriptions of Packaging

- **SOP 16**



SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN	MAX	MIN.	MAX
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.18	0.25	0.0075	0.0098
e	1.27 BSC		0.050 BSC	
D	9.80	10.00	0.3859	0.3937
H	5.80	6.20	0.2284	0.2440
E	3.80	4.00	0.1497	0.1574
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.0099	0.0196
θ	0°	8°	0°	8°
JEDEC	MS-012 (AC)			

Ordering Information

SP010		
Package Type	**Chip Type**	**Wafer Type**
SP010	—	—