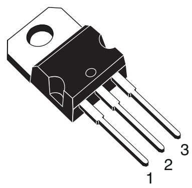
IRF820

N-channel 500V - 2.5Ω - 4A TO-220 PowerMesh™II MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
IRF820	500V	<0.3Ω	4A

- Extremely high dv/dt capability
- 100% avalnche tested
- New high voltage benchmark
- Gate charge minimized



TO-220

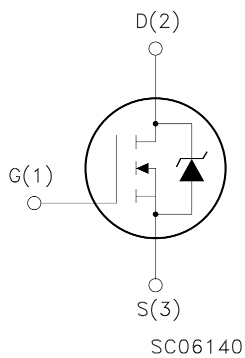
Description

The PowerMESH™II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns switching speed, gate charge and ruggedness.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
IRF820	IRF820	TO-220	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kW)	500	V
V_{GS}	Gate- source voltage	±30	V
I_D	Drain current (continuos) at t_c = 25°C	4	A
I_D	Drain current (continuos) at T_C = 100°C	2.5	A
I_{DM} (1)	Drain current (pulsed)	12	A
P_{TOT}	Total dissipation at T_C = 25°C	80	W
	Derating factor	0.64	W/°C
dv/dt (2)	Peak diode recovery voltage slope	3.5	V/ns
T_{stg}	Storage temperature	–65 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤2.5A, di/dt £50A/µs, V_{DD} ≤$V_{(BR)DSS}$, T_j £ T_{JMAX}.

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	1.56	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	°C/W
Rthc-sink	Thermal resistance case-sink typ	0.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	210	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 1.5 A		2.5	3	Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 2A		3		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		315 52 7.7		pF pF pF
$t_{d(on)}$ t_r $t_{r(Voff)}$ t_f	Turn-on delay time Rise time Off-voltage rise time Fall time	V_{DD} = 300 V, I_D = 2 A R_G = 4.7Ω V_{GS} = 10 V		10 13 15 13		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400V, I_D = 4 A, V_{GS} = 10V		12.5 2.7 6.1	17	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Table 6. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain Current Source-drain Current (pulsed)				4 16	A A
V_{SD}(2)	Forward On Voltage	I_{SD} = 4 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} =4 A, di/dt = 100A/µs V_{DD} = 100V, T_j = 150°C		400 1.64 8.2		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

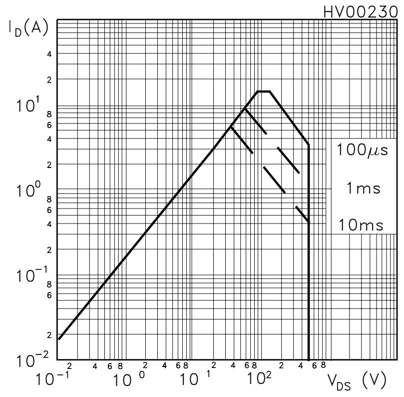


Figure 2. Thermal impedance

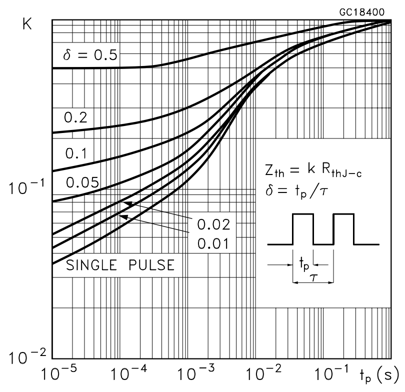


Figure 3. Output characterisics

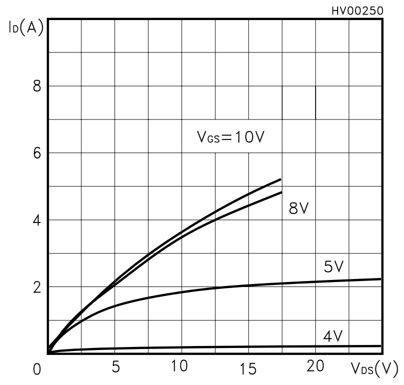


Figure 4. Transfer characteristics

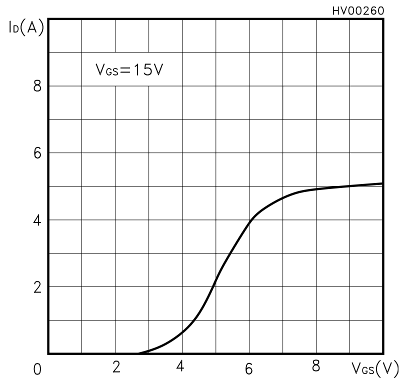


Figure 5. Transconductance

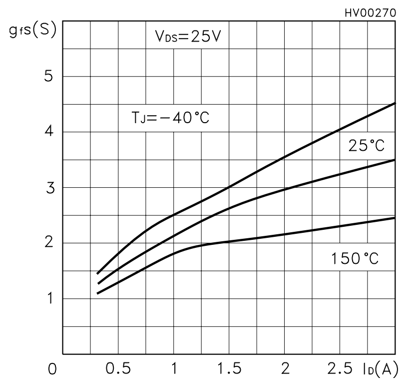


Figure 6. Static drain-source on resistance

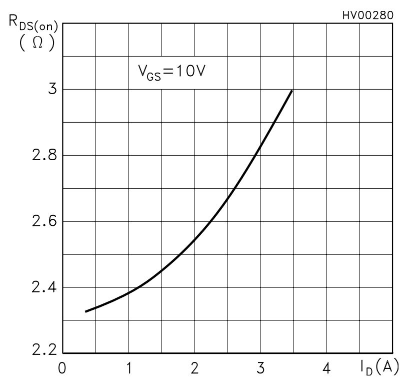


Figure 7. Gate charge vs gate-source voltage

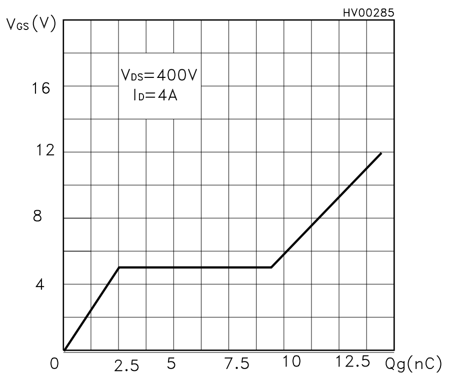


Figure 8. Capacitance variations

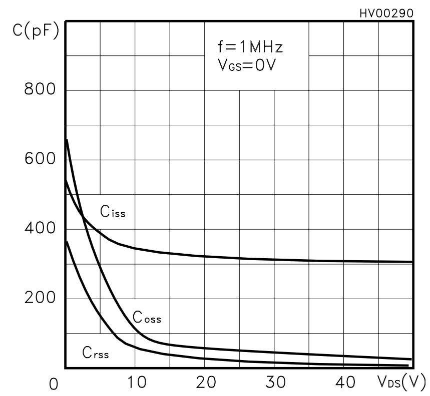


Figure 9. Normalized gate threshold voltage vs temperature

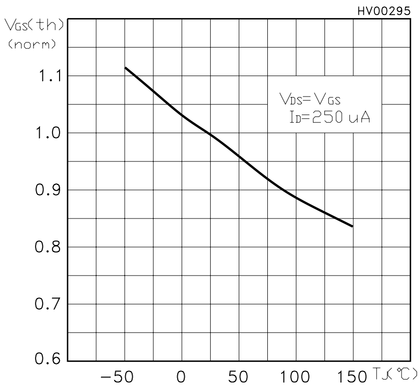


Figure 10. Normalized on resistance vs temperature

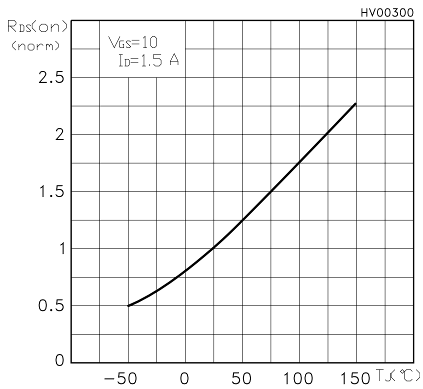
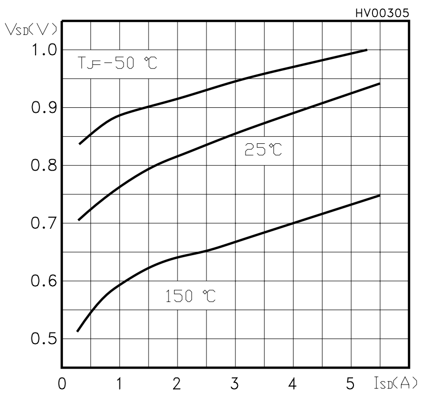


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Unclamped Inductive load test circuit

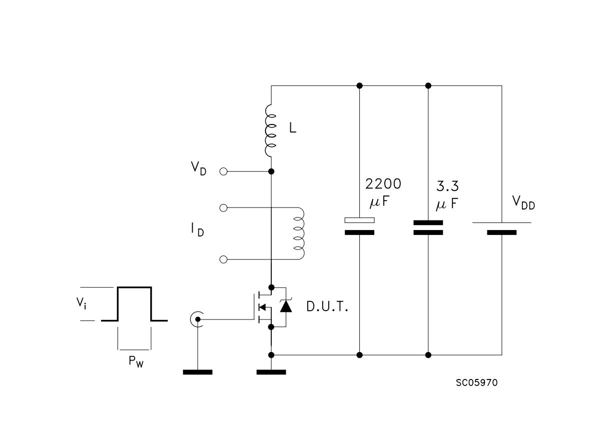


Figure 13. Unclamped inductive waveform

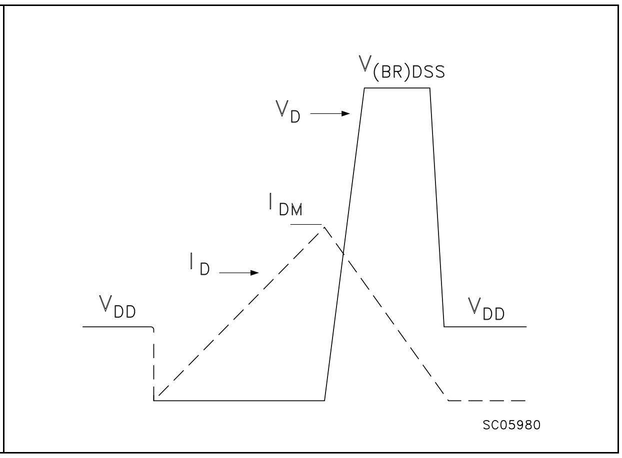


Figure 14. Switching times test circuit for resistive load

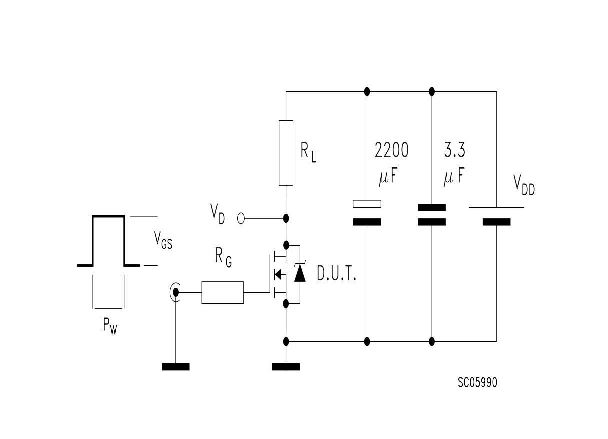


Figure 15. Gate charge test circuit

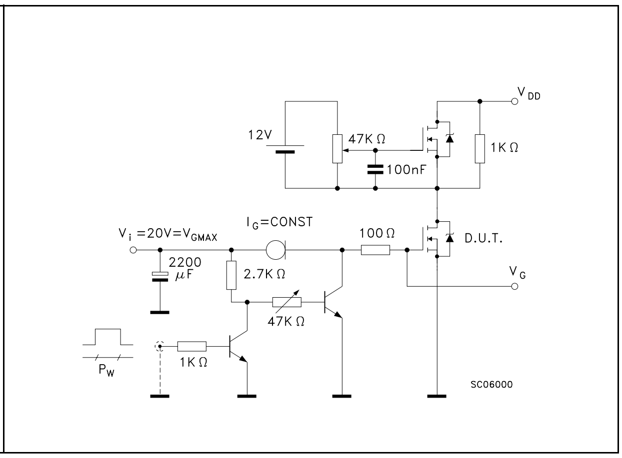
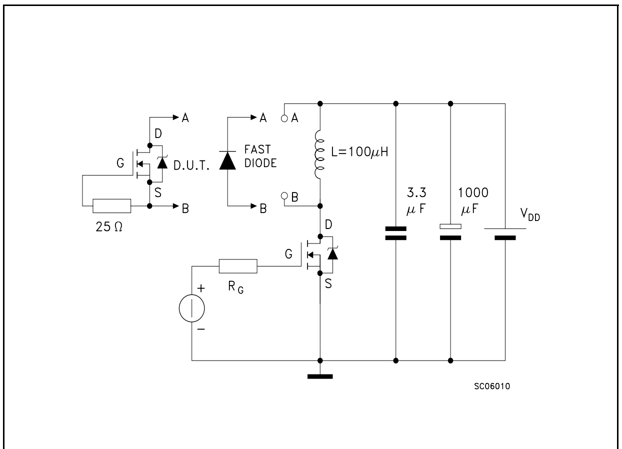


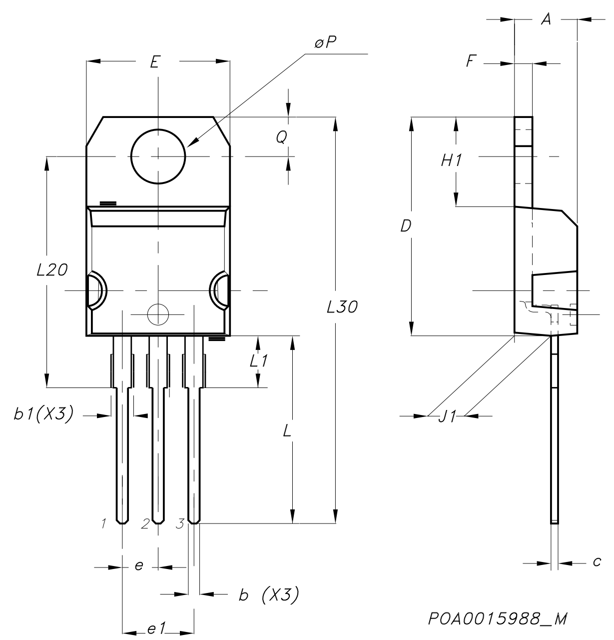
Figure 16. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	2	Preliminary version
27-Jun-2006	3	New template, no content change

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