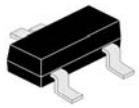
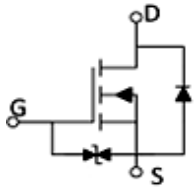
30V N-Channel Plastic-Encapsulate MOSFET

CDN1308EDL



SOT-323



SOT-323
Surface Mount
Plastic Package
RoHS compliant

Marking Code: KG

FEATURES:

1. Trench FET® power MOSFET
2. 100 % R_g tested
3. Typical ESD performance 1800V

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω) MAX.	I_D(A)[3]	Q_g (TYP.)
30	0.132 at V_{GS} = 10 V	1.5	1.4 nC
	0.144 at V_{GS} = 4.5 V	1.4	
	0.185 at V_{GS} = 2.5 V	1.3	

APPLICATION: Smart phones, tablet PC's, DC/DC converters, Boost converters, Load switch, OVP switch.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Drain-Source Voltage 30		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current (TJ=150 °C)	T_C = 25°C	I_D	1.4	A
	T_C = 70°C		1.1	A
	T_A = 25°C		1.5 [1,2]	A
	T_A = 70°C		1.2 [1,2]	A
Pulsed Drain Current (t = 300 µs)		I_{DM}	6	A
Continuous Source-Drain Diode Current	T_C = 25°C	I_S	0.4	A
	T_A = 25°C		0.3	A
Maximum Power Dissipation	T_C = 25°C	P_D	0.5	W
	T_C = 70°C		0.3	W
	T_A = 25°C		0.4 [1,2]	W
	T_A = 70°C		0.3 [1,2]	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature)			260	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYP	MAX	UNIT
Maximum Junction-to-Ambient [1,2]	t ≤ 10 s	R_{thJA}	250	300	°C
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	225	270	°C

NOTE:

1. Surface mounted on 1" x 1" FR4 board.
2. t = 10 s
3. Based on T_C = 25°C
4. Maximum under steady state conditions is 360 °C/W.

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ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

Off Characteristics

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	V_{DS}	V_{GS}=0V,I_D=250μA	30	--	--	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D=250μA	--	32	--	mV/ °C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS}(th)/T_J$		--	-3	--	
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.6	--	1.5	V
Gate-Source Leakage	I_{GSS}	V_{DS}=0V,V_{GS}=4.5V	--	--	1	μA
		V_{DS}=0V, V_{GS}=±12V	--	--	±20	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V	--	--	1	
		V_{DS}=30V,V_{GS}=0V,T_J=55°C	--	--	10	
On-State Drain Current [1]	$I_{D(on)}$	V_{DS} ≥ 5V,V_{GS}=10V	2	--	--	A
Drain-Source On-State Resistance [1]	$R_{DS(on)}$	V_{GS}=10V,I_D=1.4A	--	0.110	0.132	Ω
		V_{GS}=4.5V,I_D=1A	--	0.120	0.144	
		V_{GS}=2.5V,I_D=0.5A	--	0.142	0.185	
Forward Transconductance [1]	g_{fs}	V_{DS}=10V,I_D=1.4A	--	5	--	S

Dynamic Characteristics [2]

Input Capacitance	Ciss	V_{DS}=15V,V_{GS}=0V,f=1MHz	--	105	--	pF
Output Capacitance	Coss		--	23	--	
Reverse Transfer Capacitance	Crss		--	11	--	
Total Gate Charge	Q_g	V_{DS}=15V,V_{GS}=10V,I_D=1.4A	--	2.7	4.1	nC
		V_{DS}=15V,V_{GS}=4.5V,I_D=1.4A	--	1.4	2.1	
Gate-Source Charge	Q_{gs}		--	0.3	--	
Gate-Drain Charge	Q_{gd}		--	0.5	--	
Gate Resistance	R_g	f = 1 MHz	1.4	7	14	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=15V,R_L=13.6Ω,I_D1.1 A, V_{GEN}=10V,R_g=1Ω	--	2	4	ns
Rise Time	t_r		--	9	18	
Turn-Off Delay Time	$t_{d(off)}$		--	8	16	
Fall Time	t_f		--	8	16	
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=15V,R_L=13.6Ω,I_D≅1.1 A, V_{GEN}=4.5V,R_g=1Ω	--	8	16	
Rise Time	t_r		--	13	20	
Turn-Off Delay Time	$t_{d(off)}$		--	15	23	
Fall Time	t_f		--	6	12	

Drain-Source Diode Characteristics

Continuous Source-Drain Diode Current	I_S	T_C = 25°C	--	--	0.4	A
Pulse Diode Forward Current [1]	I_{SM}		--	--	6	
Body Diode Voltage	V_{SD}	I_F = 1.1A	--	0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F=1.1A, dI/dt=100A/μs, T_J = 25 °C	--	8	16	ns
Body Diode Reverse Recovery Charge	Q_{rr}		--	3	6	nC
Reverse Recovery Fall Time	t_a		--	5	--	ns
Reverse Recovery Rise Time	t_b		--	3	--	

Notes

1. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
2. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTICS CURVES

Fig 1: Gate Source Voltage vs. Gate Current

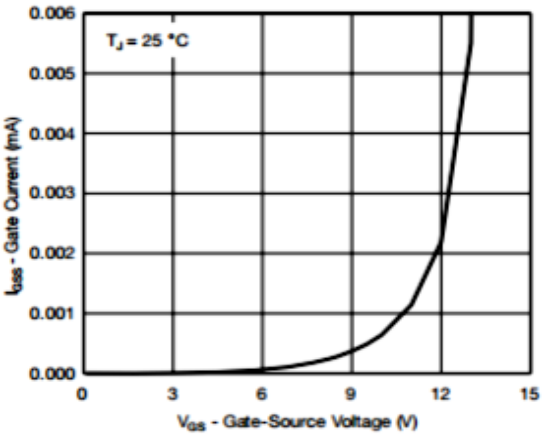


Fig 2: Gate Source Voltage vs. Gate Current

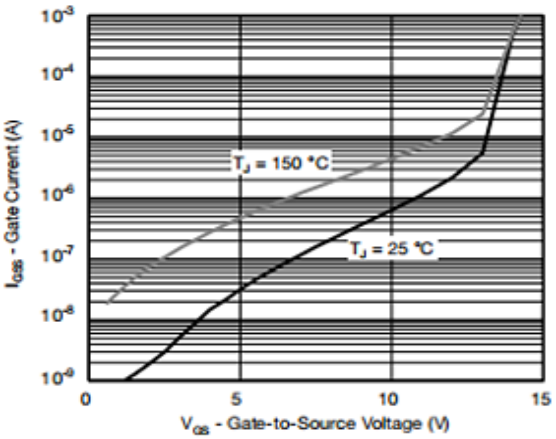


Fig 3: Output Characteristics

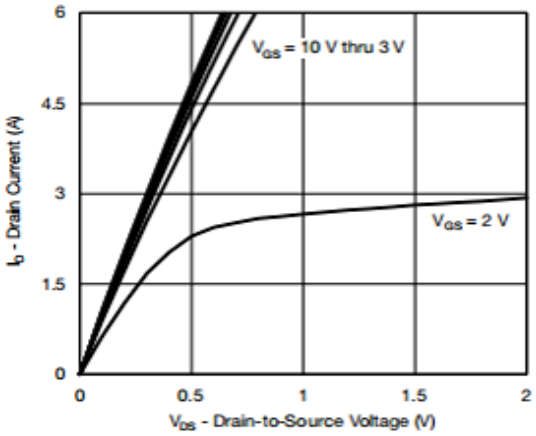


Fig 4: On-Resistance vs. Drain Current

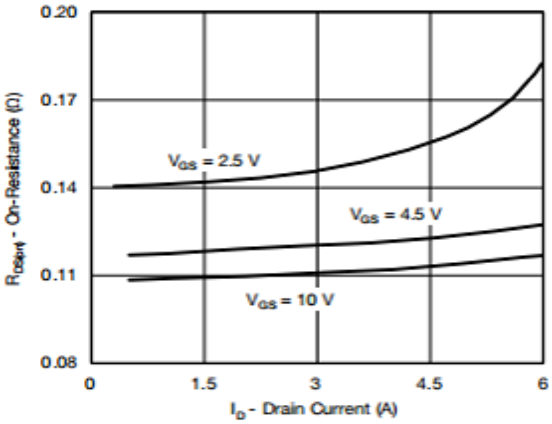


Fig 5: Transfer Characteristics

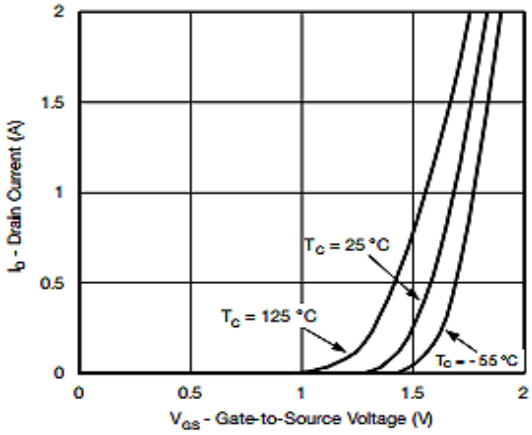
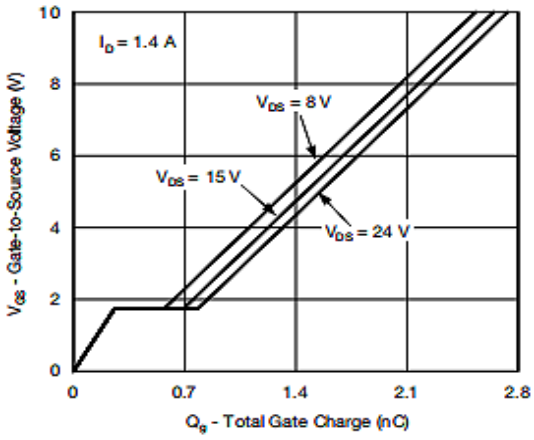


Fig 6: Gate Charge



TYPICAL CHARACTERISTICS CURVES

Fig 7: On-Resistance vs. Junction Temperature

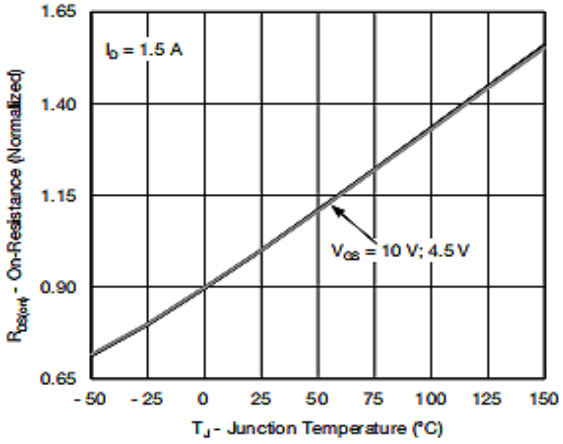


Fig 8: Source-Drain Diode Forward Voltage

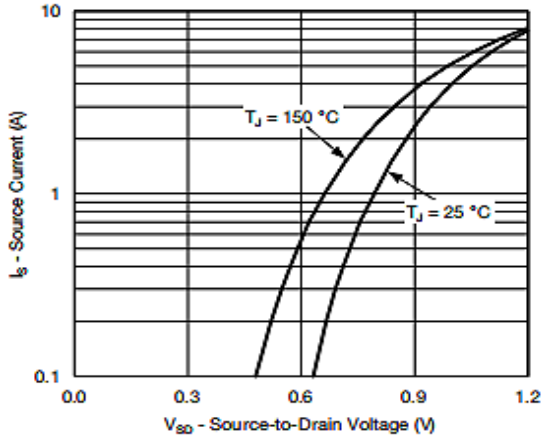


Fig 9: On-Resistance vs. Gate-to-Source Voltage

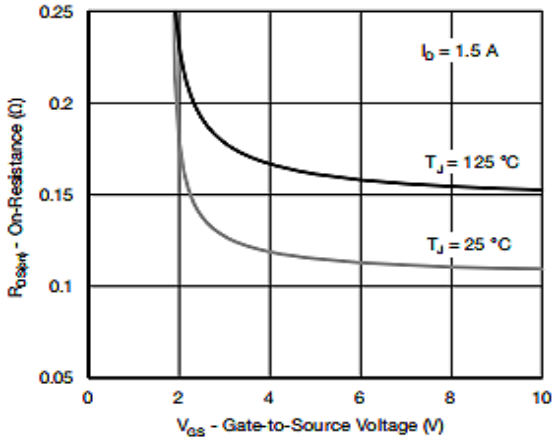


Fig 10: Threshold Voltage

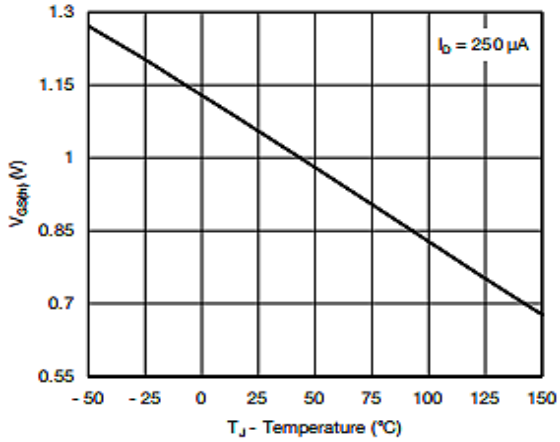


Fig 11: Single Pulse Power, Junction-to-Ambient

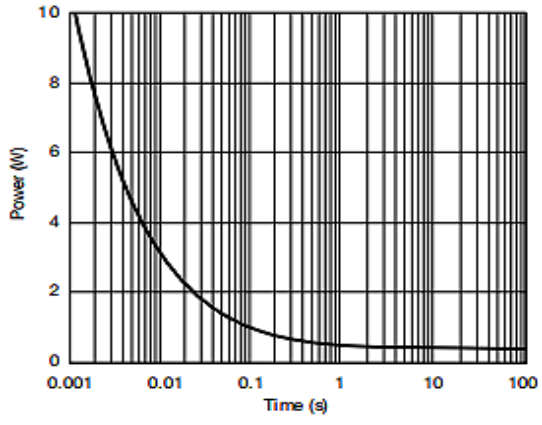
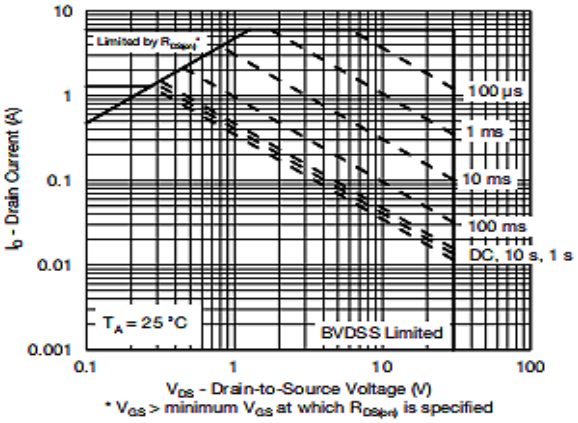


Fig 12: Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS CURVES

Fig 13: Power, Junction-to-Case

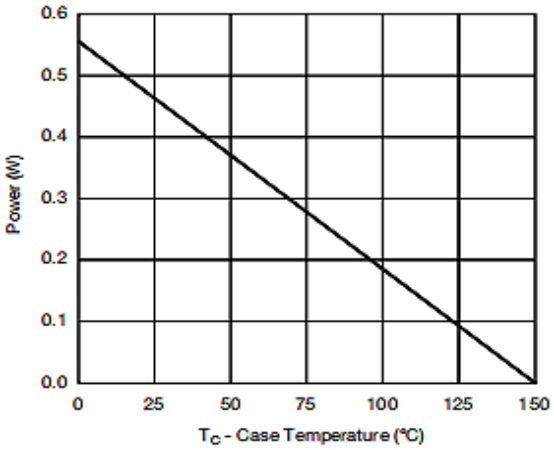


Fig 14: Power, Junction-to-Ambient

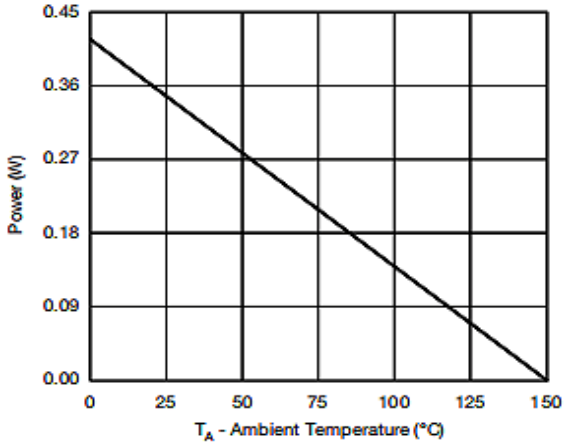
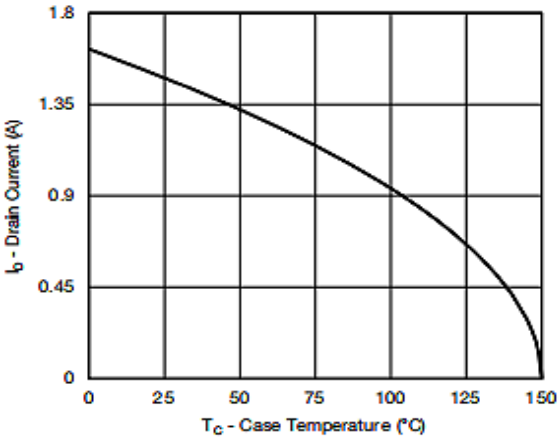


Fig 15: Current Derating [1]



1. The power dissipation P_D is based on $T_{J\,(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heat sink is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS CURVES

Fig 16: Normalized Thermal Transient Impedance, Junction-to-Ambient

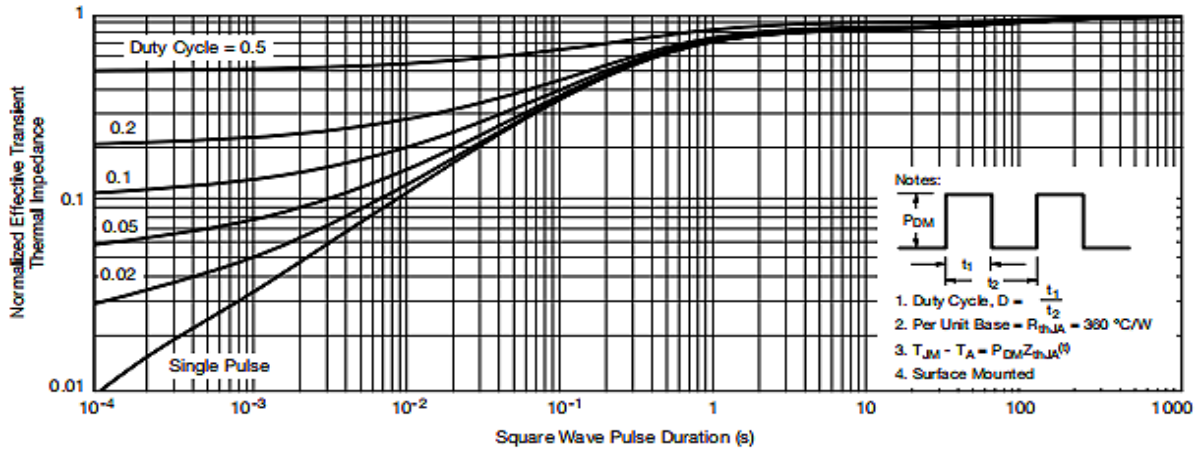
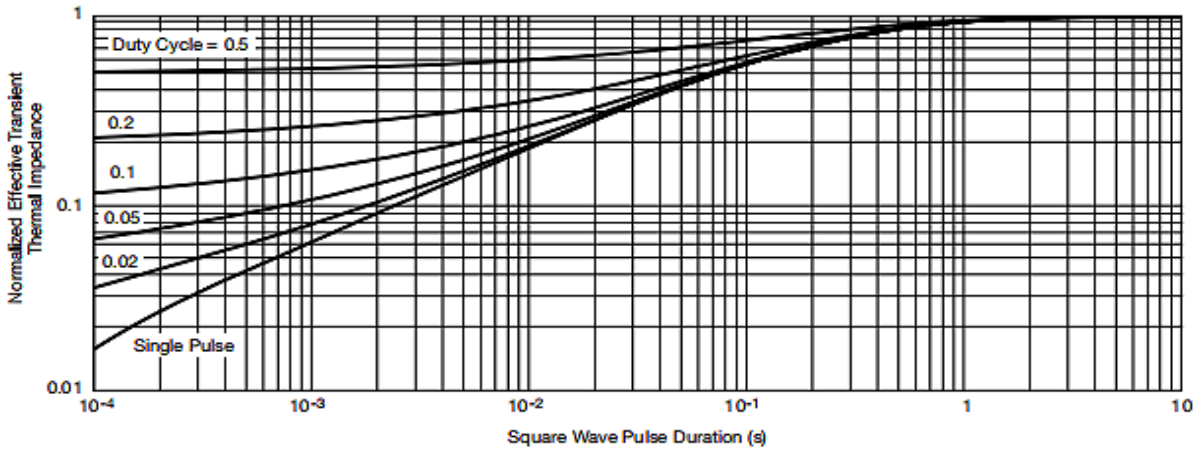
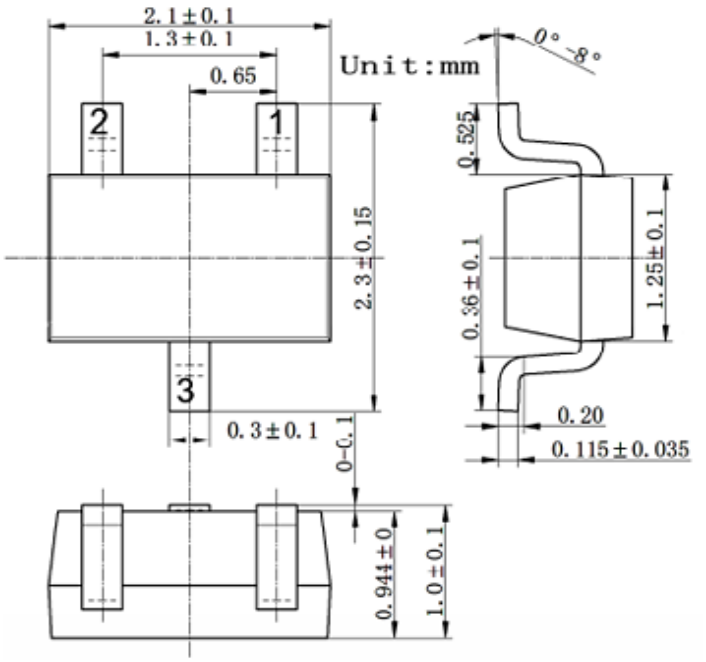


Fig 17: Normalized Thermal Transient Impedance, Junction-to-Foot



PACKAGE DETAIL \

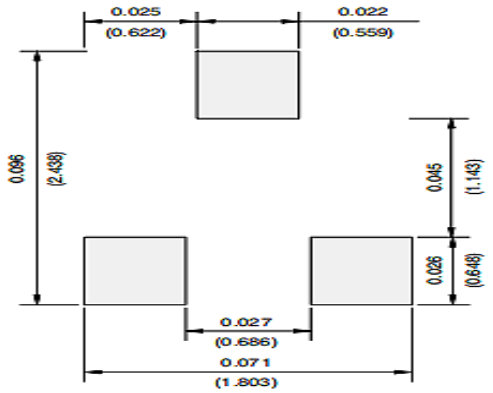
SOT-323 Package Outline Dimensions



Pin Configuration

1. Gate
2. Source
3. Drain

SOT-323 Suggested Pad Layout

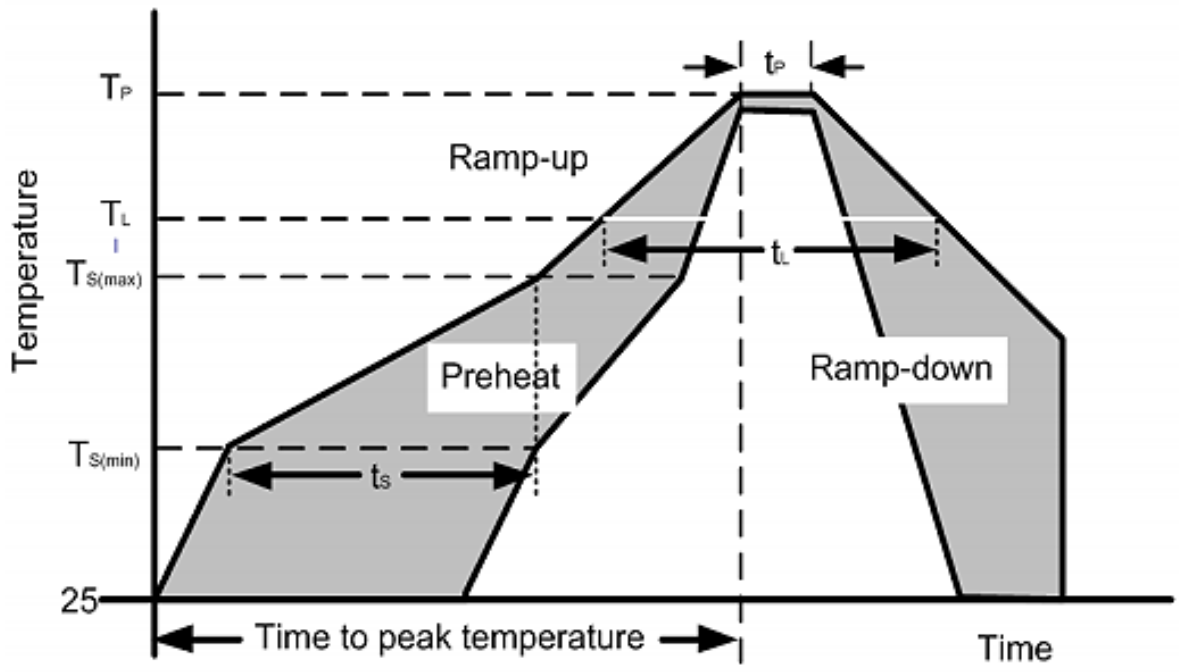


Dimensions in Inches/(mm)
Recommended Minimum Pads

Soldering Parameters

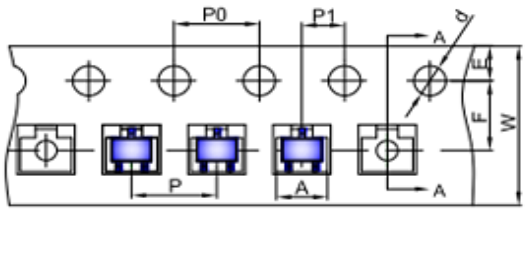
Reflow Condition		Pb--Free assembly
Pre Heat	Temperature Min ($T_{s(min)}$)	150°C
	Temperature Max ($T_{s(max)}$)	200°C
	Time (min to max) (ts)	60 – 190 secs
Average ramp up rate (Liquidus Temp) (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L——Ramp-up Rate		5°C/second max
Reflow	Temperature (TL) (Liquidus)	217°C
	Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		260+0/-5 °C
Time within actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		280°C

Temperature Profile



SOT-323 Tape and Reel Details

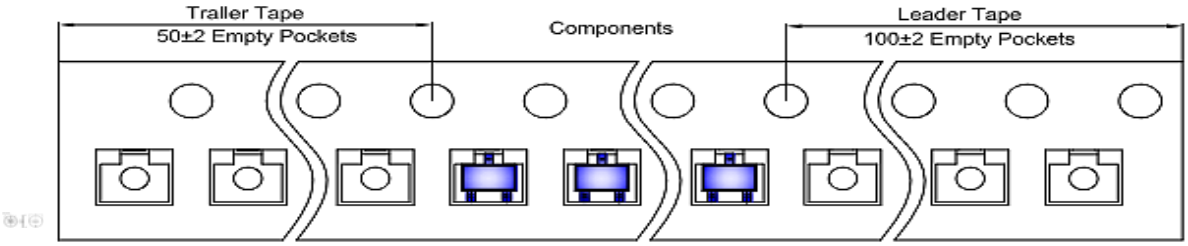
SOT-323 Embossed Carrier Tape



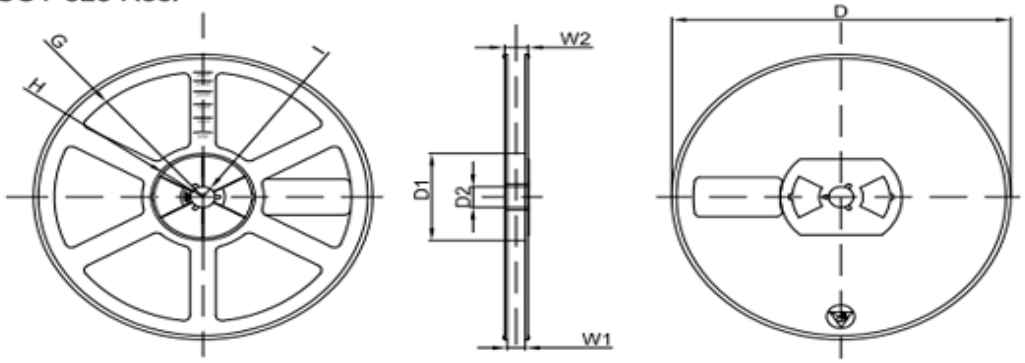
Packaging Description:
SOT-323 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 17.8cm diameter reel. The reels are clear in color and is made of polystyrene plastic (anti-static coated).

Dimensions are in millimeter										
Pkg type	A	B	C	d	E	F	P0	P	P1	W
SOT-323	2.25	2.55	1.19	Ø1.55	1.75	3.50	4.00	4.00	2.00	8.00

SOT-323 Tape Leader and Trailer



SOT-323 Reel



Dimensions are in millimeter								
Reel Option	D	D1	D2	G	H	I	W1	W2
7"Dia	Ø178.00	54.40	13.00	R78.00	R25.60	R6.50	9.50	12.30

REEL	Reel Size	Box	Box Size(mm)	Carton	Carton Size(mm)	G.W.(kg)
3000 pcs	7 Inch	45,000 pcs	203×203×195	180,000 pcs	438×438×220	

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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