TLC227x, TLC227xA: Advanced LinCMOS Rail-to-Rail Operational Amplifiers

1 Features

- Output Swing Includes Both Supply Rails
- Low Noise: 9 nV/√Hz Typical at f = 1 kHz
- Low-Input Bias Current: 1-pA Typical
- Fully-Specified for Both Single-Supply and Split-Supply Operation
- Common-Mode Input Voltage Range Includes Negative Rail
- High-Gain Bandwidth: 2.2-MHz Typical
- High Slew Rate: 3.6-V/µs Typical
- Low Input Offset Voltage: 950 µV Maximum at T_A = 25°C
- Macromodel Included
- Performance Upgrades for the TLC272 and TLC274
- Available in Q-Temp Automotive

2 Applications

- White Goods (Refrigerators, Washing Machines)
- Hand-held Monitoring Systems
- Configuration Control and Print Support
- Transducer Interfaces
- Battery-Powered Applications

3 Description

The TLC2272 and TLC2274 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC227x family offers 2 MHz of bandwidth and 3 V/µs of slew rate for higher-speed applications. These devices offer comparable AC performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC227x has a noise voltage of 9 nV/√Hz, two times lower than competitive solutions.

The TLC227x family of devices, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA family is available with a maximum input offset voltage of 950 µV. This family is fully characterized at 5 V and ±5 V.

The TLC227x also make great upgrades to the TLC27x in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices.

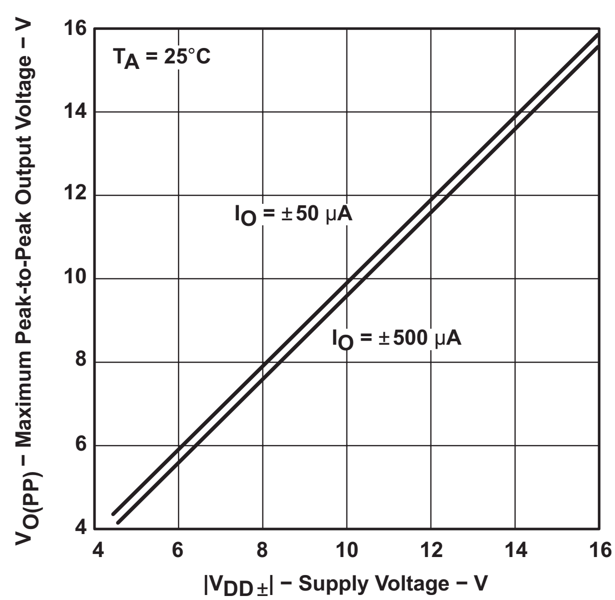
If the design requires single amplifiers, see the TLV2211, TLV2221 and TLV2231 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high density, battery-powered equipment.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC2272	TSSOP (8)	4.40 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
	SO (8)	5.30 mm × 6.20 mm
	PDIP (8)	6.35 mm × 9.81 mm
TLC2274	TSSOP (14)	4.40 mm × 5.00 mm
	SOIC (14)	3.91 mm × 8.65 mm
	SO (14)	5.30 mm × 10.30 mm
	PDIP (14)	6.35 mm × 19.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Maximum Peak-to-Peak Output Voltage vs Supply Voltage



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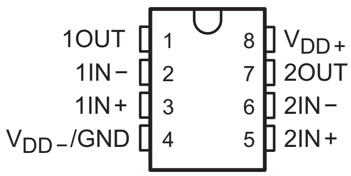
4 Revision History

Changes from Revision G (May 2004) to Revision H **Page**

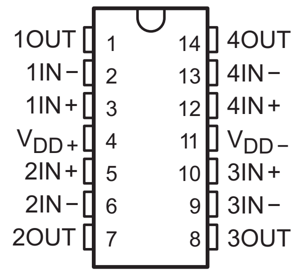
- Added *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support*section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Added ESD Rating table for the D and PW package devices. ... 5

5 Pin Configuration and Functions

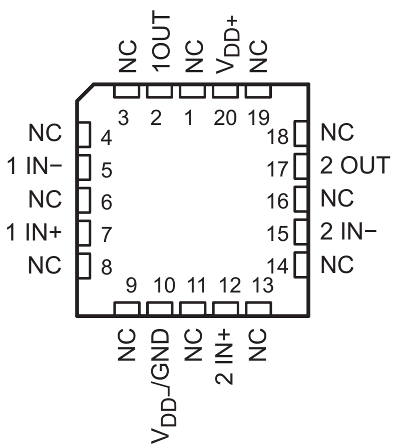
TLC2272
D, JG, P, or PW Package
8-Pin SOIC, CDIP, PDIP, or TSSOP
Top View



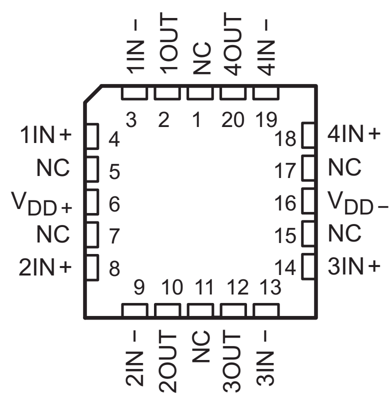
TLC2274
D, J, N, PW, or W Package
14-Pin SOIC, CDIP, PDIP, TSSOP, or CFP
Top View



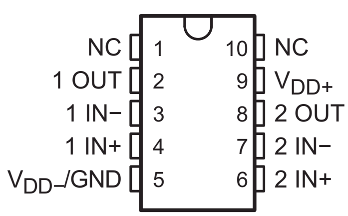
TLC2272
FK Package
20-Pin LCCC
Top View



TLC2274
FK Package
20-Pin LCCC
Top View



TLC2272
U Package
10-Pin CFP
Top View



Pin Functions

PIN						I/O	DESCRIPTION
NAME	NO.						
	TLC2272			TLC2274			
	D, JG, P, or PW	FK	U	D, J, N, PW, or W	FK		
1IN+	3	7	4	3	4	I	Non-inverting input, Channel 1
1IN-	2	5	3	2	3	I	Inverting input, Channel 1
1OUT	1	2	2	1	2	O	Output, Channel 1
2IN+	5	12	6	5	8	I	Non-inverting input, Channel 2
2IN-	6	15	7	6	9	I	Inverting input, Channel 2
2OUT	7	17	8	7	10	O	Output, Channel 2
3IN+	—	—	—	10	14	I	Non-inverting input, Channel 3
3IN-	—	—	—	9	13	I	Inverting input, Channel 3
3OUT	—	—	—	8	12	O	Output, Channel 3
4IN+	—	—	—	12	18	I	Non-inverting input, Channel 4
4IN-	—	—	—	13	19	I	Inverting input, Channel 4
4OUT	—	—	—	14	20	O	Output, Channel 4
V_{DD+}	8	20	9	4	6	—	Positive (highest) supply
V_{DD-}	—	—	—	11	16	—	Negative (lowest) supply
V_{DD-}/GND	4	10	5	—	—	—	Negative (lowest) supply
NC	—	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	1, 10	—	1, 5, 7, 11, 15, 17	—	No Connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{DD+} (2)			8	V
V_{DD-} (2)		–8		V
Differential input voltage, V_{ID} (3)			±16	V
Input voltage, V_I(any input) (2)		V_{DD-} − 0.3	V_{DD+}	V
Input current, I_I (any input)			±5	mA
Output current, I_O			±50	mA
Total current into V_{DD+}			±50	mA
Total current out of V_{DD-}			±50	mA
Duration of short-circuit current at (or below) 25°C (4)		Unlimited		
Operating free-air temperature range, T_A	C level parts	0	70	°C
	I, Q level parts	–40	125	
	M level parts	–55	125	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, P or PW package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or U package		300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD}.
(3) Differential voltages are at IN+ with respect to IN–. Excessive current will flow if input is brought below V_{DD-} − 0.3 V.
(4) The output may be shorted to either supply. Temperature or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	Q-grade and M-grade devices in D and PW packages	±2000	V
		Charged-device model (CDM), per AEC Q100-011	Q-grade and M-grade devices in D and PW packages	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{DD\pm}$	Supply voltage	C LEVEL PARTS	±2.2	±8	V
		I LEVEL PARTS	±2.2	±8	
		Q LEVEL PARTS	±2.2	±8	
		M LEVEL PARTS	±2.2	±8	
V_I	Input voltage	C LEVEL PARTS	V_{DD-}	V_{DD+} −1.5	V
		I LEVEL PARTS	V_{DD-}	V_{DD+} −1.5	
		Q LEVEL PARTS	V_{DD-}	V_{DD+} −1.5	
		M LEVEL PARTS	V_{DD-}	V_{DD+} −1.5	
V_{IC}	Common-mode input voltage	C LEVEL PARTS	V_{DD-}	V_{DD+} −1.5	V
		I LEVEL PARTS	V_{DD-}	V_{DD+} −1.5	
		Q LEVEL PARTS	V_{DD-}	V_{DD+} −1.5	
		M LEVEL PARTS	V_{DD-}	V_{DD+} −1.5	

Recommended Operating Conditions (continued)

			MIN	MAX	UNIT
T_A	Operating free-air temperature	C LEVEL PARTS	0	70	°C
		I LEVEL PARTS	–40	125	
		Q LEVEL PARTS	–40	125	
		M LEVEL PARTS	–55	125	

6.4 Thermal Information

THERMAL METRIC(1)		TLC2272					TLC2274					UNIT
		D (SOIC)	P (PDIP)	PW (TSSOP)	FK (LCCC)	U (CFP)	D (SOIC)	N (PDIP)	PW (TSSOP)	FK (LCCC)	J (CDIP)	
		8-PIN	8-PIN	8-PIN	20-PIN	10-PIN	14-PIN	14-PIN	14-PIN	20-PIN	14-PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)(3)	115.6	58.5	175.8	—	—	83.8	—	111.6	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (2)(3)	61.8	48.3	58.8	18	121.3	43.2	34	41.2	16	16.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.9	35.6	104.3	—	—	38.4	—	54.7	—	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.3	25.9	5.9	—	—	9.4	—	3.9	—	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.4	35.5	102.6	—	—	38.1	—	53.9	—	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	8.68	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

6.5 TLC2272 and TLC2272A Electrical Characteristics V_{DD} = 5 V

at specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	TLC2272	T_A = 25°C		300	2500	µV
			TLC2272A			300	950	
			TLC2272	Full Range(1)			3000	
			TLC2272A				1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				2		µV/°C
	Input offset voltage long-term drift(2)	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		0.5	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
I_{IB}	Input bias current	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		1	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; |V_{IO}| ≤ 5 mV		T_A = 25°C	–0.3	2.5	4	V
				Full Range(1)	0	2.5	3.5	

(1) T_A = –55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272 and TLC2272A Electrical Characteristics V_{DD} = 5 V (continued)

at specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −20 µA				4.99		V
		I_{OH} = −200 µA		T_A = 25°C	4.85	4.93		
				Full Range(1)	4.85			
		I_{OH} = −1 mA		T_A = 25°C	4.25	4.65		
				Full Range(1)	4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 50 µA			0.01		V
			I_{OL} = 500 µA	T_A = 25°C		0.09	0.15	
				Full Range(1)			0.15	
			I_{OL} = 5 mA	T_A = 25°C		0.9	1.5	
				Full Range(1)			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V; R_L = 10 kΩ(3)	C level part	T_A = 25°C	15	35		V/mV
				T_A = 0°C to 80°C	15			
			I level part	T_A = 25°C	15	35		
				T_A = –40°C to 85°C	15			
			Q level part	T_A = 25°C	10	35		
				T_A = –40°C to 125°C	10			
			M level part	T_A = 25°C	10	35		
				T_A = –55°C to 125°C	10			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V; R_L = 1 MΩ(3)				175		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		T_A = 25°C	70	75		dB
				Full Range(1)	70			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD} / 2, no load		T_A = 25°C	80	95		dB
				Full Range(1)	80			
I_{DD}	Supply currrent	V_O = 2.5 V, no load		T_A = 25°C		2.2	3	mA
				Full Range(1)			3	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ(3), C_L = 100 pF(3)		T_A = 25°C	2.3	3.6		V/µs
				Full Range(1)	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz				50		nV/√Hz
		f = 1 kHz				9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz				1		µV
		f = 0.1 Hz to 10 Hz				1.4		
I_n	Equivalent input noise current					0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ(3)		A_V = 1		0.0013%		
				A_V = 10		0.004%		
				A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ(3), C_L = 100 pF(3)				2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ(3), C_L = 100 pF(3)				1		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ(3), Step = 0.5 V to 2.5 V, C_L = 100 pF(3)		To 0.1%		1.5		µs
				To 0.01%		2.6		
φ_m	Phase margin at unity gain	R_L = 10 kΩ(3), C_L = 100 pF(3)				50°		
	Gain margin	R_L = 10 kΩ(3), C_L = 100 pF(3)				10		dB

(3) Referenced to 0 V.

6.6 TLC2272 and TLC2272A Electrical Characteristics $V_{DD\pm}$ = ±5 V

at specified free-air temperature, $V_{DD\pm}$ = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	TLC2272	T_A = 25°C		300	2500	µV
			TLC2272A			300	950	
			TLC2272	Full Range(1)			3000	
			TLC2272A				1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				2		µV/°C
	Input offset voltage long-term drift(2)	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		0.5	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
I_{IB}	Input bias current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		1	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; |V_{IO} | ≤ 5 mV		T_A = 25°C	–5.3	0	4	V
				Full Range(1)	–5	0	3.5	
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA				4.99		V
		I_O = −200 µA		T_A = 25°C	4.85	4.93		
				Full Range(1)	4.85			
		I_O = −1 mA		T_A = 25°C	4.25	4.65		
				Full Range(1)	4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V,	I_O = 50 µA			–4.99		V
			I_O = 500 µA	T_A = 25°C	–4.85	–4.91		
				Full Range(1)	–4.85			
			I_O = 5 mA	T_A = 25°C	–3.5	–4.1		
				Full Range(1)	–3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V; R_L = 10 kΩ	C level part	T_A = 25°C	25	50		V/mV
				T_A = 0°C to 80°C	25			
			I level part	T_A = 25°C	25	50		
				T_A = –40°C to 85°C	25			
			Q level part	T_A = 25°C	20	50		
				T_A = –40°C to 125°C	20			
			M level part	T_A = 25°C	20	50		
				T_A = –55°C to 125°C	20			
		V_O = ±4 V; R_L = 1 MΩ				300		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = –5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C	75	80		dB
				Full Range(1)	75			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD+} = 2.2 V to ±8 V, V_{IC} = 0 V, no load		T_A = 25°C	80	95		dB
				Full Range(1)	80			
I_{DD}	Supply currrent	V_O = 0 V, no load		T_A = 25°C		2.4	3	mA
				Full Range(1)			3	

(1) T_A = –55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272 and TLC2272A Electrical Characteristics $V_{DD\pm}$ = ±5 V (continued)

at specified free-air temperature, $V_{DD\pm}$ = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	T_A = 25°C	2.3	3.6		V/µs
			Full Range(1)	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz			50		nV/√Hz
		f = 1 kHz			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			1		µV
		f = 0.1 Hz to 10 Hz			1.4		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = ±2.3, f = 20 kHz, R_L = 10 kΩ	A_V = 1		0.0011%		
			A_V = 10		0.004%		
			A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ, C_L = 100 pF			0.54		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ, Step = –2.3 V to 2.3 V, C_L = 100 pF	To 0.1%		1.5		µs
			To 0.01%		3.2		
$φ_m$	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF			52°		
	Gain margin	R_L = 10 kΩ, C_L = 100 pF			10		dB

6.7 TLC2274 and TLC2274A Electrical Characteristics V_{DD} = 5 V

at specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	TLC2274	T_A = 25°C		300	2500	µV
			TLC2274A			300	950	
			TLC2274	Full Range(1)			3000	
			TLC2274A				1500	
$α_{VIO}$	Temperature coefficient of input offset voltage	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				2		µV/°C
	Input offset voltage long-term drift(2)	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		0.5	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
I_{IB}	Input bias current	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		1	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; |V_{IO}| ≤ 5 mV		T_A = 25°C	–0.3	2.5	4	V
				Full Range(1)	0	2.5	3.5	
V_{OH}	High-level output voltage	I_{OH} = −20 µA				4.99		V
		I_{OH} = −200 µA		T_A = 25°C	4.85	4.93		
				Full Range(1)	4.85			
		I_{OH} = −1 mA		T_A = 25°C	4.25	4.65		
				Full Range(1)	4.25			

(1) T_A = –55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274 and TLC2274A Electrical Characteristics V_{DD} = 5 V (continued)

at specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 50 µA			0.01		V
			I_{OL} = 500 µA	T_A = 25°C		0.09	0.15	
				Full Range(1)			0.15	
			I_{OL} = 5 mA	T_A = 25°C		0.9	1.5	
				Full Range(1)			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V; R_L = 10 kΩ(3)	C level part	T_A = 25°C	15	35		V/mV
				T_A = 0°C to 80°C	15			
			I level part	T_A = 25°C	15	35		
				T_A = –40°C to 85°C	15			
			Q level part	T_A = 25°C	10	35		
				T_A = –40°C to 125°C	10			
			M level part	T_A = 25°C	10	35		
				T_A = –55°C to 125°C	10			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V; R_L = 1 MΩ(3)				175		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		T_A = 25°C	70	75		dB
				Full Range(1)	70			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD} / 2, no load		T_A = 25°C	80	95		dB
				Full Range(1)	80			
I_{DD}	Supply currrent	V_O = 2.5 V, no load		T_A = 25°C		4.4	6	mA
				Full Range(1)			6	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ(3), C_L = 100 pF(3)		T_A = 25°C	2.3	3.6		V/µs
				Full Range(1)	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz				50		nV/√Hz
		f = 1 kHz				9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz				1		µV
		f = 0.1 Hz to 10 Hz				1.4		
I_n	Equivalent input noise current					0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ(3)		A_V = 1		0.0013%		
				A_V = 10		0.004%		
				A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ(3), C_L = 100 pF(3)				2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ(3), C_L = 100 pF(3)				1		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ(3), Step = 0.5 V to 2.5 V, C_L = 100 pF(3)		To 0.1%		1.5		µs
				To 0.01%		2.6		
φ_m	Phase margin at unity gain	R_L = 10 kΩ(3), C_L = 100 pF(3)				50°		
	Gain margin	R_L = 10 kΩ(3), C_L = 100 pF(3)				10		dB

(3) Referenced to 0 V.

6.8 TLC2274 and TLC2274A Electrical Characteristics $V_{DD\pm}$ = ±5 V

at specified free-air temperature, $V_{DD\pm}$ = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	TLC2274	T_A = 25°C		300	2500	µV
			TLC2274A			300	950	
			TLC2274	Full Range(1)			3000	
			TLC2274A				1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				2		µV/°C
	Input offset voltage long-term drift(2)	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		0.5	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
I_{IB}	Input bias current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	All level parts	T_A = 25°C		1	60	pA
			C level part	T_A = 0°C to 80°C			100	
			I level part	T_A = –40°C to 85°C			150	
			Q level part	T_A = –40°C to 125°C			800	
			M level part	T_A = –55°C to 125°C			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; |V_{IO} | ≤ 5 mV		T_A = 25°C	–5.3	0	4	V
				Full Range(1)	–5	0	3.5	
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA				4.99		V
		I_O = −200 µA		T_A = 25°C	4.85	4.93		
				Full Range(1)	4.85			
		I_O = −1 mA		T_A = 25°C	4.25	4.65		
				Full Range(1)	4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V	I_O = 50 µA			–4.99		V
			I_O = 500 µA	T_A = 25°C	–4.85	–4.91		
				Full Range(1)	–4.85			
			I_O = 5 mA	T_A = 25°C	–3.5	–4.1		
				Full Range(1)	–3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V; R_L = 10 kΩ	C level part	T_A = 25°C	25	50		V/mV
				T_A = 0°C to 80°C	25			
			I level part	T_A = 25°C	25	50		
				T_A = –40°C to 85°C	25			
			Q level part	T_A = 25°C	20	50		
				T_A = –40°C to 125°C	20			
			M level part	T_A = 25°C	20	50		
				T_A = –55°C to 125°C	20			
		V_O = ±4 V; R_L = 1 MΩ				300		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = –5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C	75	80		dB
				Full Range(1)	75			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD+} = 2.2 V to ±8 V, V_{IC} = 0 V, no load		T_A = 25°C	80	95		dB
				Full Range(1)	80			
I_{DD}	Supply currrent	V_O = 0 V, no load		T_A = 25°C		4.8	6	mA
				Full Range(1)			6	

(1) T_A = –55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274 and TLC2274A Electrical Characteristics $V_{DD\pm}$ = ±5 V (continued)

at specified free-air temperature, $V_{DD\pm}$ = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	T_A = 25°C	2.3	3.6		V/µs
			Full Range(1)	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz			50		nV/√Hz
		f = 1 kHz			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			1		µV
		f = 0.1 Hz to 10 Hz			1.4		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = ±2.3, f = 20 kHz, R_L = 10 kΩ	A_V = 1		0.0011%		
			A_V = 10		0.004%		
			A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ, C_L = 100 pF			0.54		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ, Step = –2.3 V to 2.3 V, C_L = 100 pF	To 0.1%		1.5		µs
			To 0.01%		3.2		
φ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF			52°		
	Gain margin	R_L = 10 kΩ, C_L = 100 pF			10		dB

6.9 Typical Characteristics

Table 1. Table of Graphs

			FIGURE[1]
V_{IO}	Input offset voltage	Distribution	1, 2, 3, 4
		vs Common-mode voltage	5, 6
α_{VIO}	Input offset voltage temperature coefficient	Distribution	7, 8, 9, 10[2]
I_{IB} / I_{IO}	Input bias and input offset current	vs Free-air temperature	11[2]
V_I	Input voltage	vs Supply voltage	12
		vs Free-air temperature	13[2]
V_{OH}	High-level output voltage	vs High-level output current	14[2]
V_{OL}	Low-level output voltage	vs Low-level output current	15, 16[2]
V_{OM+}	Maximum positive peak output voltage	vs Output current	17[2]
V_{OM-}	Maximum negative peak output voltage	vs Output current	18[2]
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	19
I_{OS}	Short-circuit output current	vs Supply voltage	20
		vs Free-air temperature	21[2]
V_O	Output voltage	vs Differential input voltage	22, 23
A_{VD}	Large-signal differential voltage amplification	vs Load resistance	24
	Large-signal differential voltage amplification and phase margin	vs Frequency	25, 26
	Large-signal differential voltage amplification	vs Free-air temperature	27[2], 28[2]
z_0	Output impedance	vs Frequency	29, 30
CMRR	Common-mode rejection ratio	vs Frequency	31
		vs Free-air temperature	32
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	33, 34
		vs Free-air temperature	35[2]
I_{DD}	Supply current	vs Supply voltage	36[2], 37[2]
		vs Free-air temperature	38[2], 39[2]
SR	Slew rate	vs Load Capacitance	40
		vs Free-air temperature	41[2]
V_O	Inverting large-signal pulse response		42, 43
	Voltage-follower large-signal pulse response		44, 45
	Inverting small-signal pulse response		46, 47
	Voltage-follower small-signal pulse response		48, 49
V_n	Equivalent input noise voltage	vs Frequency	50, 51
	Noise voltage over a 10-second period		52
	Integrated noise voltage	vs Frequency	53
THD+N	Total harmonic distortion + noise	vs Frequency	54
	Gain-bandwidth product	vs Supply voltage	55
		vs Free-air temperature	56[2]
φ_m	Phase margin	vs Load capacitance	57
	Gain margin	vs Load capacitance	58

(1) For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.
(2) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

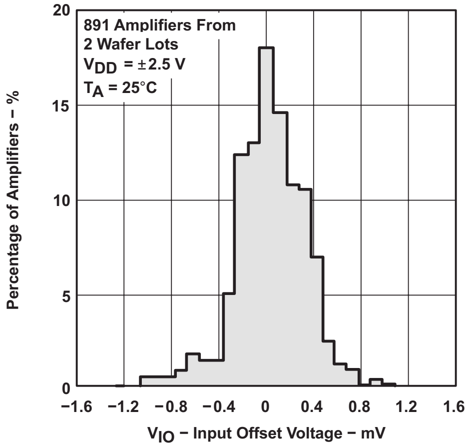


Figure 1. Distribution of TLC2272 Input Offset Voltage

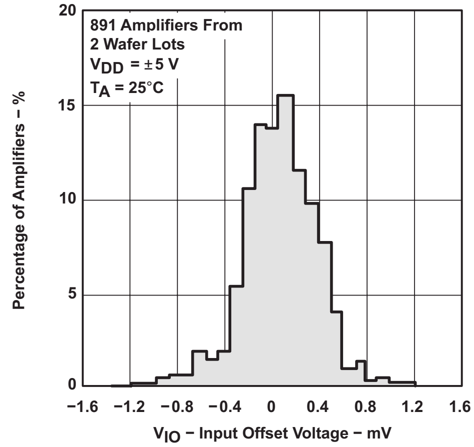


Figure 2. Distribution of TLC2272 Input Offset Voltage

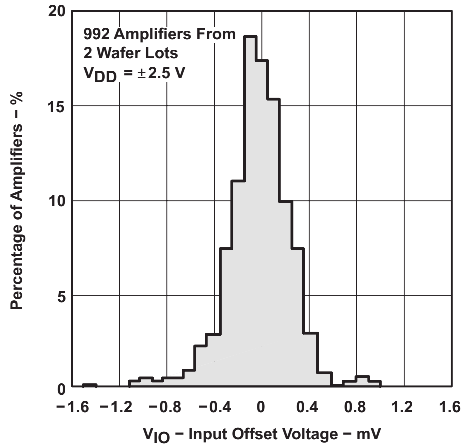


Figure 3. Distribution of TLC2274 Input Offset Voltage

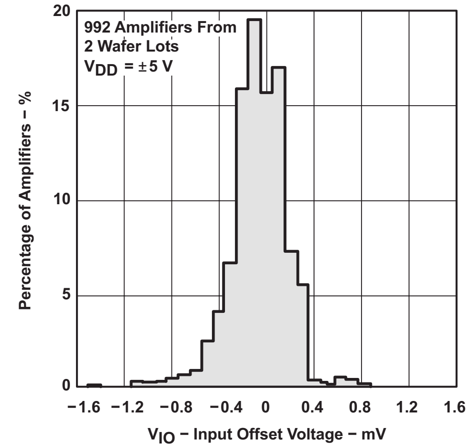


Figure 4. Distribution of TLC2274 Input Offset Voltage

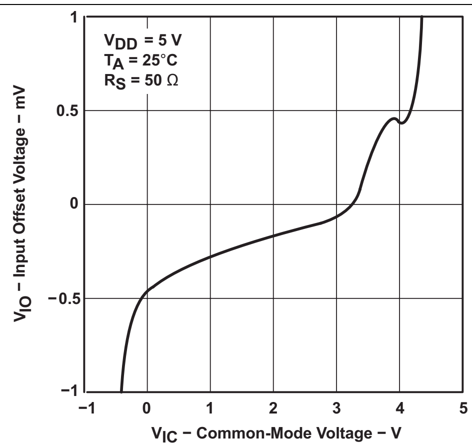


Figure 5. Input Offset Voltage vs Common-Mode Voltage

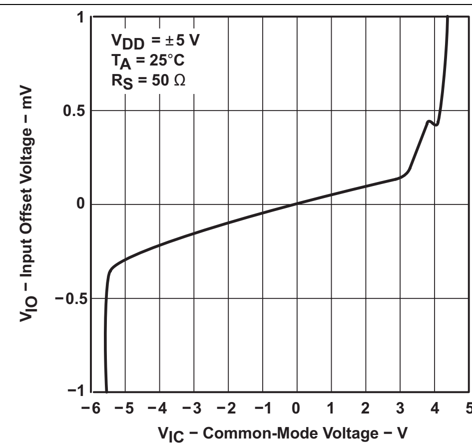


Figure 6. Input Offset Voltage vs Common-Mode Voltage

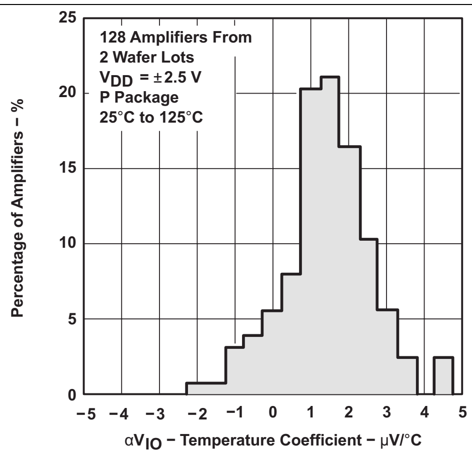


Figure 7. Distribution of TLC2272 vs Input Offset Voltage Temperature Coefficient

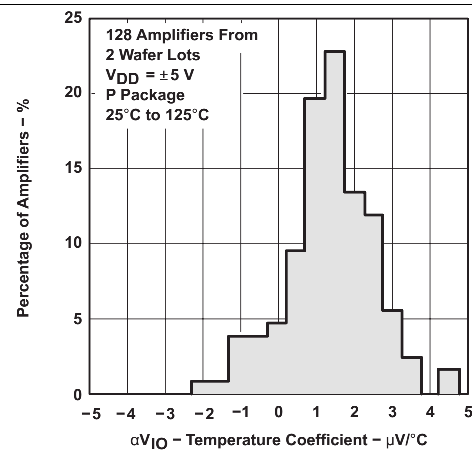


Figure 8. Distribution of TLC2272 vs Input Offset Voltage Temperature Coefficient

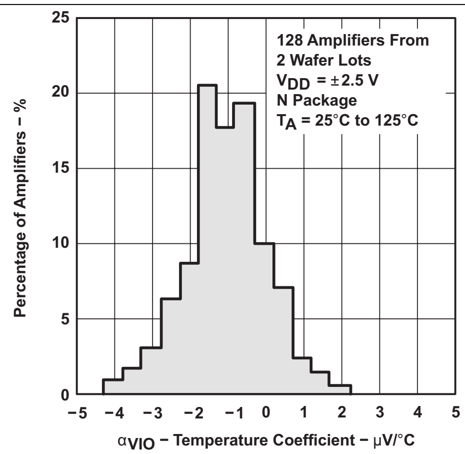


Figure 9. Distribution of TLC2274 vs Input Offset Voltage Temperature Coefficient

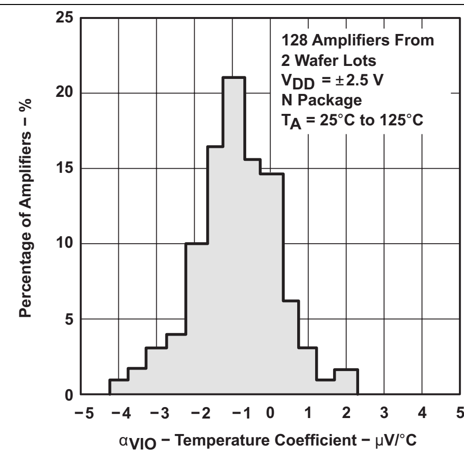


Figure 10. Distribution of TLC2274 vs Input Offset Voltage Temperature Coefficient

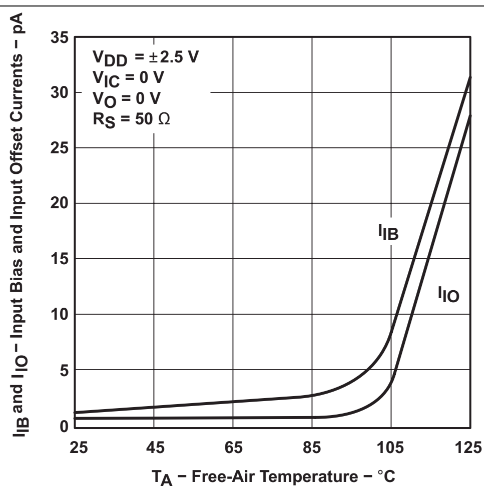


Figure 11. Input Bias and Input Offset Current vs Free-Air Temperature

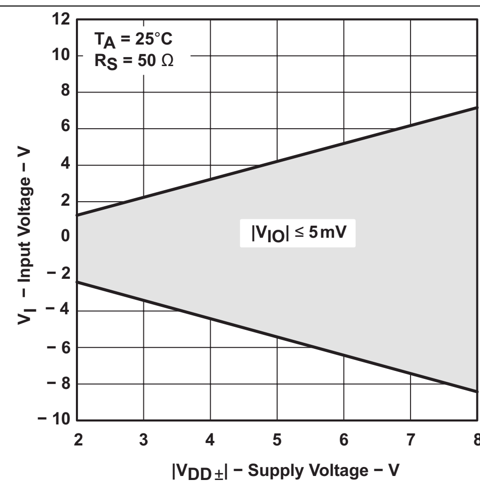


Figure 12. Input Voltage vs Supply Voltage

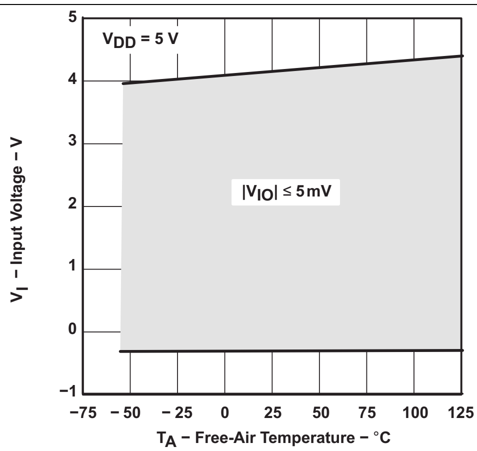


Figure 13. Input Voltage vs Free-Air Temperature

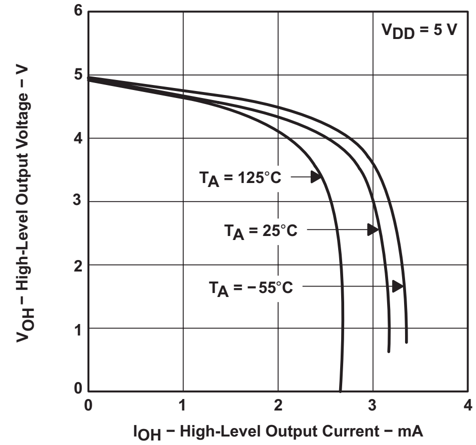


Figure 14. High-Level Output Voltage vs High-Level Output Current

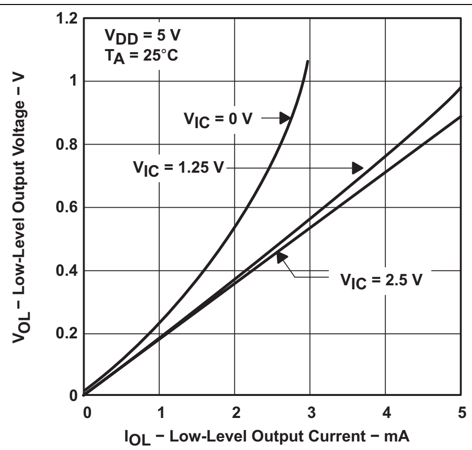


Figure 15. Low-Level Output Voltage vs Low-Level Output Current

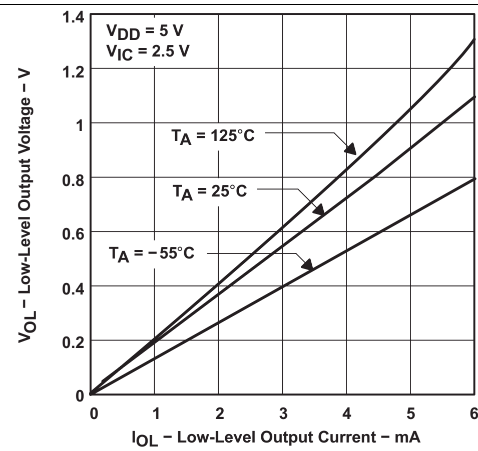


Figure 16. Low-Level Output Voltage vs Low-Level Output Current

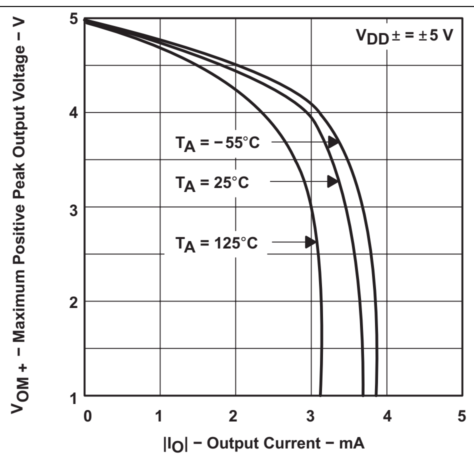


Figure 17. Maximum Positive Peak Output Voltage vs Output Current

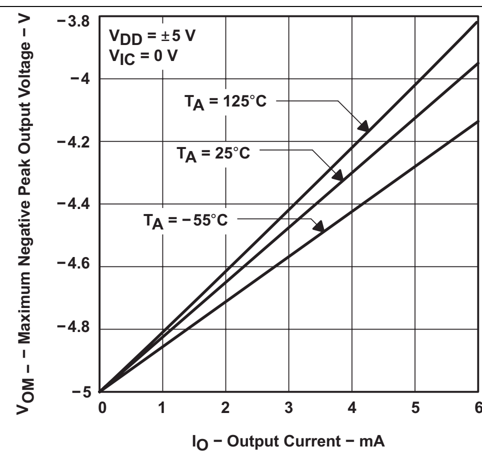


Figure 18. Maximum Positive Peak Output Voltage vs Output Current

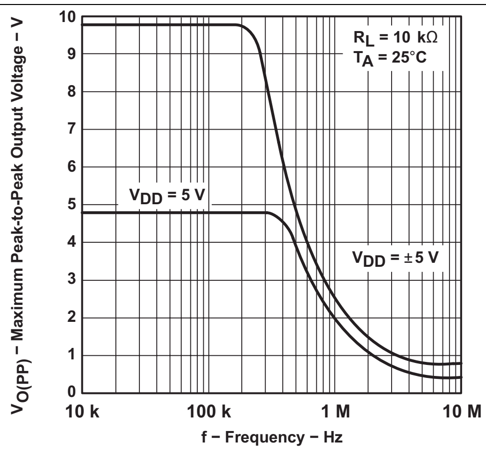


Figure 19. Maximum Peak-to-Peak Output Voltage vs Frequency

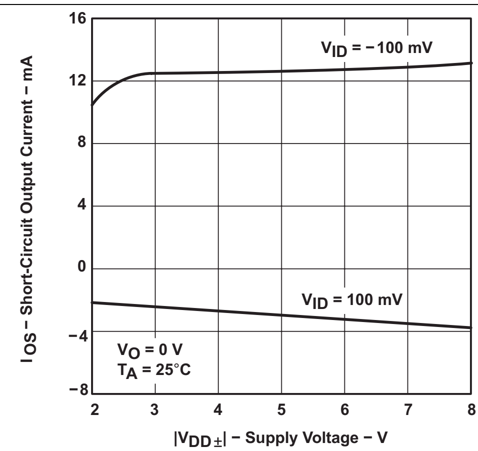


Figure 20. Short-Circuit Output Current vs Supply Voltage

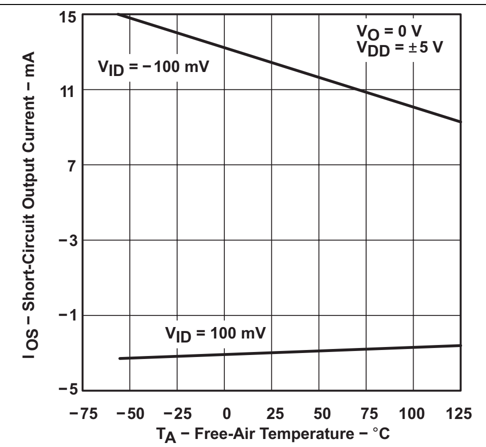


Figure 21. Short-Circuit Output Current vs Free-Air Temperature

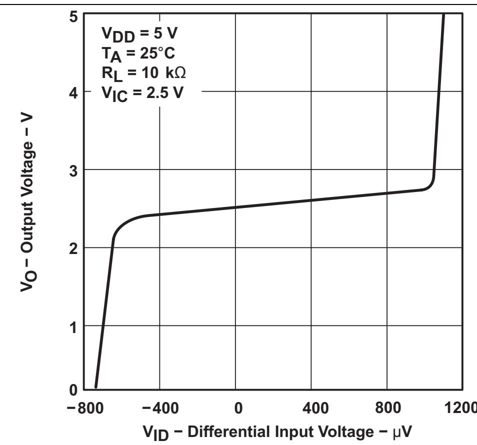


Figure 22. Output Voltage vs Differential Input Voltage

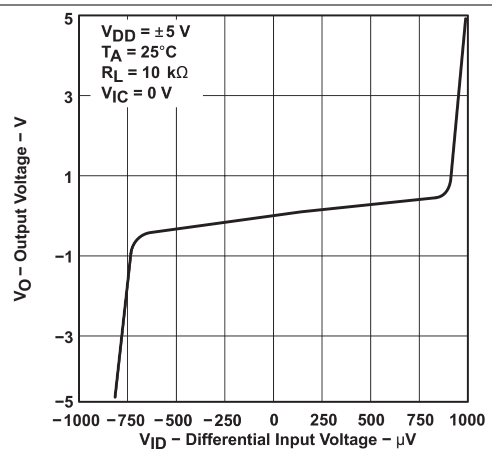


Figure 23. Output Voltage vs Differential Input Voltage

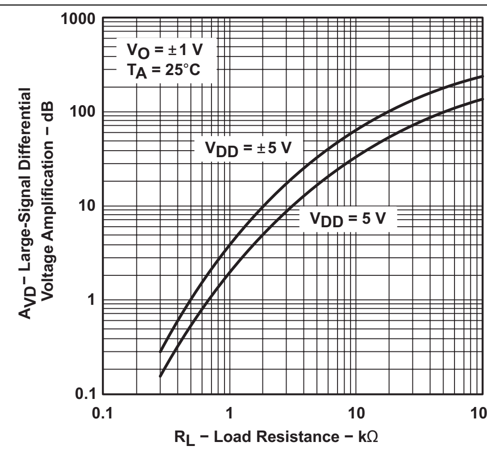


Figure 24. Large-Signal Differential Voltage Amplification vs Load Resistance

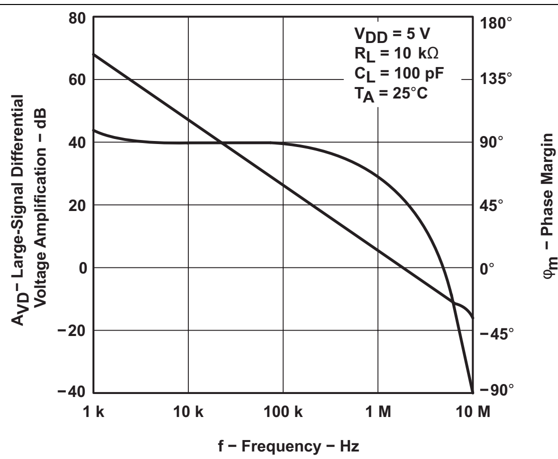


Figure 25. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

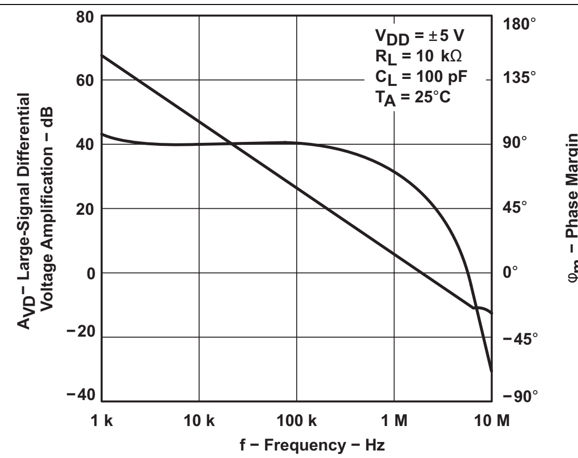


Figure 26. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

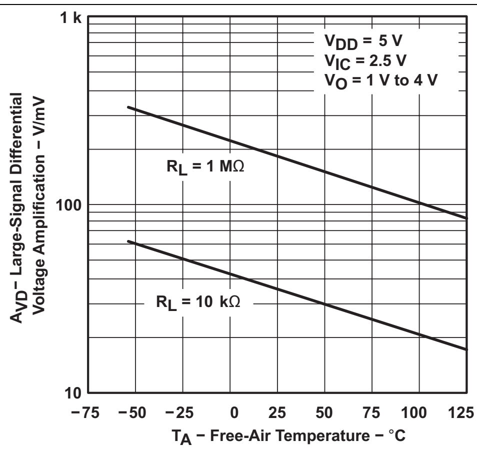


Figure 27. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

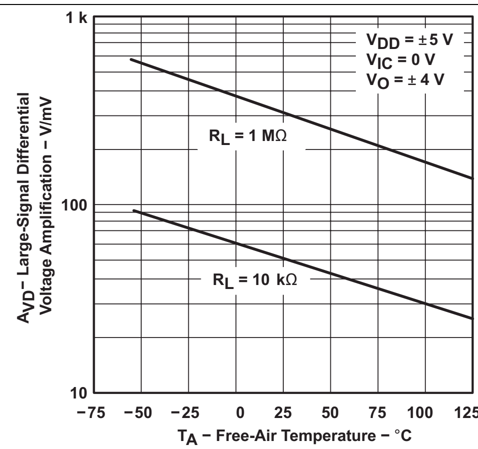


Figure 28. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

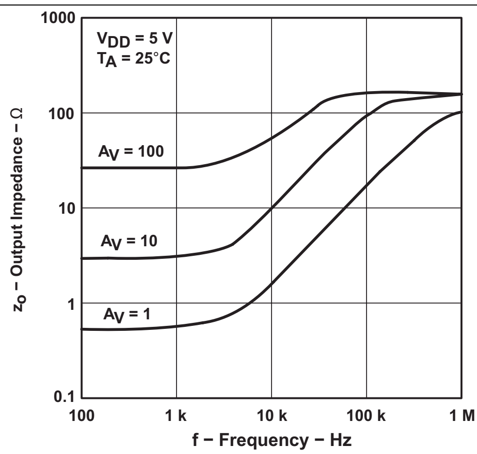


Figure 29. Output Impedance vs Frequency

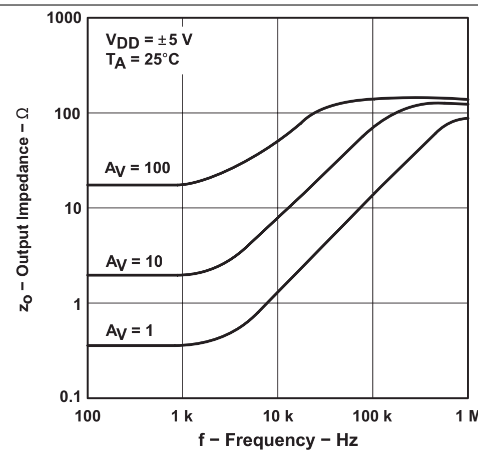


Figure 30. Output Impedance vs Frequency

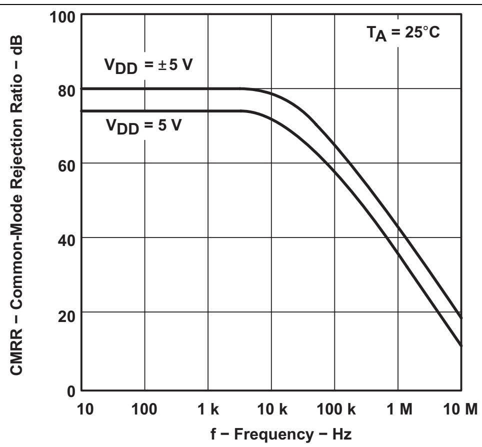


Figure 31. Common-Mode Rejection Ratio vs Frequency

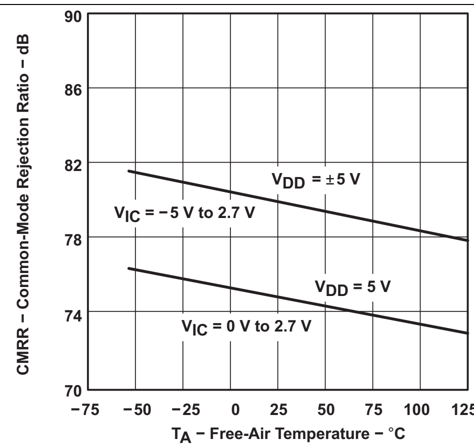


Figure 32. Common-Mode Rejection Ratio vs Free-Air Temperature

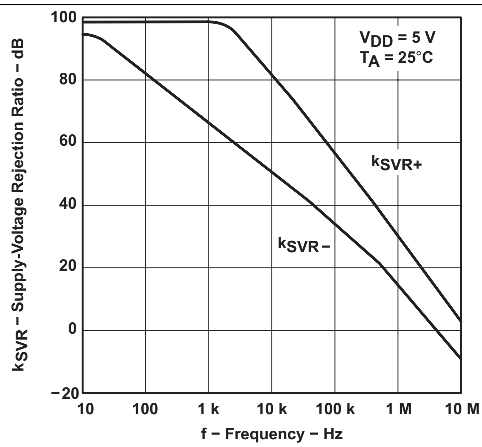


Figure 33. Supply-Voltage Rejection Ratio vs Frequency

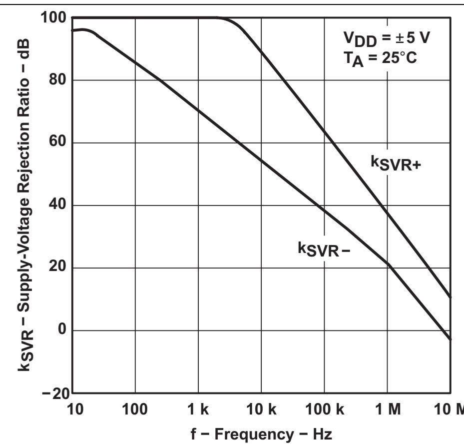


Figure 34. Supply-Voltage Rejection Ratio vs Frequency

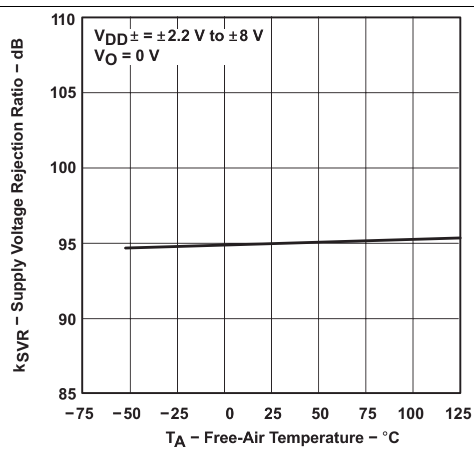


Figure 35. Supply-Voltage Rejection Ratio vs Free-Air Temperature

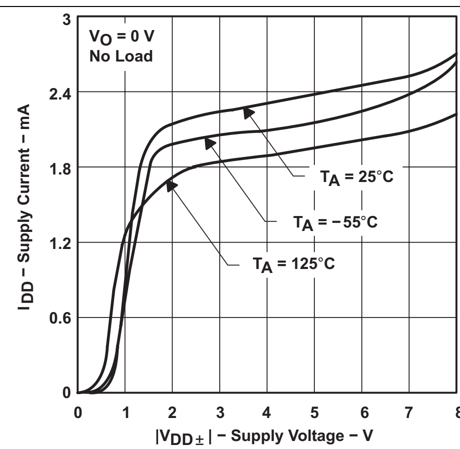


Figure 36. TLC2272 Supply Current vs Supply Voltage

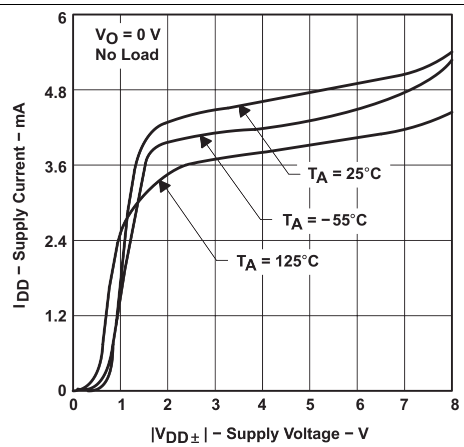


Figure 37. TLC2274 Supply Current vs Supply Voltage

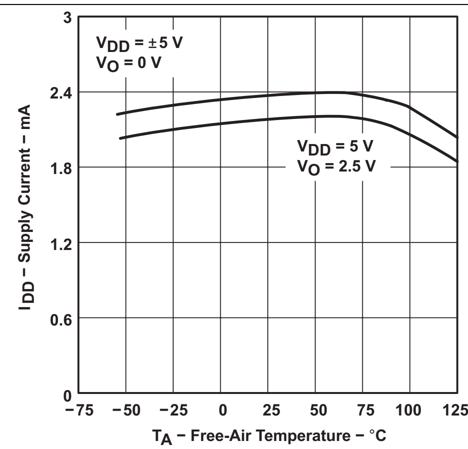


Figure 38. TLC2272 Supply Current vs Free-Air Temperature

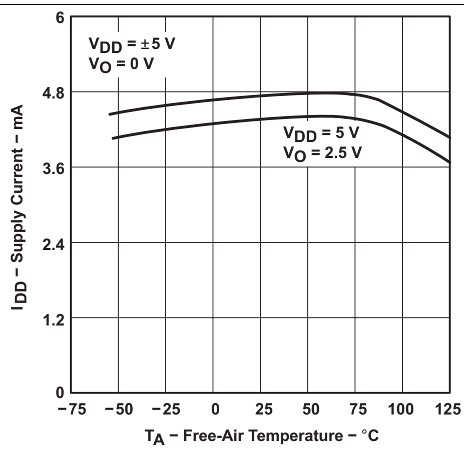


Figure 39. TLC2274 Supply Current vs Free-Air Temperature

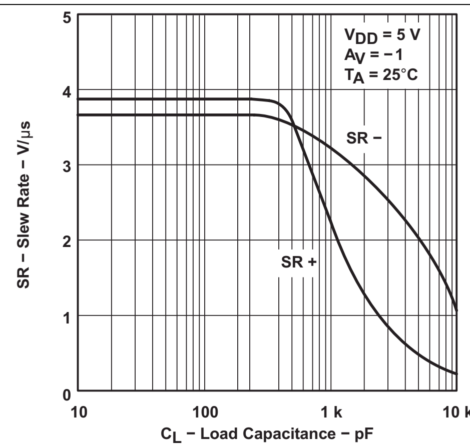


Figure 40. Slew Rate vs Load Capacitance

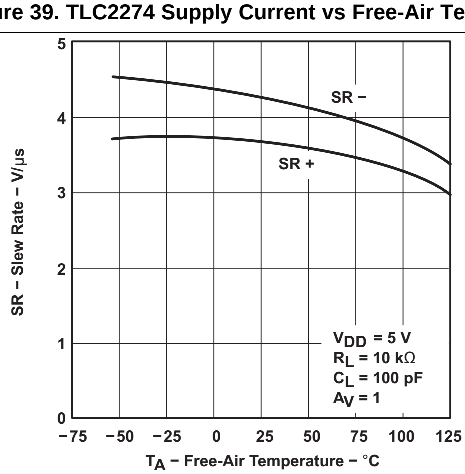


Figure 41. Slew Rate vs Free-Air Temperature

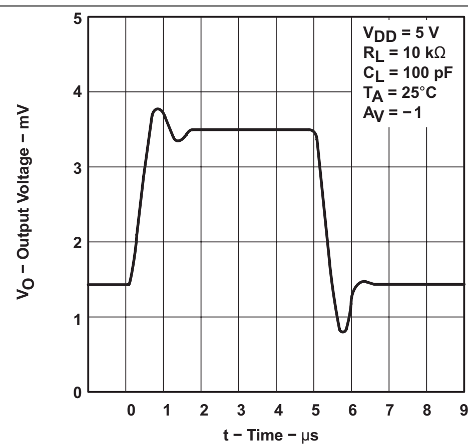


Figure 42. Inverting Large-Signal Pulse Response

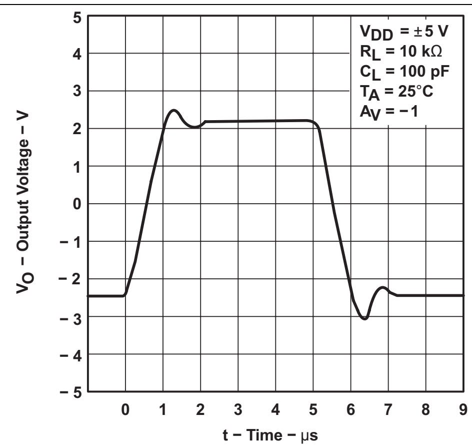


Figure 43. Inverting Large-Signal Pulse Response

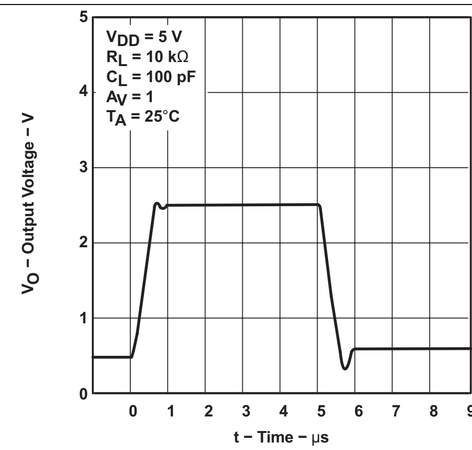


Figure 44. Voltage-Follower Large-Signal Pulse Response

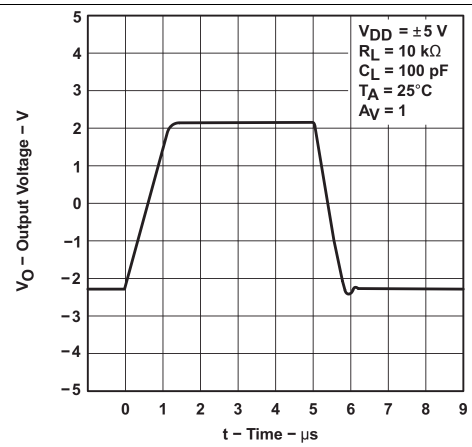


Figure 45. Voltage-Follower Large-Signal Pulse Response

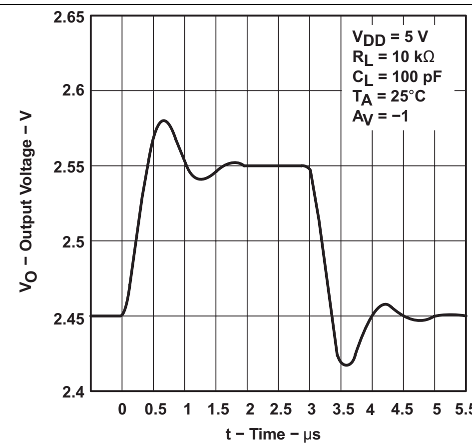


Figure 46. Inverting Small-Signal Pulse Response

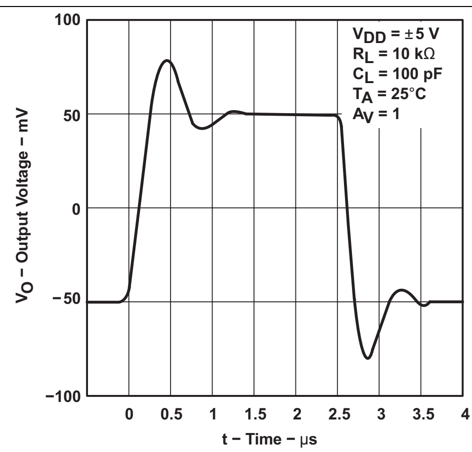


Figure 47. Inverting Small-Signal Pulse Response

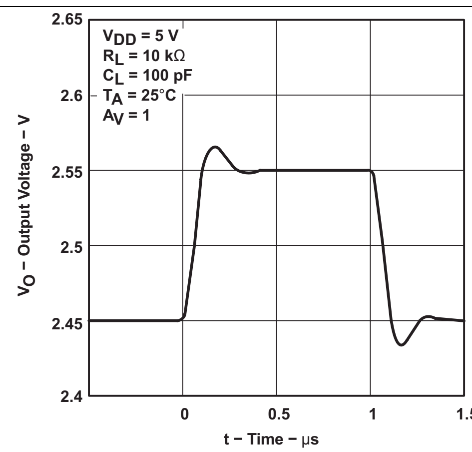


Figure 48. Voltage-Follower Small-Signal Pulse Response

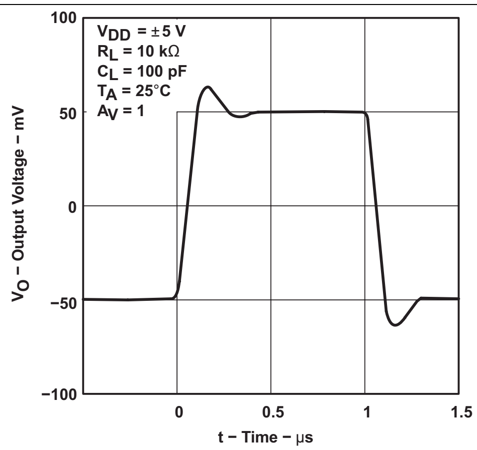


Figure 49. Voltage-Follower Small-Signal Pulse Response

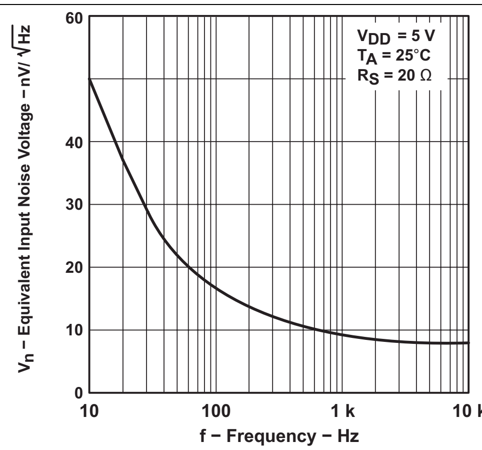


Figure 50. Equivalent Input Noise Voltage vs Frequency

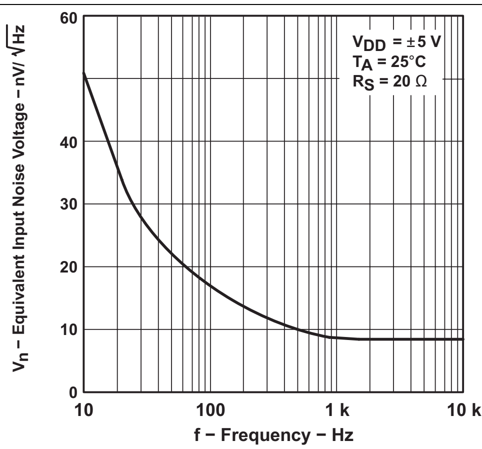


Figure 51. Equivalent Input Noise Voltage vs Frequency

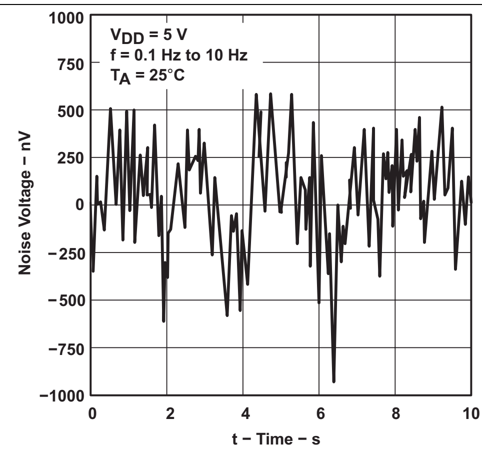


Figure 52. Noise Voltage Over a 10 Second Period

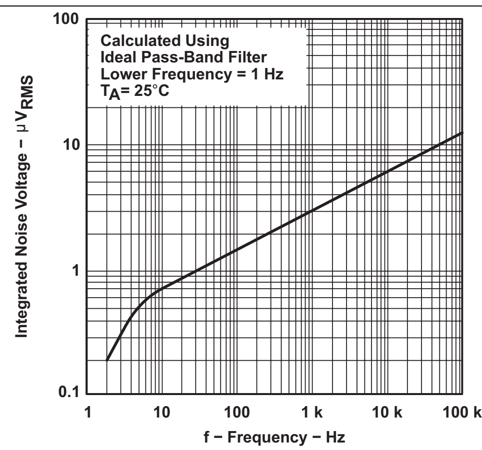


Figure 53. Integrated Noise Voltage vs Frequency

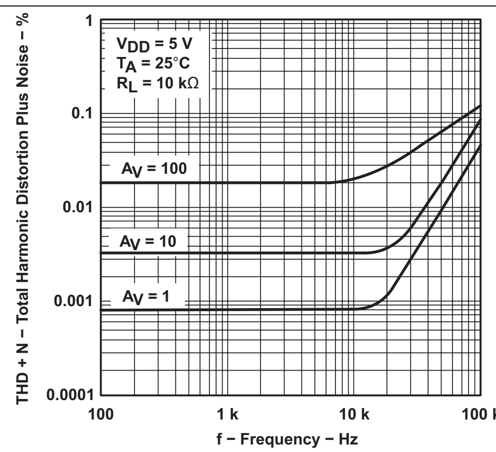


Figure 54. Total Harmonic Distortion + Noise vs Frequency

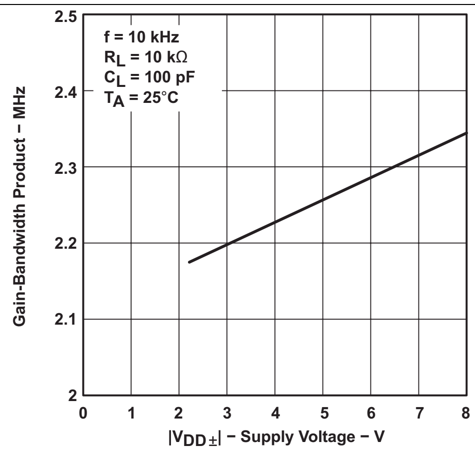


Figure 55. Gain-Bandwidth Product vs Supply Voltage

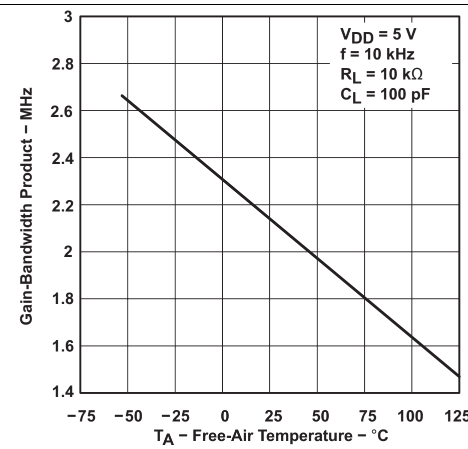


Figure 56. Gain-Bandwidth Product vs Free-Air Temperature

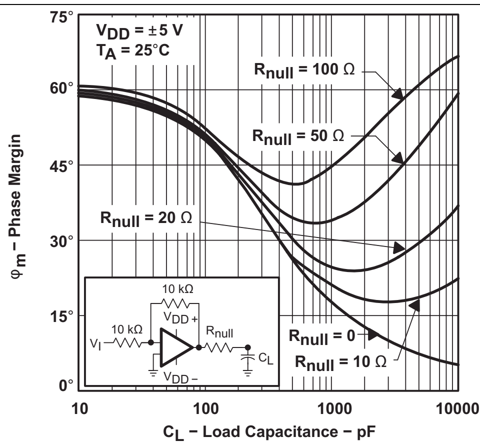


Figure 57. Phase Margin vs Load Capacitance

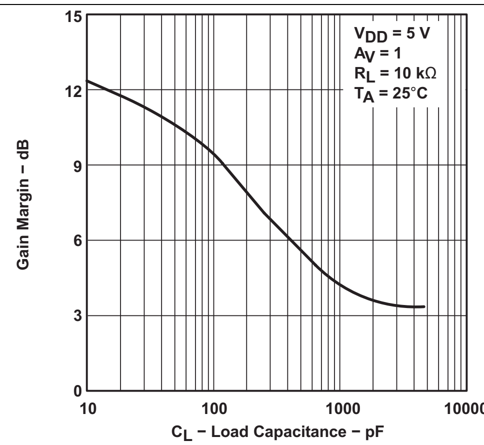


Figure 58. Gain Margin vs Load Capacitance

7 Detailed Description

7.1 Overview

The TLC227x and TLC227xA families of devices are rail-to-rail output operational amplifiers. These devices operate from 4.4-V to 16-V single supply and ±2.2-V ±8-V dual supply, are unity-gain stable, and are suitable for a wide range of general-purpose applications.

7.2 Functional Block Diagram

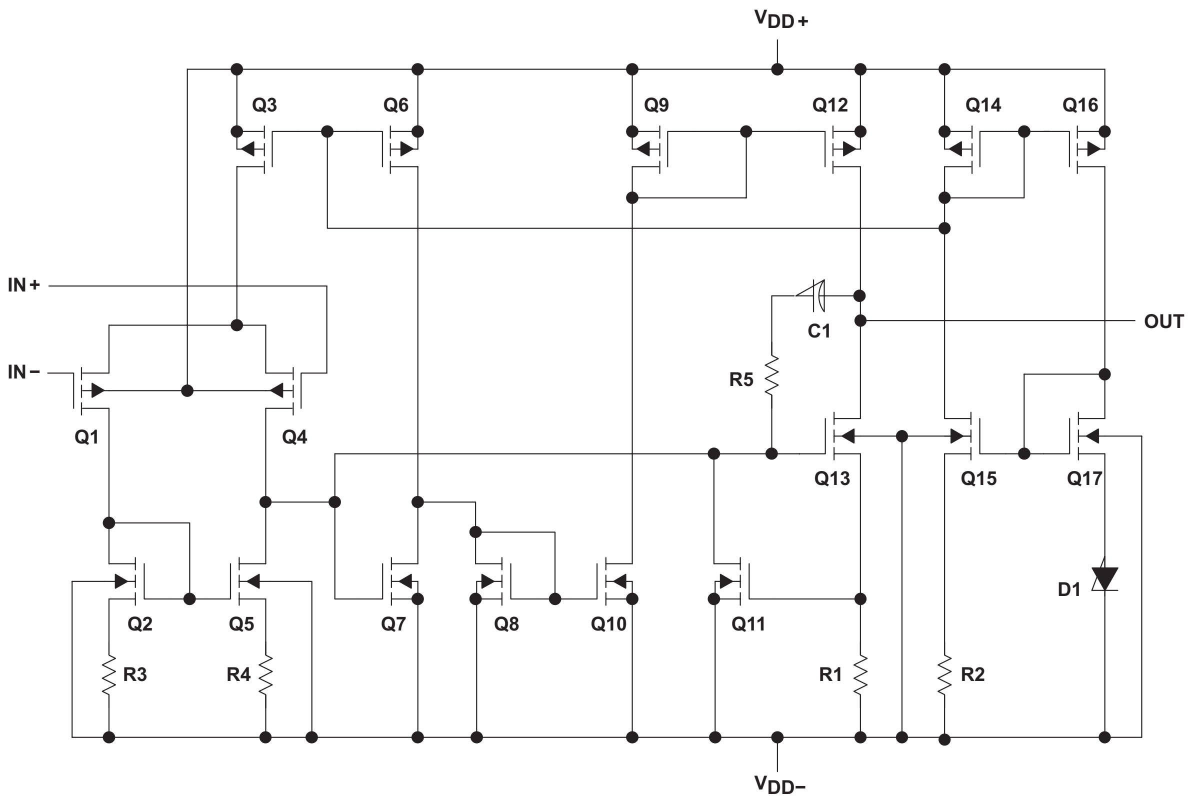


Table 2. Device Component Count(1)

Component	TLC2272	TLC2274
Transistors	38	76
Resistors	26	52
Diodes	9	18
Capacitors	3	6

(1) Includes both amplifiers and all ESD, bias, and trim circuitry.

7.3 Feature Description

The TLC227x and TLC227xA family of devices feature 2-MHz bandwidth and voltage noise of 9 nV/$\sqrt{\text{Hz}}$ with performance rated from 4.4 V to 16 V across an automotive temperature range (–40°C to 125°C). LinMOS suits a wide range of audio, automotive, industrial, and instrumentation applications.

7.4 Device Functional Modes

The TLC227x and TLC227xA families of devices is powered on when the supply is connected. The devices may operate with single or dual supply, depending on the application. The devices are in its full performance once the supply is above the recommended value.

8 Application and Implementation

NOTE

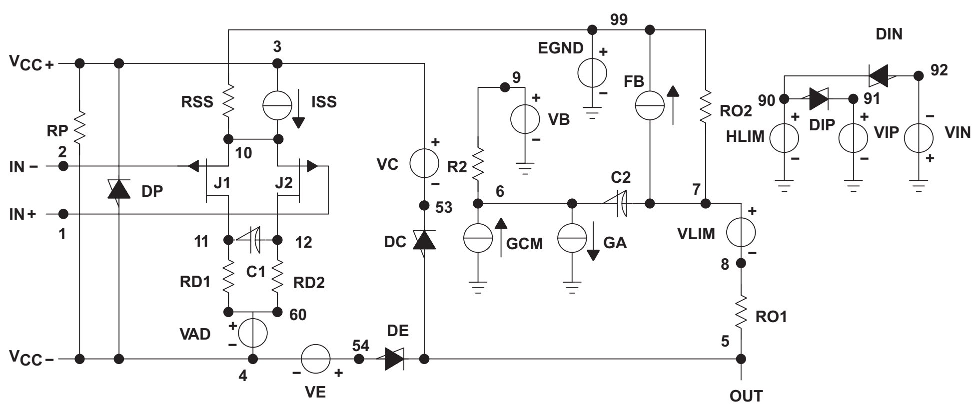
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Macromodel Information

Macromodel information provided was derived using MicroSim Parts™, the model generation software used with MicroSim PSpice™. The Boyle macromodel [(1)] and subcircuit in Figure 59 were generated using the TLC227x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit




```
.SUBCKT TLC227x 1 2 3 4 5
        C1      11      1214E−12
        C2      6       760.00E−12
        DC      5       53DX
        DE      54      5DX
        DLP     90      91DX
        DLN     92      90DX
        DP      4       3DX
        EGND    99      0POLY (2) (3,0) (4,) 0 .5 .5
        FB      99      0POLY (5) VB VC VE VLP VLN 0
        + 984.9E3 −1E6 1E6 1E6 −1E6
        GA      6       011 12 377.0E−6
        GCM 0 6 10 99 134E−9
        ISS     3       10DC 216.OE−6
        HLIM    90      0VLIM 1K
        J1      11      210 JX
        J2      12      110 JX
        R2      6       9100.OE3

RD1     60      112.653E3
RD2     60      122.653E3
R01     8       550
R02     7       9950
RP      3       44.310E3
RSS     10      99925.9E3
VAD     60      4−.5
VB      9       0DC 0
VC 3 53 DC .78
VE      54      4DC .78
VLIM    7       8DC 0
VLP     91      0DC 1.9
VLN     0       92DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=1.500E−12BETA=1.316E-3
+ VTO=−.270)
.ENDS
```

Figure 59. Boyle Macromodel and Subcircuit

(1) *Macromodeling of Integrated Circuit Operational Amplifiers*, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

8.2 Typical Application

8.2.1 High-Side Current Monitor

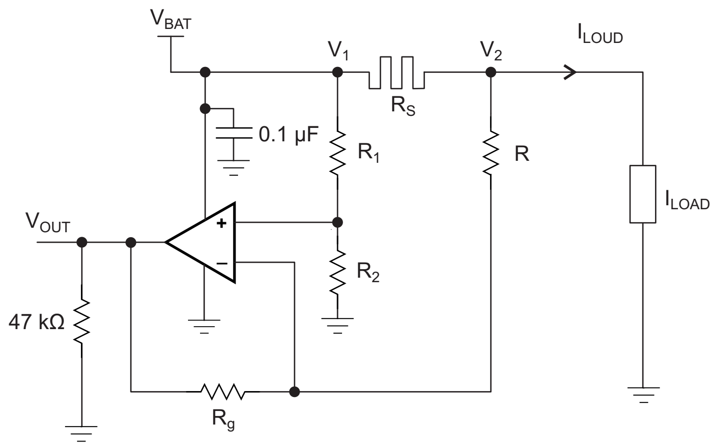


Figure 60. Equivalent Schematic (Each Amplifier)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

PARAMETER		VALUE
V_{BAT}	Battery Voltage	12 V
R_{SENSE}	Sense Resistor	0.1 Ω
I_{LOAD}	Load Current	0 A to 10 A
	Operational Amplifier	Set in Differential configuration with Gain = 10

8.2.1.2 Detailed Design Procedure

This circuit is designed for measuring the high-side current in automotive body control modules with 12-V battery or similar applications. The operational amplifier is set as differential with an external resistor network.

8.2.1.2.1 Differential Amplifier Equations

Equation 1 and Equation 2 are used to calculate V_{OUT}.

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g} - \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}} \times \frac{V_1 + V_2}{2} + \frac{1 + \frac{1}{2}\left(\frac{R_1}{R_2} + \frac{R}{R_g}\right)}{1 + \frac{R_1}{R_2}}(V_1 - V_2)\right) \tag{1}$$

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g} - \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}} \times V_{BAT} + \frac{1 + \frac{1}{2}\left(\frac{R_1}{R_2} + \frac{R}{R_g}\right)}{1 + \frac{R_1}{R_2}} \times R_S \times I_{Load}\right) \tag{2}$$

In an ideal case $R_1 = R$ and $R_2 = R_g$, and V_{OUT} can then be calculated using Equation 3:

$$V_{OUT} = \frac{R_g}{R} \times R_S \times I_{Load} \tag{3}$$

However, as the resistors have tolerances, they cannot be perfectly matched.

$R_1 = R \pm \Delta R_1$

$R_2 = R_2 \pm \Delta R_2$

$R = R \pm \Delta R$

$R_g = R_g \pm \Delta R_g$

$$\text{Tol} = \frac{DR}{R} \tag{4}$$

By developing the equations and neglecting the second order, the worst case is when the tolerances add up. This is shown by Equation 5.

$$V_{OUT} = \pm\,(4\ \text{Tol})\frac{R_g}{R + R_g} \times V_{BAT} + \left(1 \pm 2\ \text{Tol}\left(1 + \frac{2R}{R + R_g}\right)\right)\frac{R_g}{R} \times R_S \times I_{LOAD}$$

where

- Tol = 0.01 for 1%
- Tol = 0.001 for 0.1% (5)

If the resistors are perfectly matched, then Tol = 0 and V_{OUT} is calculated using Equation 6.

$$V_{OUT} = \frac{R_g}{R} \times R_S \times I_{LOAD} \tag{6}$$

The highest error is from the Common mode, as shown in Equation 7.

$$4\ (\text{Tol})\frac{R_g}{R + R_g} \times V_{BAT} \tag{7}$$

Gain of 10, R_g / R = 10, and Tol = 1%:

Common mode error = ((4 × 0.01) / 1.1) × 12 V = 0.436 V

Gain of 10 and Tol = 0.1%:

Common mode error = 43.6 mV

The resistors were chosen from 2% batches.

R_1 and R 12 kΩ

R_2 and R_g 120 kΩ

Ideal Gain = 120 / 12 = 10

The measured value of the resistors:

R_1 = 11.835 kΩ

R = 11.85 kΩ

R_2 = 117.92 kΩ

R_g = 118.07 kΩ

8.2.1.3 Application Curves

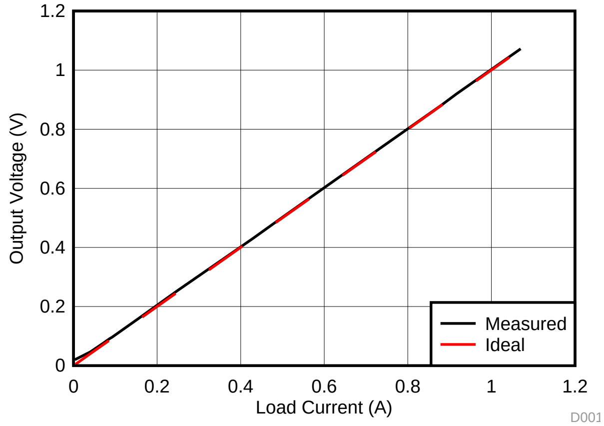


Figure 61. Output Voltage Measured vs Ideal (0 to 1 A)

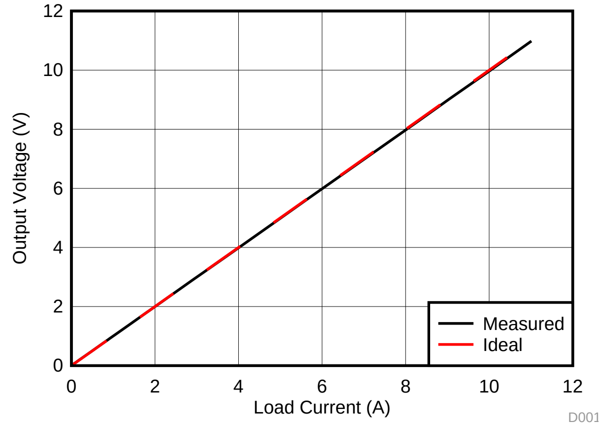


Figure 62. Output Voltage Measured vs Ideal (0 to 10 A)

9 Power Supply Recommendations

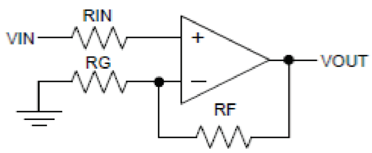
Supply voltage for a single supply is from 4.4 V to 16 V, and from ±2.2 V to ±8 V for dual supply. In the high-side sensing application, the supply is connected to a 12-V battery.

10 Layout

10.1 Layout Guidelines

The TLC227x and TLC227xA families of devices are wideband amplifiers. To realize the full operational performance of the devices, good high-frequency printed-circuit-board (PCB) layout practices are required. Low-loss 0.1-μF bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

10.2 Layout Example



(Schematic Representation)

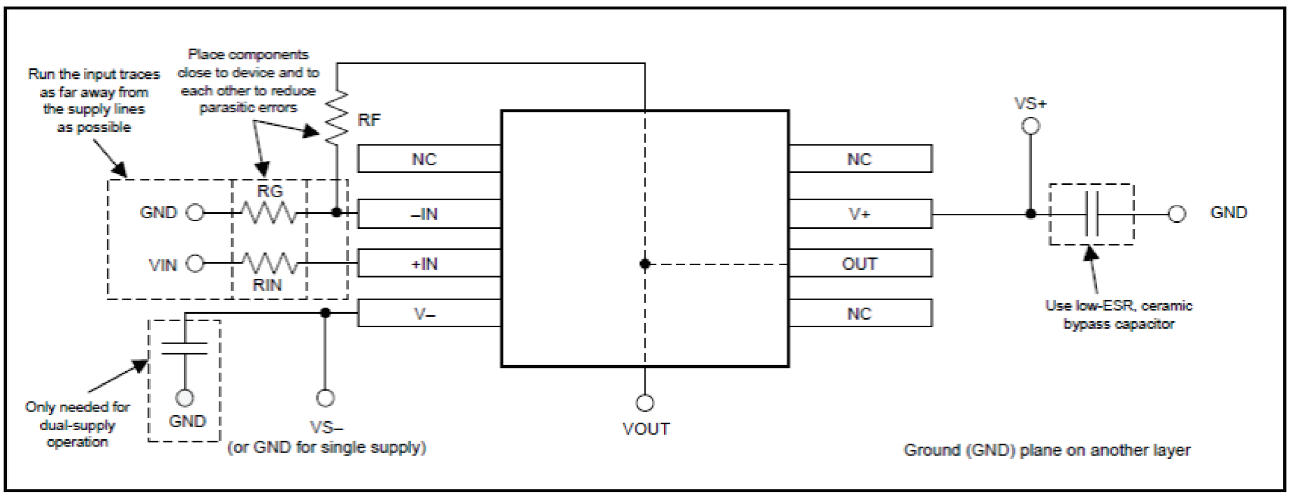


Figure 63. Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLC2272	Click here	Click here	Click here	Click here	Click here
TLC2272A	Click here	Click here	Click here	Click here	Click here
TLC2272M	Click here	Click here	Click here	Click here	Click here
TLC2272AM	Click here	Click here	Click here	Click here	Click here
TLC2274	Click here	Click here	Click here	Click here	Click here
TLC2274A	Click here	Click here	Click here	Click here	Click here
TLC2274M	Click here	Click here	Click here	Click here	Click here
TLC2274AM	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
MicroSim Parts, PSpice are trademarks of MicroSim.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2272ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AC	Samples
TLC2272ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AC	Samples
TLC2272ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AC	Samples
TLC2272ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AC	Samples
TLC2272ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272AC	Samples
TLC2272ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272AC	Samples
TLC2272ACPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2272A	Samples
TLC2272ACPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2272A	Samples
TLC2272ACPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2272A	Samples
TLC2272ACPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2272A	Samples
TLC2272AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AI	Samples
TLC2272AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AI	Samples
TLC2272AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AI	Samples
TLC2272AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AI	Samples
TLC2272AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272AI	Samples
TLC2272AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272AI	Samples
TLC2272AMD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2272AMDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AM	Samples
TLC2272AMDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AM	Samples
TLC2272AMDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AM	Samples
TLC2272AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2272A	Samples
TLC2272AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C2272A	Samples
TLC2272AQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2272A	Samples
TLC2272AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C2272A	Samples
TLC2272CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2272C	Samples
TLC2272CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2272C	Samples
TLC2272CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2272C	Samples
TLC2272CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2272C	Samples
TLC2272CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2272CP	Samples
TLC2272CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2272CP	Samples
TLC2272CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2272	Samples
TLC2272CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2272	Samples
TLC2272CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2272	Samples
TLC2272CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2272	Samples
TLC2272CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2272	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2272ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272I	Samples
TLC2272IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272I	Samples
TLC2272IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272I	Samples
TLC2272IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272I	Samples
TLC2272IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272IP	Samples
TLC2272IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272IP	Samples
TLC2272IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2272	Samples
TLC2272IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2272	Samples
TLC2272IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2272	Samples
TLC2272IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2272	Samples
TLC2272MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272M	Samples
TLC2272MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272M	Samples
TLC2272MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272M	Samples
TLC2272MDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272M	Samples
TLC2272QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C2272Q	Samples
TLC2272QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2272Q	Samples
TLC2272QPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		T2272Q	Samples
TLC2274ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2274AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2274ACDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2274AC	Samples
TLC2274ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2274AC	Samples
TLC2274ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2274AC	Samples
TLC2274ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2274ACN	Samples
TLC2274ACNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2274ACN	Samples
TLC2274ACPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2274A	Samples
TLC2274ACPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2274A	Samples
TLC2274ACPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2274A	Samples
TLC2274ACPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2274A	Samples
TLC2274AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AI	Samples
TLC2274AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AI	Samples
TLC2274AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AI	Samples
TLC2274AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AI	Samples
TLC2274AIN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLC2274AIN	Samples
TLC2274AINE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLC2274AIN	Samples
TLC2274AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2274A	Samples
TLC2274AIPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2274A	Samples
TLC2274AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2274A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2274AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2274A	Samples
TLC2274AMD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AM	Samples
TLC2274AMDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2274AM	Samples
TLC2274AMDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2274AM	Samples
TLC2274AQD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2274A	Samples
TLC2274AQDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PJ2274A	Samples
TLC2274AQDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2274A	Samples
TLC2274AQDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PJ2274A	Samples
TLC2274CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274C	Samples
TLC2274CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274C	Samples
TLC2274CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274C	Samples
TLC2274CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274C	Samples
TLC2274CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2274CN	Samples
TLC2274CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2274CN	Samples
TLC2274CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274	Samples
TLC2274CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2274	Samples
TLC2274CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2274	Samples
TLC2274CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2274	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2274CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2274	Samples
TLC2274ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274I	Samples
TLC2274IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274I	Samples
TLC2274IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274I	Samples
TLC2274IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274I	Samples
TLC2274IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2274IN	Samples
TLC2274IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2274	Samples
TLC2274IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2274	Samples
TLC2274IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2274	Samples
TLC2274IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2274	Samples
TLC2274MD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC2274M	Samples
TLC2274MDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PJ2274M	Samples
TLC2274MDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC2274M	Samples
TLC2274MDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PJ2274M	Samples
TLC2274MN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	TLC2274MN	Samples
TLC2274QD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2274	Samples
TLC2274QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274	Samples
TLC2274QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLC2272, TLC2272A, TLC2272AM, TLC2272M, TLC2274, TLC2274A, TLC2274AM, TLC2274M :

- Catalog: TLC2272A, TLC2272, TLC2274A, TLC2274

- Automotive: TLC2272-Q1, TLC2272A-Q1, TLC2272A-Q1, TLC2272-Q1, TLC2274-Q1, TLC2274A-Q1, TLC2274A-Q1, TLC2274-Q1

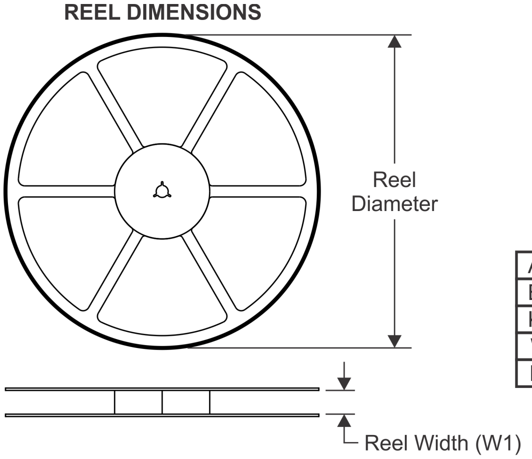
- Enhanced Product: TLC2272A-EP, TLC2272A-EP, TLC2274-EP, TLC2274A-EP, TLC2274A-EP, TLC2274-EP

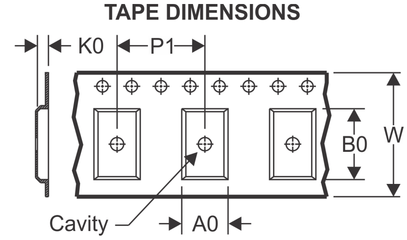
- Military: TLC2272M, TLC2272AM, TLC2274M, TLC2274AM

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

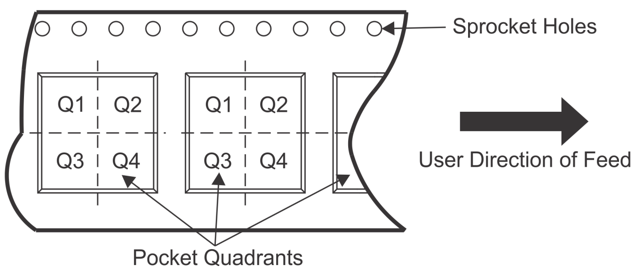
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

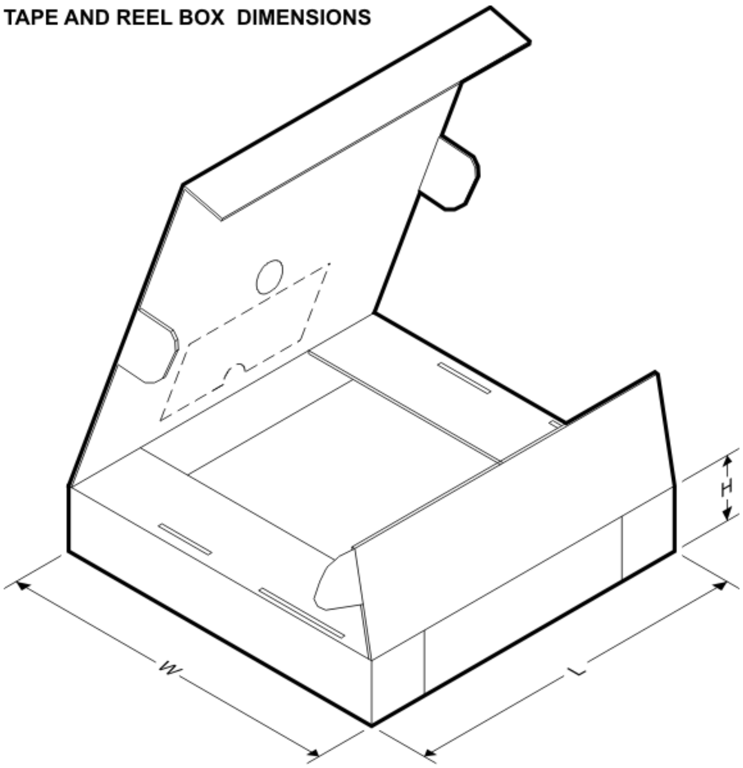


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2272ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272ACPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272AMDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272AMDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272AQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272QDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272QPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2274ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274AQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2274CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC2274CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274MDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274MDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274QDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



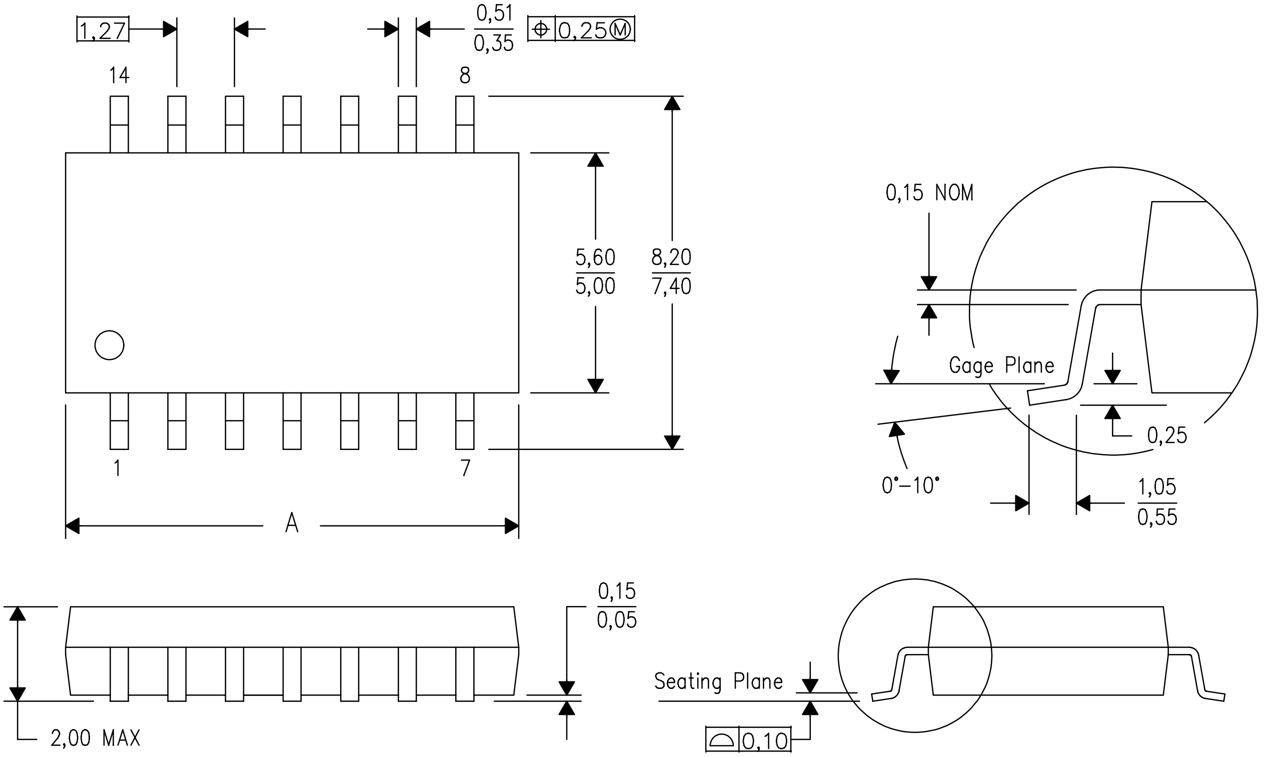
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2272ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272ACPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2272AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272AMDR	SOIC	D	8	2500	367.0	367.0	38.0
TLC2272AMDRG4	SOIC	D	8	2500	367.0	367.0	38.0
TLC2272AQDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2272IDR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2272IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2272MDR	SOIC	D	8	2500	367.0	367.0	38.0
TLC2272QDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272QPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2274ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274ACPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274AIDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274AQDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC2274CDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274CNSR	SO	NS	14	2000	367.0	367.0	38.0
TLC2274CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274MDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC2274MDRG4	SOIC	D	14	2500	367.0	367.0	38.0
TLC2274QDRG4	SOIC	D	14	2500	367.0	367.0	38.0

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

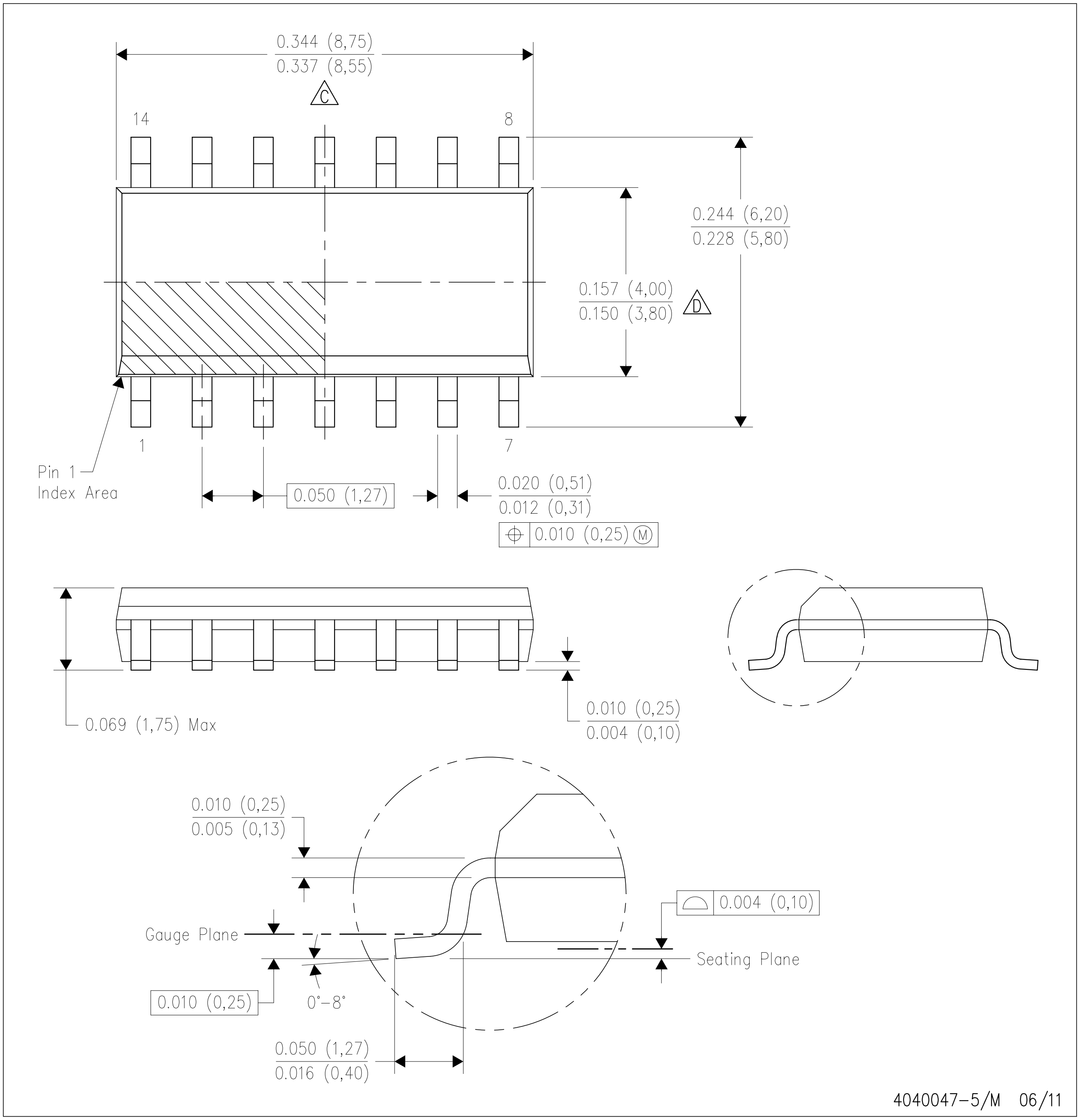


PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

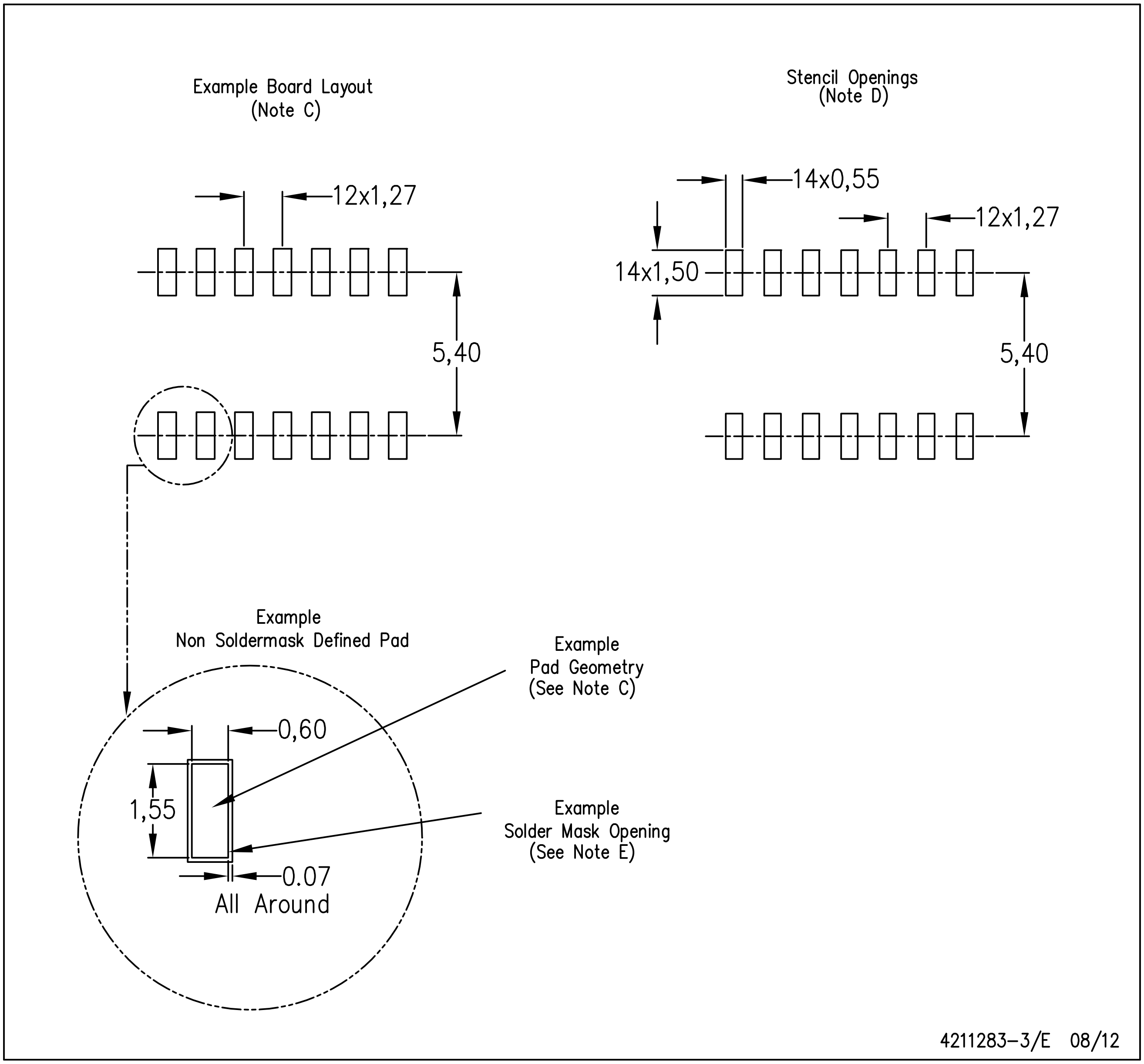
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



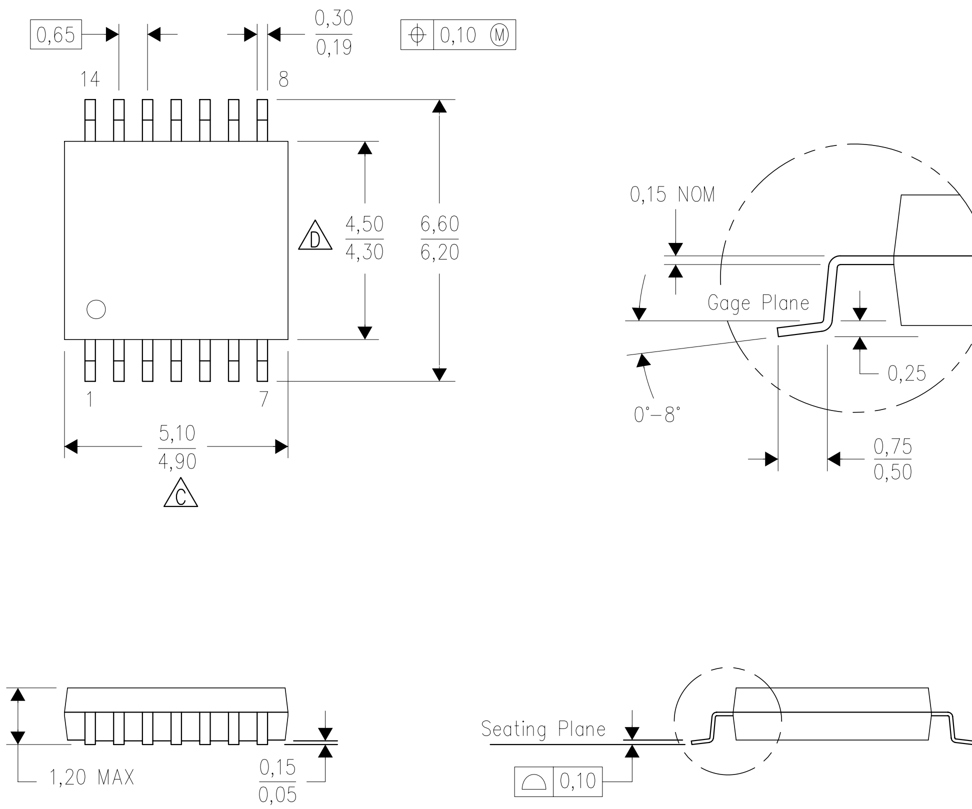
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

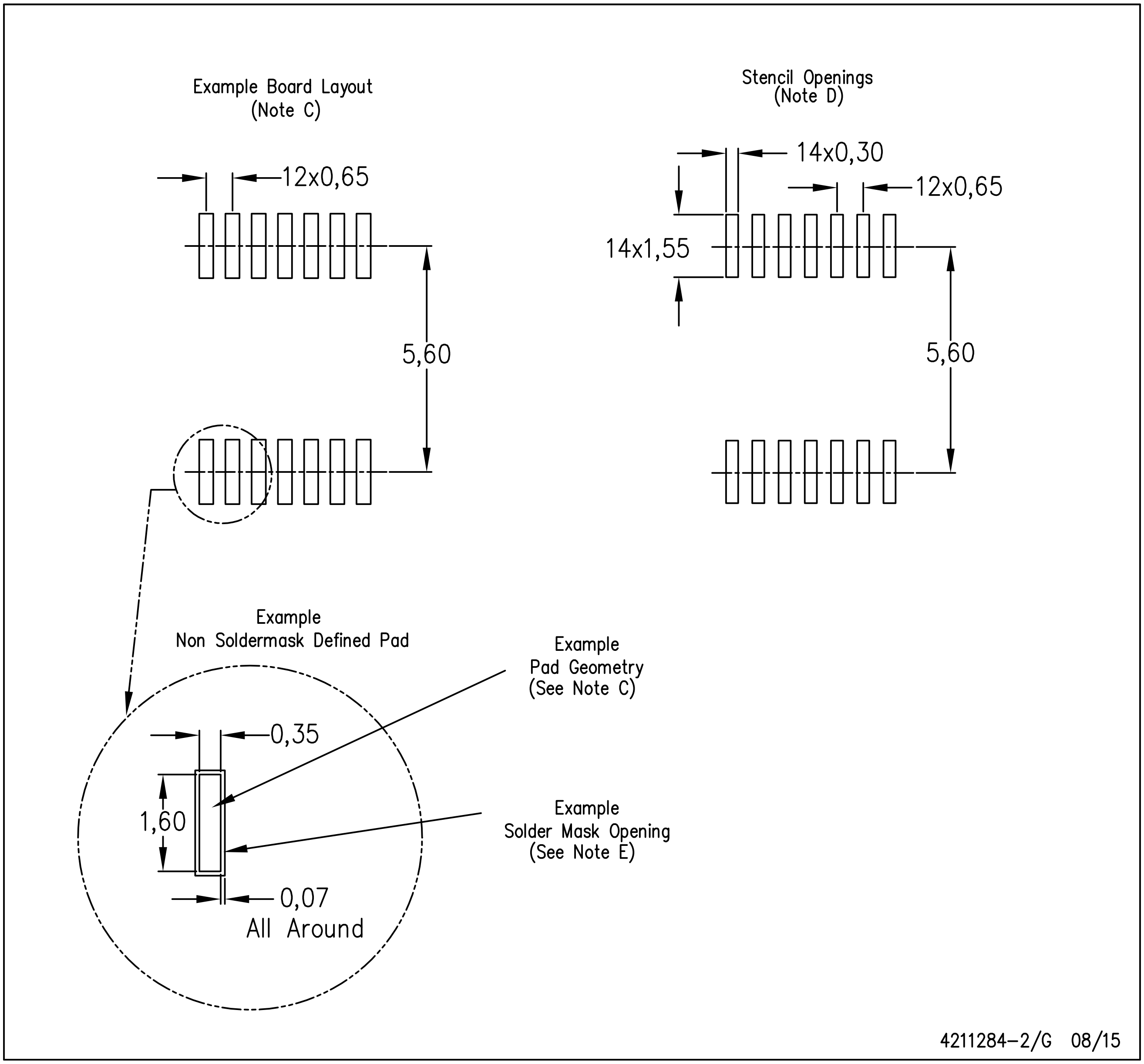
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

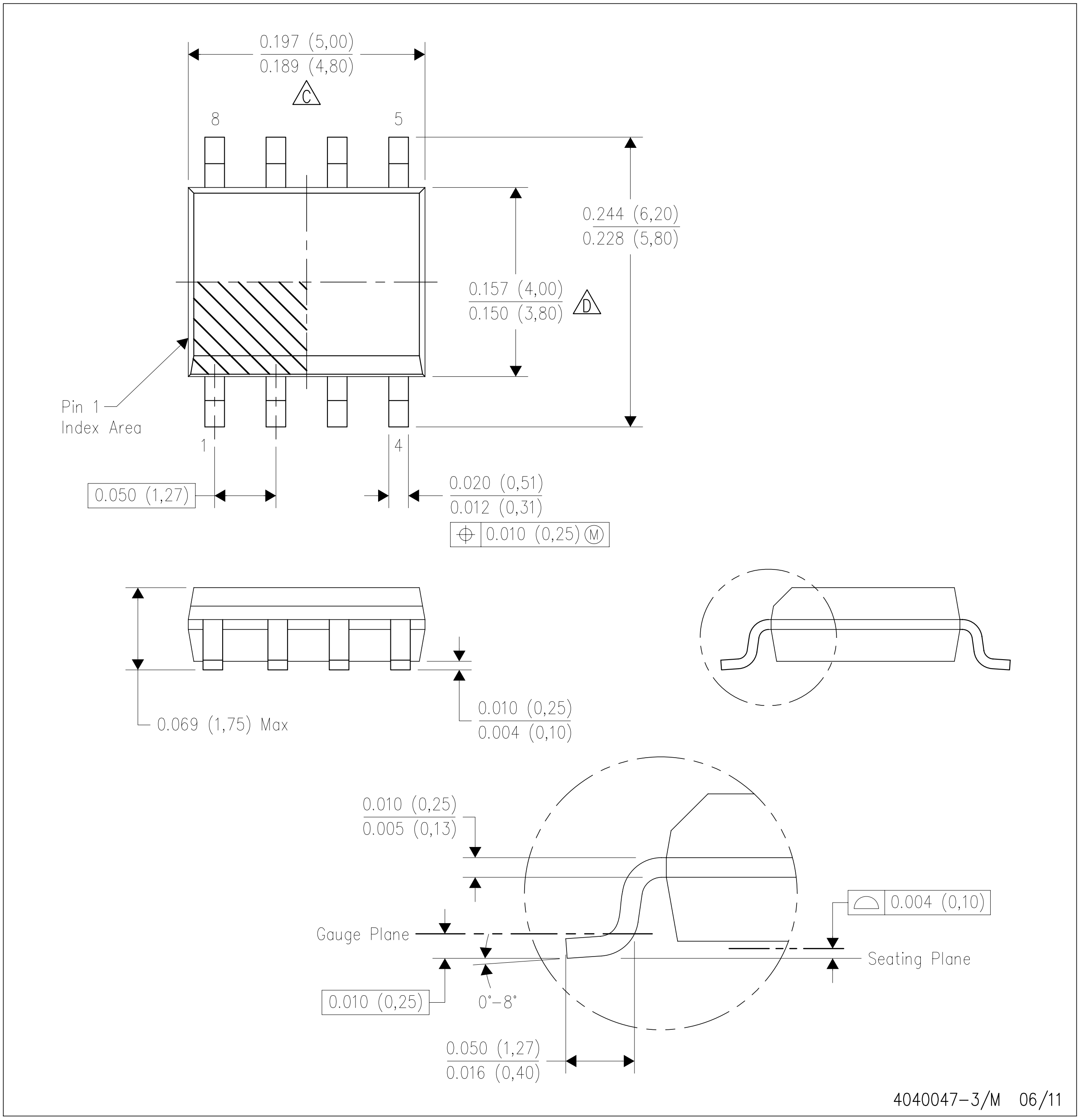
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



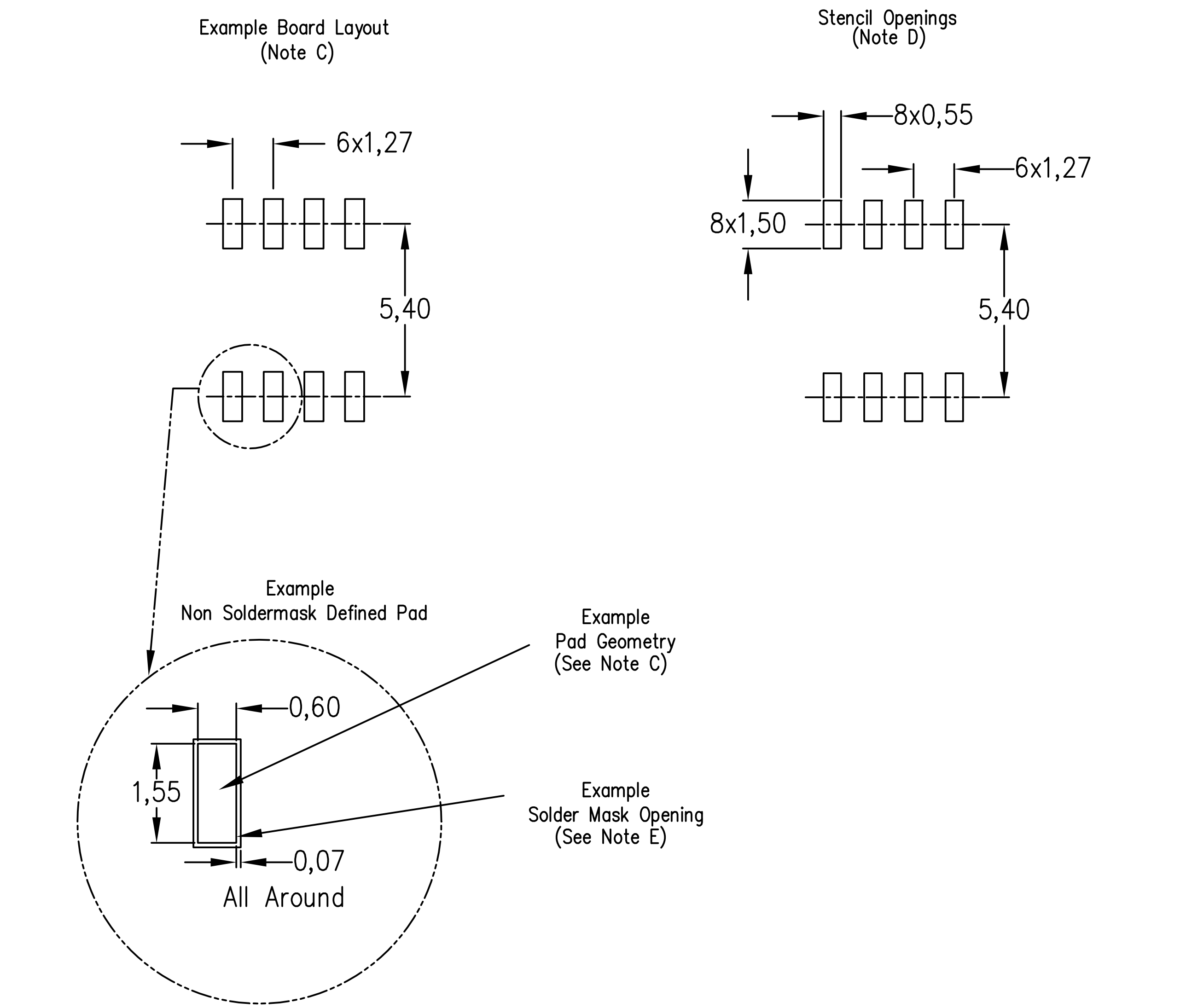
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

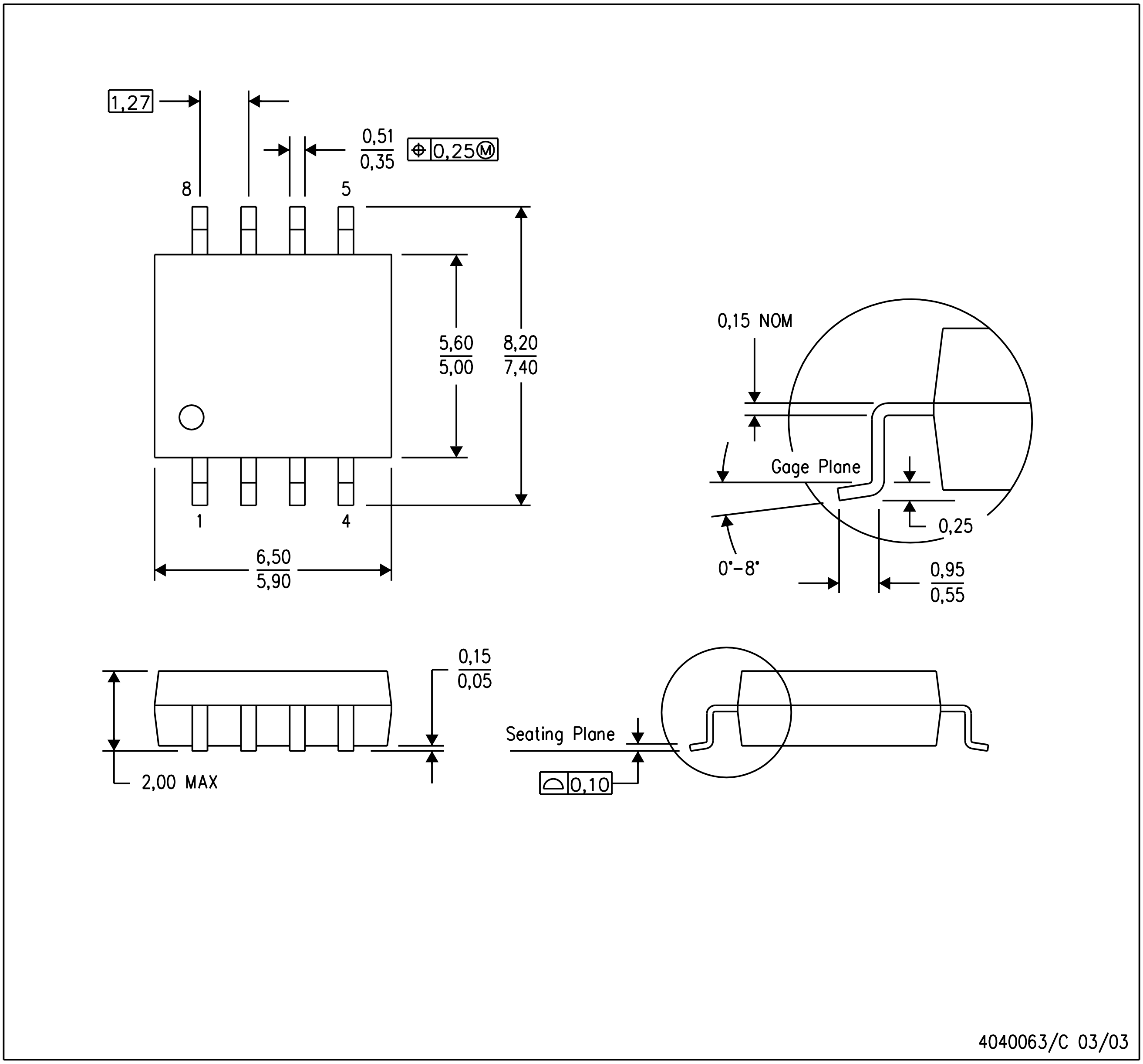
D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4211283-2/E 08/12

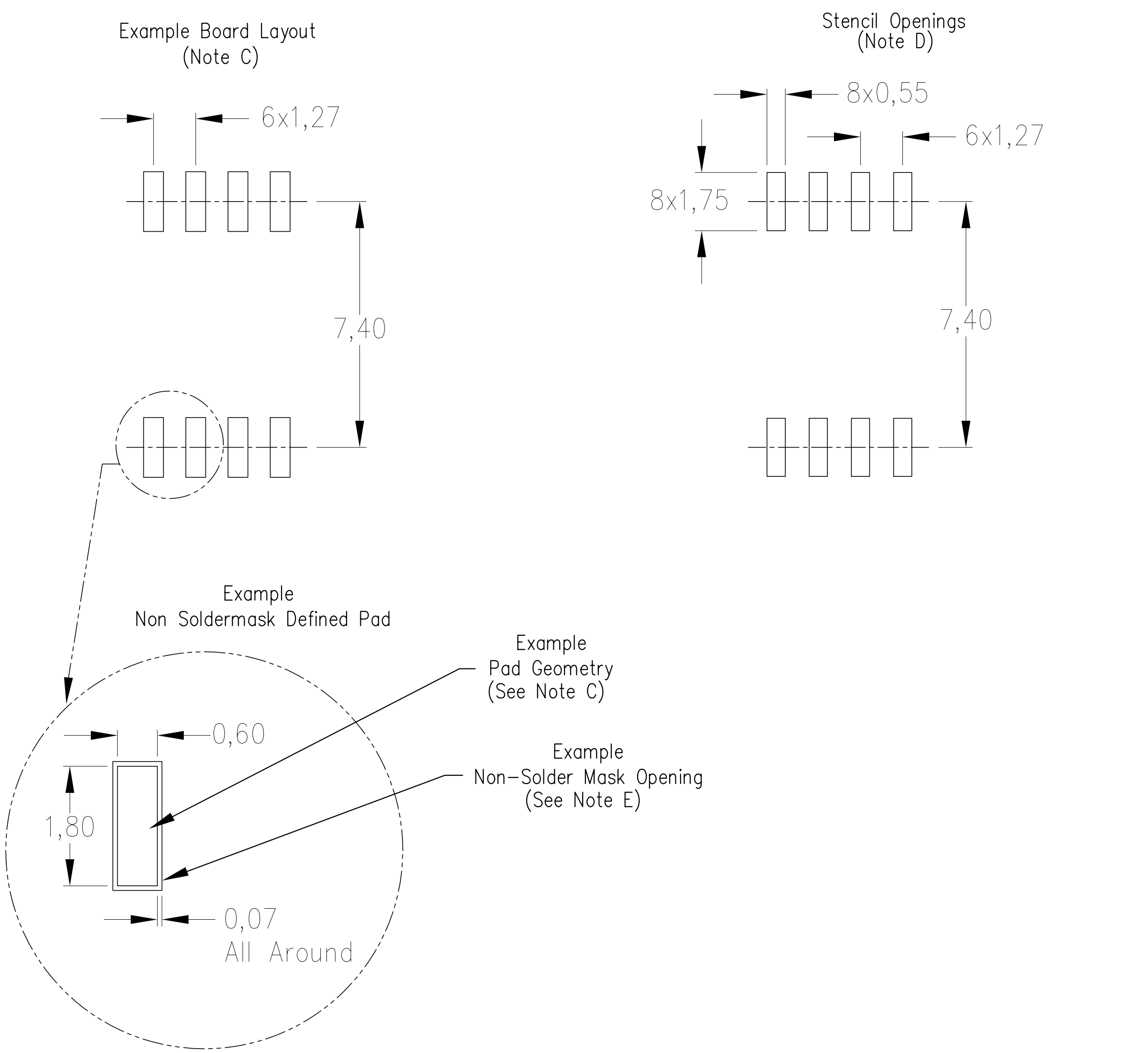
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

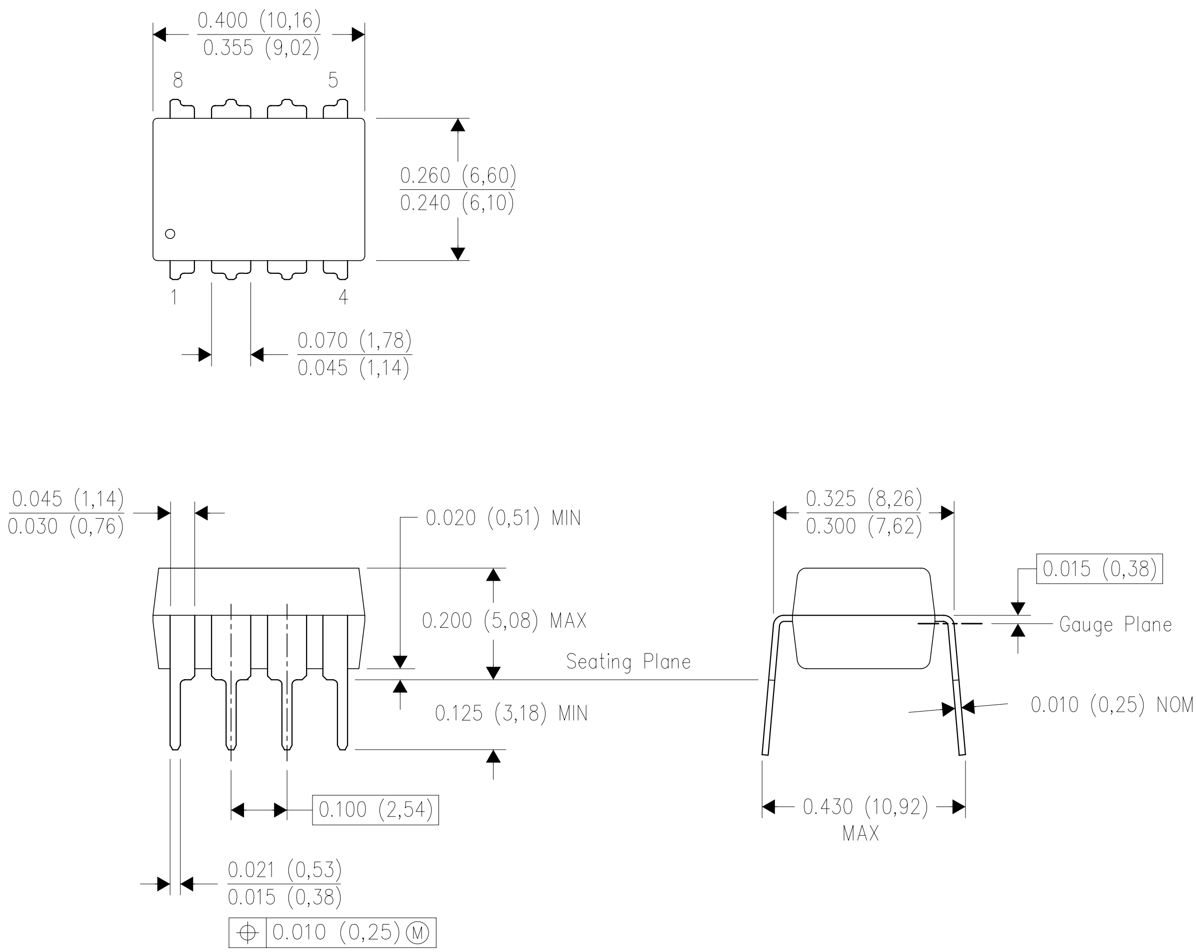
PS (R-PDSO-G8) PLASTIC SMALL OUTLINE



4212188/A 09/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

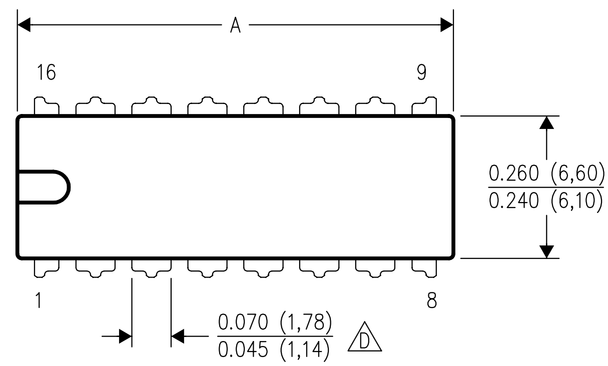


4040082/E 04/2010

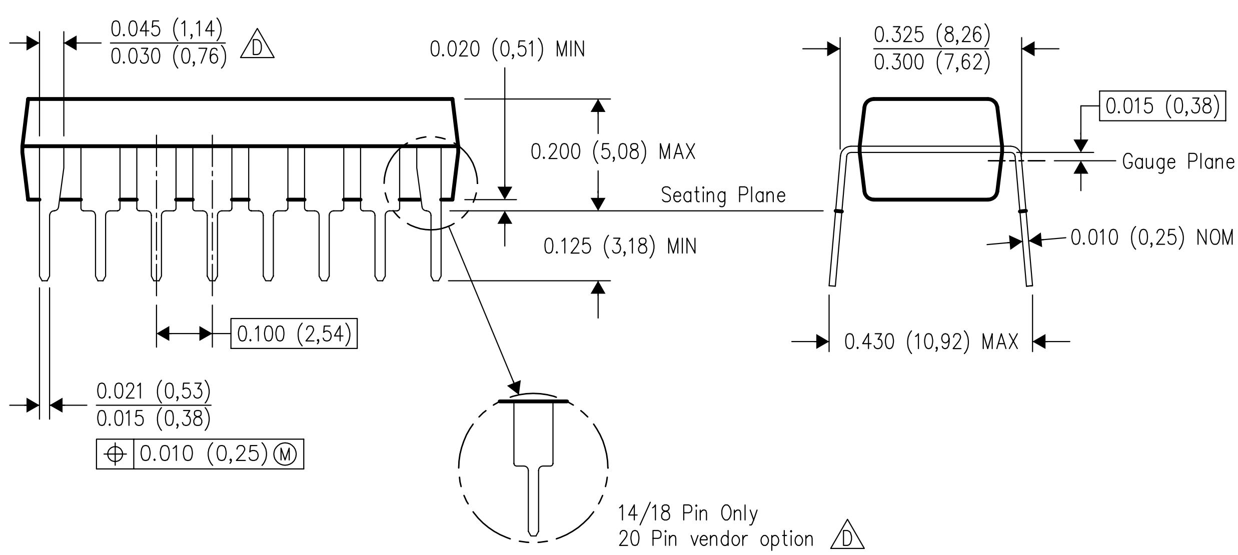
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

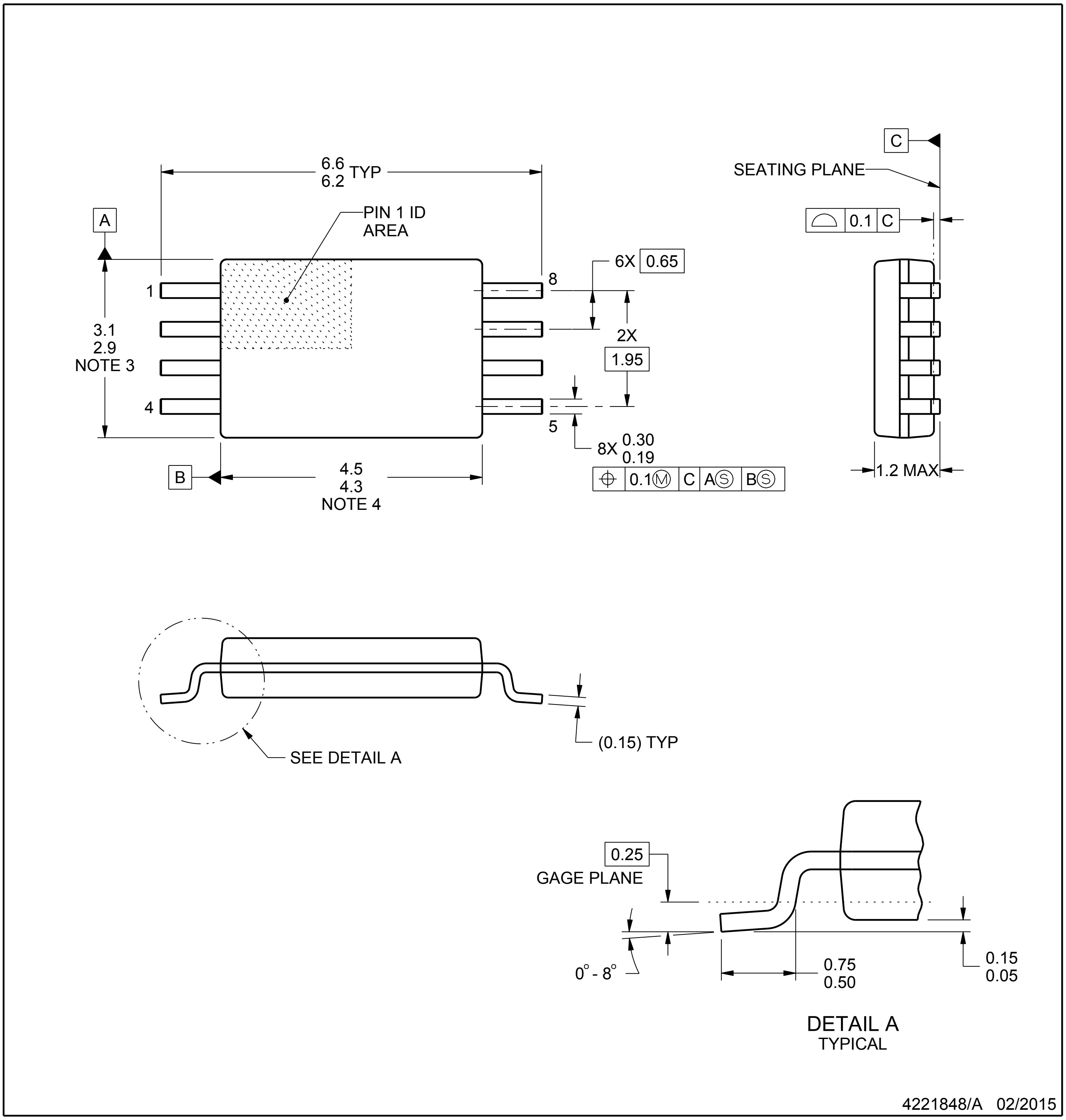


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



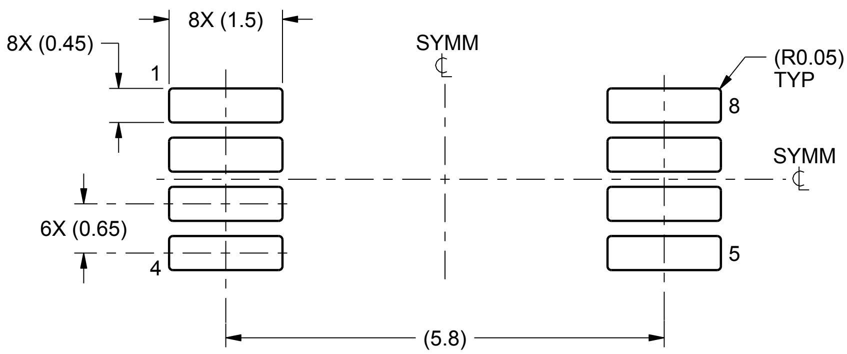
4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

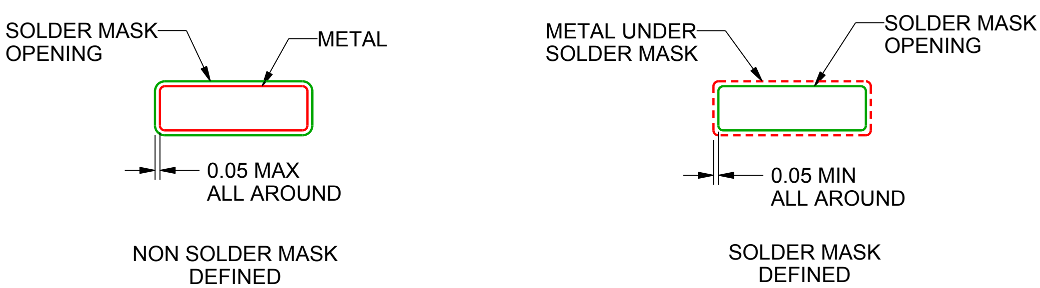


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

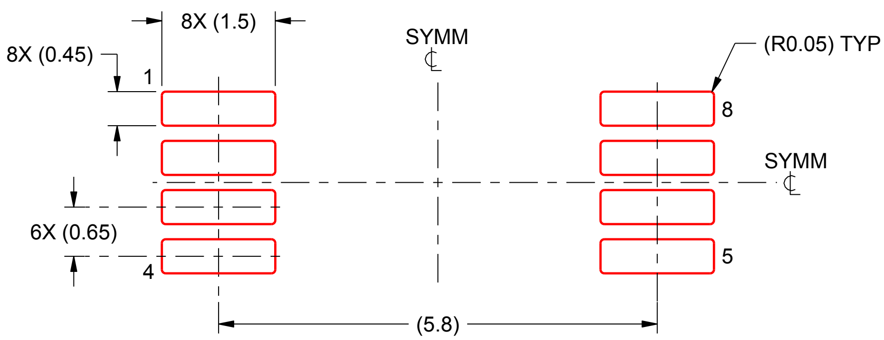


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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