

# IRFR/U3910

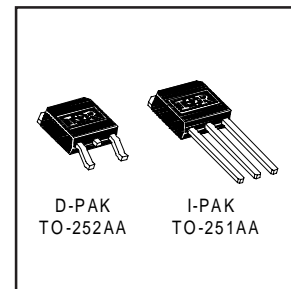
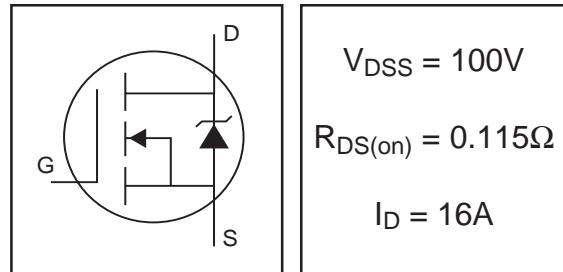
HEXFET® Power MOSFET

- Ultra Low On-Resistance
- Surface Mount (IRFR3910)
- Straight Lead (IRFU3910)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



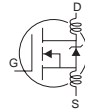
## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	16	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	12	
$I_{DM}$	Pulsed Drain Current ①⑥	60	
$P_D @ T_C = 25^\circ C$	Power Dissipation	79	W
	Linear Derating Factor	0.53	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy②⑥	150	mJ
$I_{AR}$	Avalanche Current①⑥	9.0	A
$E_{AR}$	Repetitive Avalanche Energy①⑥	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

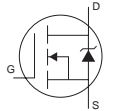
## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) **	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

**Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.115		V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	6.4	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 9.0A⑥
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	44	nC	I <sub>D</sub> = 9.0A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	6.2		V <sub>DS</sub> = 80V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	21		V <sub>GS</sub> = 10V, See Fig. 6 and 13 ④⑥
t <sub>d(on)</sub>	Turn-On Delay Time	—	6.4	—		ns
t <sub>r</sub>	Rise Time	—	27	—	I <sub>D</sub> = 9.0A	
t <sub>d(off)</sub>	Turn-Off Delay Time	—	37	—	R <sub>G</sub> = 12Ω	
t <sub>f</sub>	Fall Time	—	25	—	R <sub>D</sub> = 5.5Ω, See Fig. 10 ④⑥	
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact⑤
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	640	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	160	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	88	—		f = 1.0MHz, See Fig. 5⑥

**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	16	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①⑥	—	—	60		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 9.0A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	130	190	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 9.0A
Q <sub>rr</sub>	Reverse Recovery Charge	—	650	970	nC	di/dt = 100A/μs ④⑥
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② V<sub>DD</sub> = 25V, starting T<sub>J</sub> = 25°C, L = 3.1mH R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 9.0A. (See Figure 12)
- ③ I<sub>SD</sub> ≤ 9.0A, di/dt ≤ 520A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%
- ⑤ This is applied for I-PAK, L<sub>s</sub> of D-PAK is measured between lead and center of die contact
- ⑥ Uses IRF530N data and test conditions

\*\* When mounted on 1" square PCB (FR-4 or G-10 Material) .  
For recommended footprint and soldering techniques refer to application note #AN-994

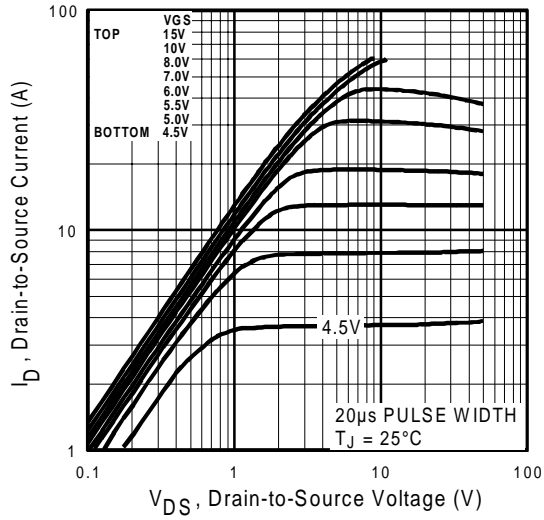


Fig 1. Typical Output Characteristics

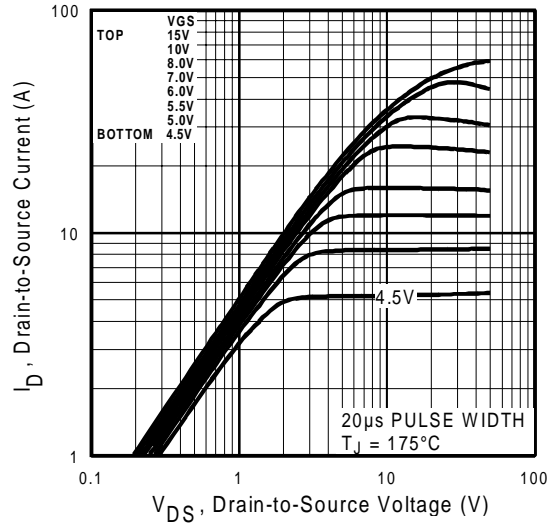


Fig 2. Typical Output Characteristics

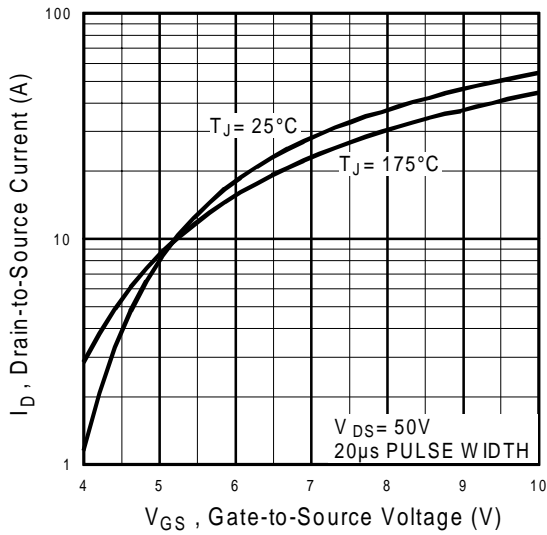


Fig 3. Typical Transfer Characteristics

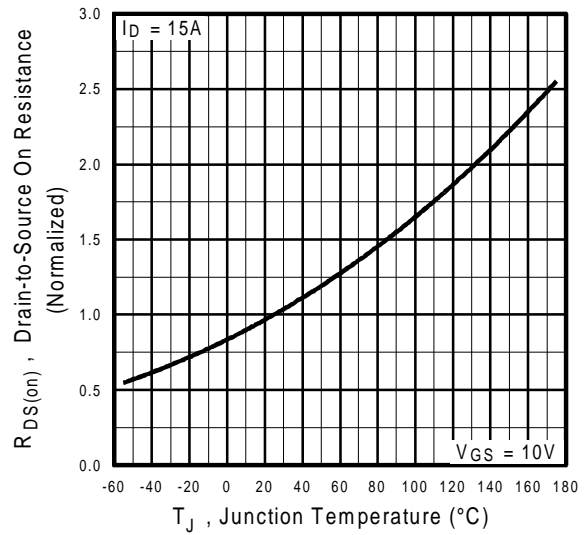
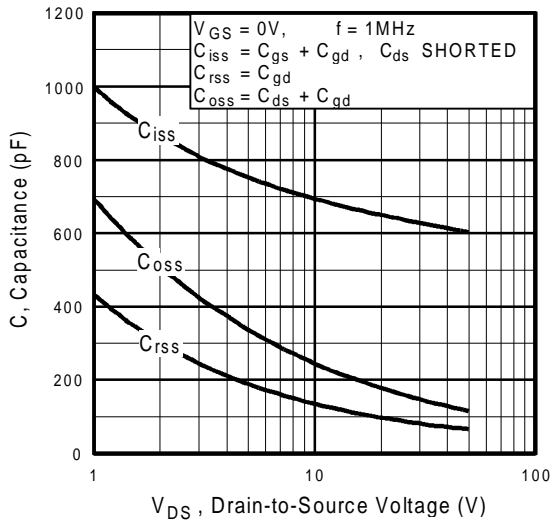
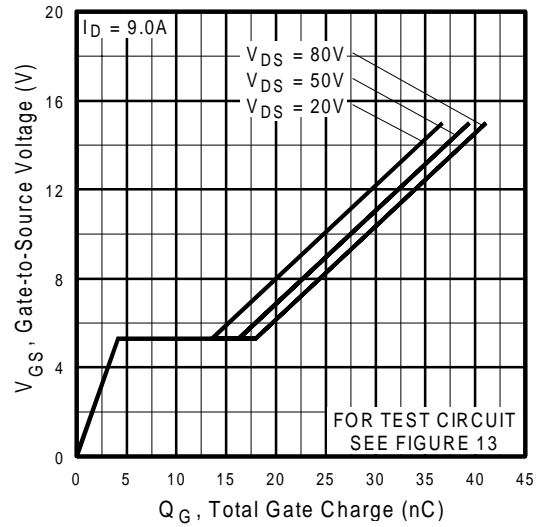


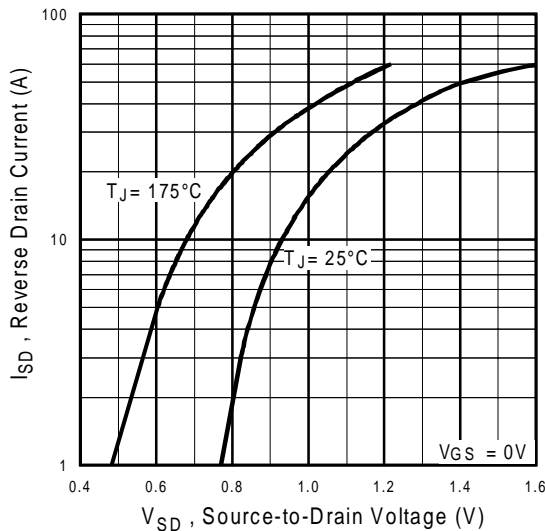
Fig 4. Normalized On-Resistance Vs. Temperature



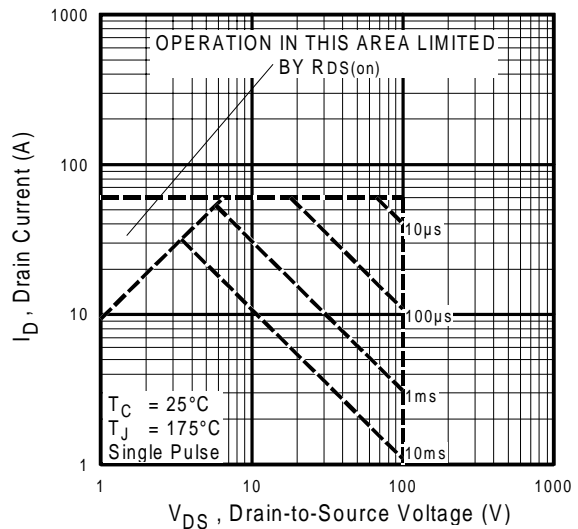
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



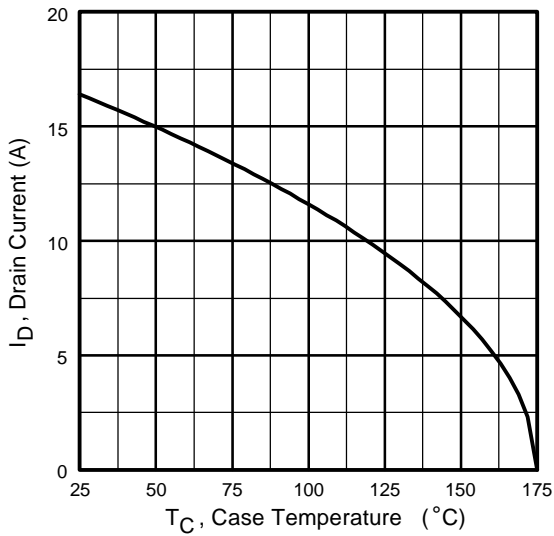
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



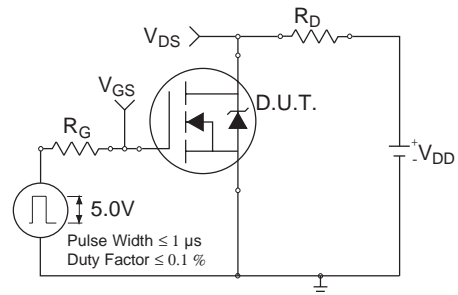
**Fig 7.** Typical Source-Drain Diode Forward Voltage



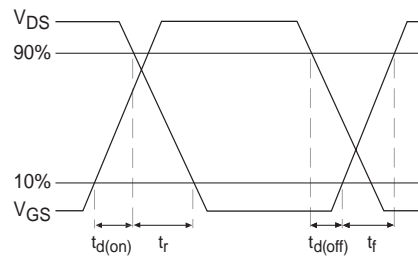
**Fig 8.** Maximum Safe Operating Area



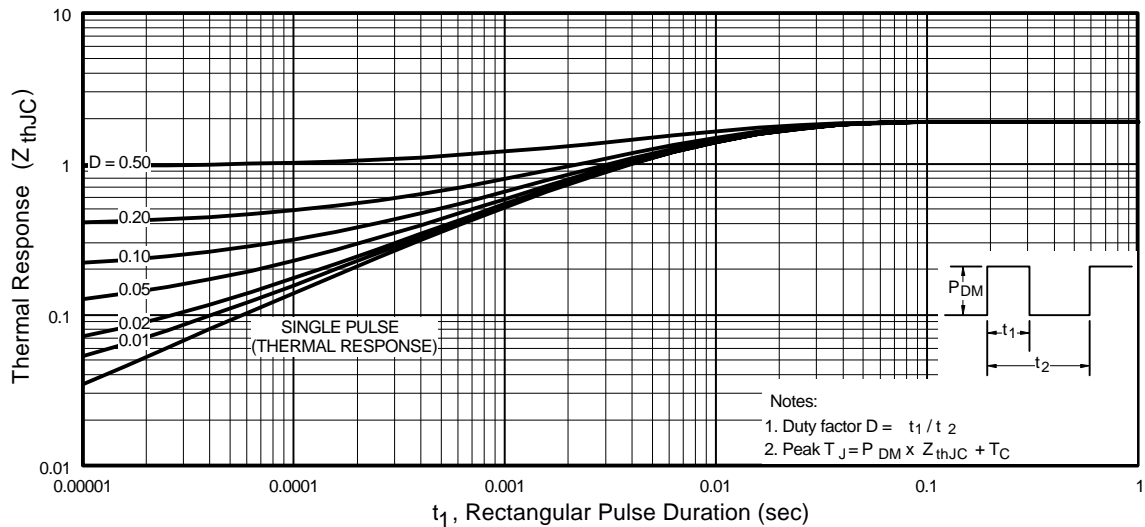
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

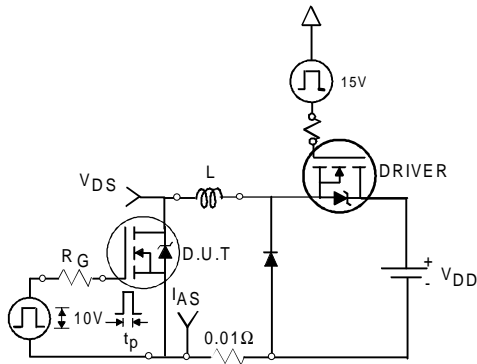


Fig 12a. Unclamped Inductive Test Circuit

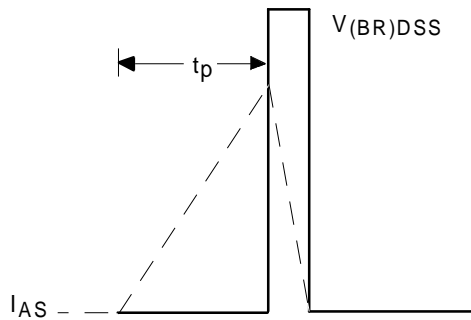


Fig 12b. Unclamped Inductive Waveforms

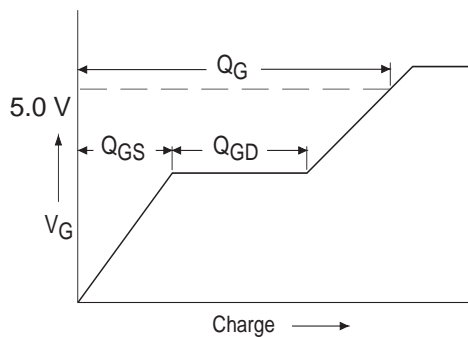


Fig 13a. Basic Gate Charge Waveform

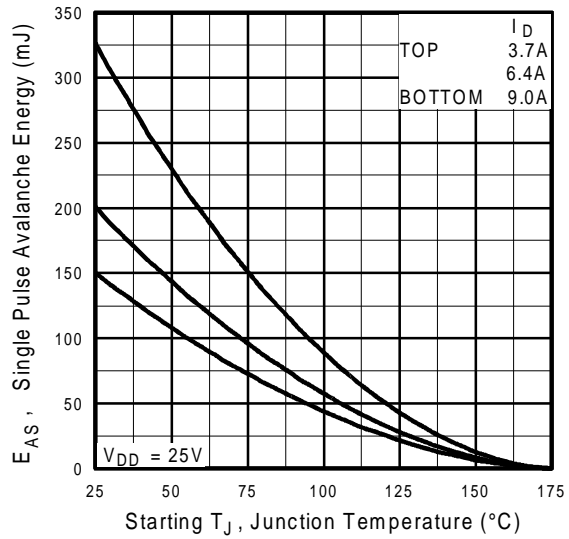


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

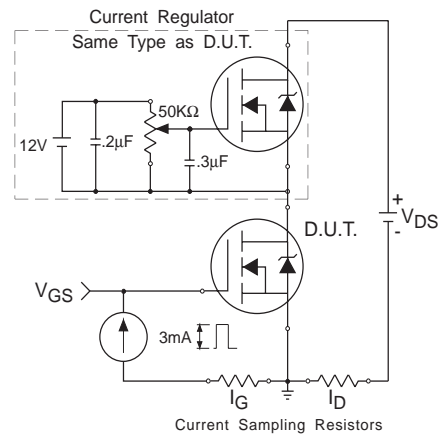
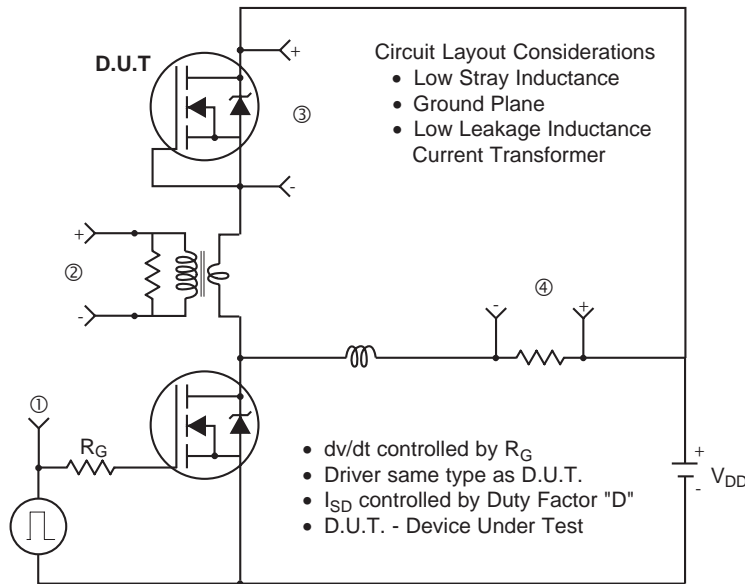


Fig 13b. Gate Charge Test Circuit

### Peak Diode Recovery dv/dt Test Circuit



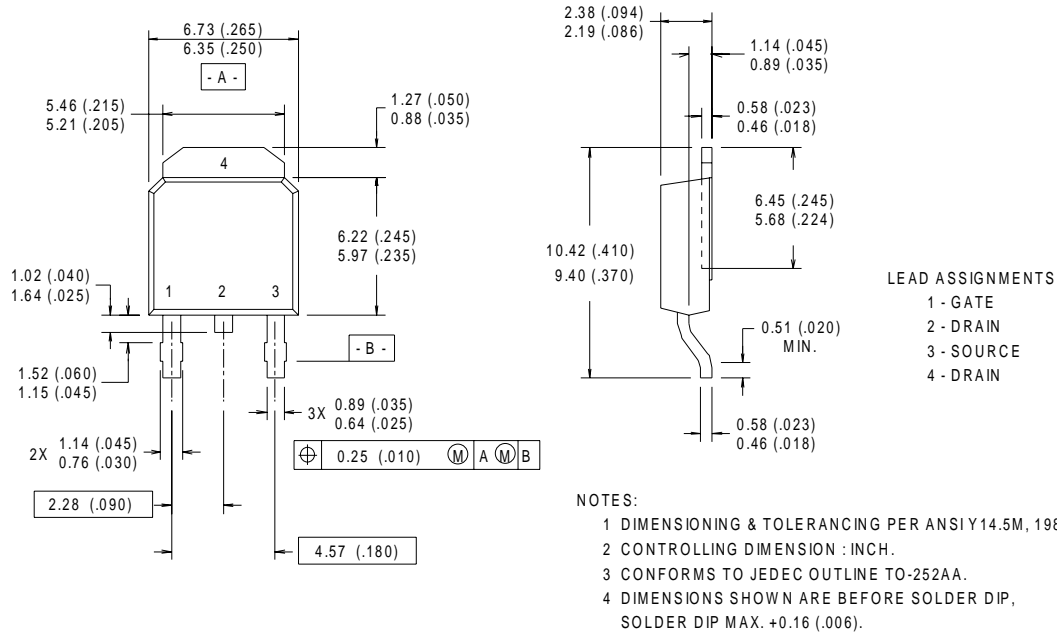
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

**Package Outline**

**TO-252AA Outline**

Dimensions are shown in millimeters (inches)



**Part Marking Information**

**TO-252AA (D-PARK)**

EXAMPLE : THIS IS AN IRFR120  
 WITH ASSEMBLY  
 LOT CODE 9U1P





## Package Outline

### TO-251AA Outline

Dimensions are shown in millimeters (inches)



#### LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

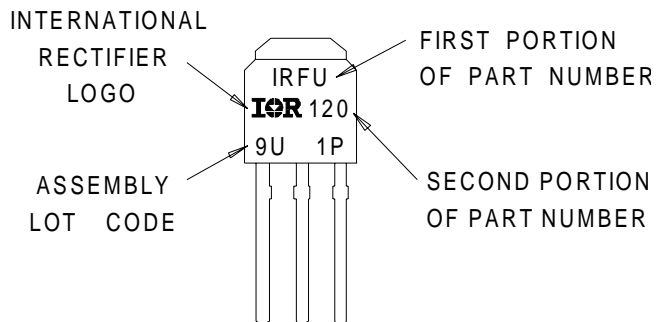
#### NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSII Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 CONFORMS TO JEDEC OUTLINE TO-252AA.
- 4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

## Part Marking Information

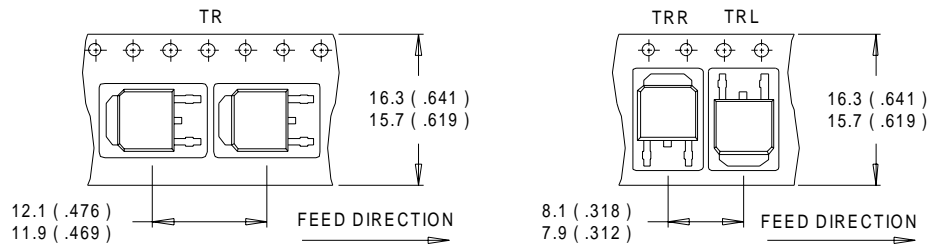
### TO-251AA (I-PARK)

EXAMPLE : THIS IS AN IRFU120  
 WITH ASSEMBLY  
 LOT CODE 9U1P

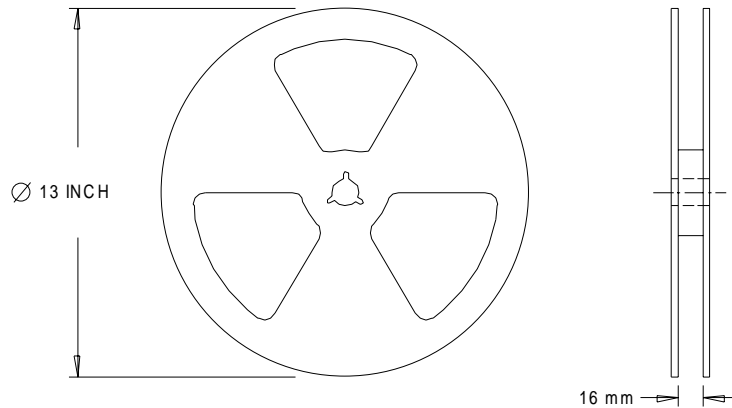


**Tape & Reel Information**

**TO-252AA**



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

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