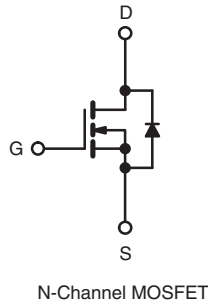
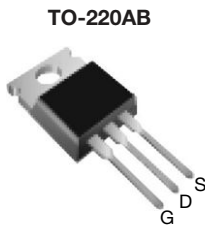


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.28
Q_g (Max.) (nC)	130	
Q_{gs} (nC)	33	
Q_{gd} (nC)	59	
Configuration	Single	



FEATURES

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low t_{rr} and Soft Diode Recovery
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- ZVS and High Frequency Circuit
- PWM Inverters

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFB17N50LPbF
	SiHFB17N50L-E3
SnPb	IRFB17N50L
	SiHFB17N50L


ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	V_{DS}		500	V	
Gate-Source Voltage	V_{GS}		± 30		
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	16	A	
		$T_C = 100\text{ }^\circ\text{C}$	11		
Pulsed Drain Current ^a	I_{DM}		64		
Linear Derating Factor			1.8	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy ^b	E_{AS}		390	mJ	
Repetitive Avalanche Current ^a	I_{AR}		16	A	
Repetitive Avalanche Energy ^a	E_{AR}		22	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		P_D	220	W
Peak Diode Recovery dV/dt ^c	dV/dt		13	V/ns	
Operating Junction and Storage Temperature Range	T_J, T_{stg}		- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d		
Mounting Torque	6-32 or M3 screw		10	lbf · in	
			1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 3.0\text{ mH}$, $R_g = 25\text{ }^\circ\Omega$, $I_{AS} = 16\text{ A}$ (see fig. 12).
- $I_{SD} \leq 16\text{ A}$, $dI/dt \leq 347\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.56	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.6	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$		-	-	50	μA
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	2.0	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 9.9\text{ A}^b$	-	0.28	0.32	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 9.9\text{ A}^b$		11	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5		-	2760	-	pF
Output Capacitance	C_{oss}			-	325	-	
Reverse Transfer Capacitance	C_{rss}			-	37	-	
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	3690	-	pF
		$V_{GS} = 0\text{ V}$	$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	84	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	159	-	pF
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 16\text{ A}, V_{DS} = 400\text{ V},$ see fig. 6 and 13 ^b	-	-	130	nC
Gate-Source Charge	Q_{gs}			-	-	33	
Gate-Drain Charge	Q_{gd}			-	-	59	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 16\text{ A},$ $R_g = 7.5\text{ }\Omega,$ see fig. 10 ^b		-	21	-	ns
Rise Time	t_r			-	51	-	
Turn-Off Delay Time	$t_{d(off)}$			-	50	-	
Fall Time	t_f			-	28	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	16	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	64	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 16\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$	$I_F = 16\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	170	250	ns
		$T_J = 125\text{ }^\circ\text{C}$		-	220	330	
Body Diode Reverse Recovery Charge	Q_{rr}	$T_J = 25\text{ }^\circ\text{C}$		-	470	710	nC
		$T_J = 125\text{ }^\circ\text{C}$		-	810	1210	
Reverse Recovery Current	I_{RRM}			-	7.3	11	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

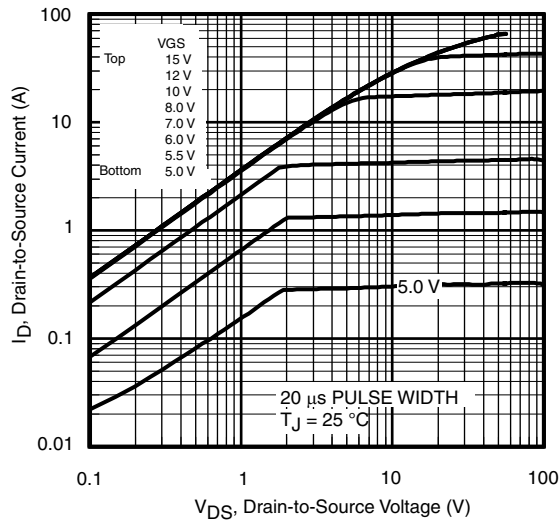


Fig. 1 - Typical Output Characteristics

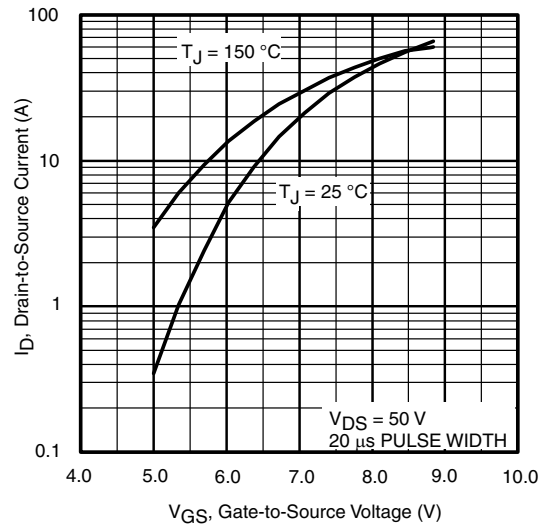


Fig. 3 - Typical Transfer Characteristics

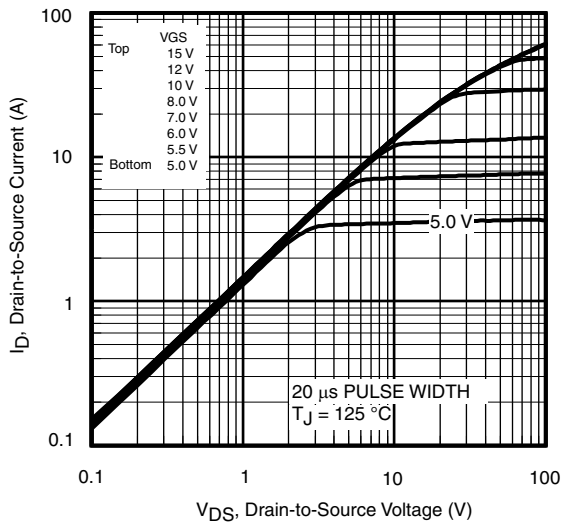


Fig. 2 - Typical Output Characteristics

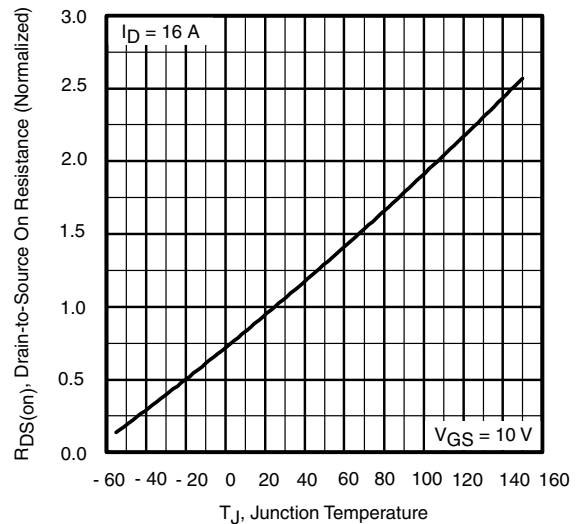


Fig. 4 - Normalized On-Resistance vs. Temperature

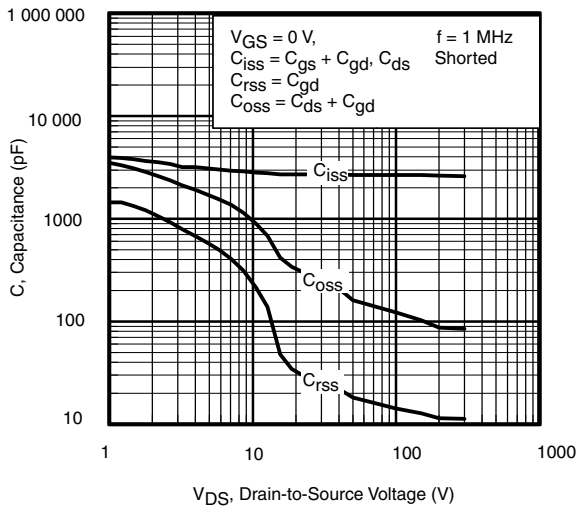


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

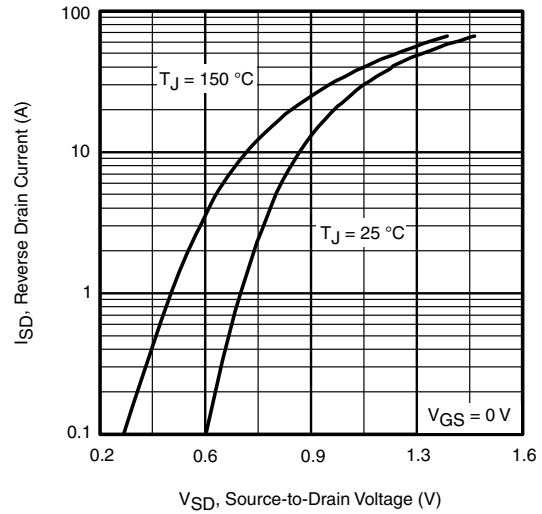


Fig. 7 - Typical Source-Drain Diode Forward Voltage

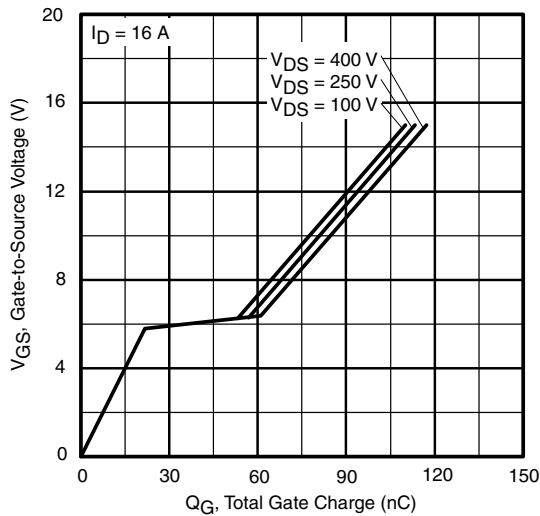


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

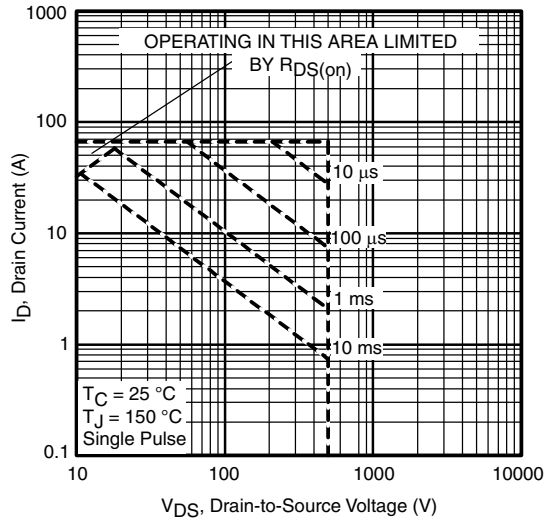


Fig. 8 - Maximum Safe Operating Area

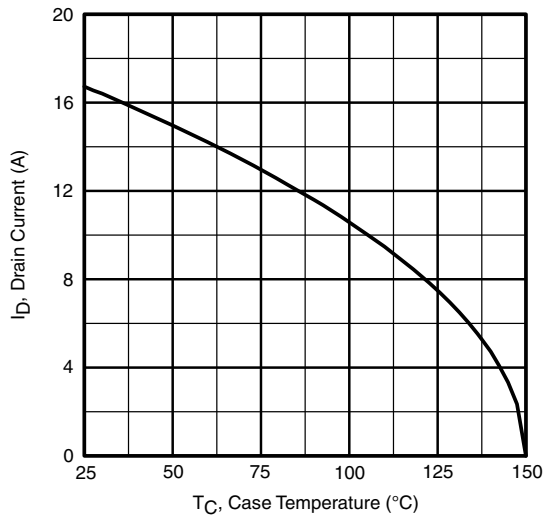


Fig. 9 - Maximum Drain Current vs. Case Temperature

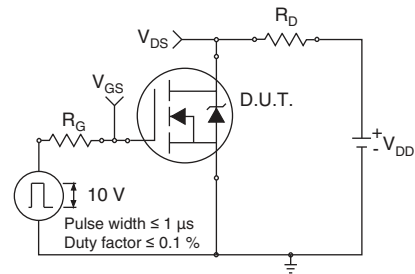


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

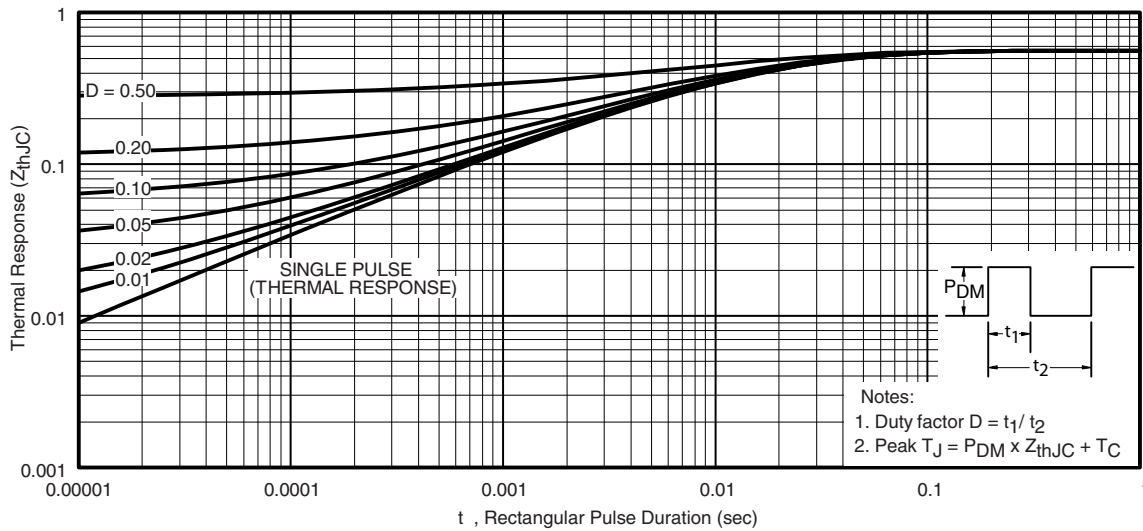


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

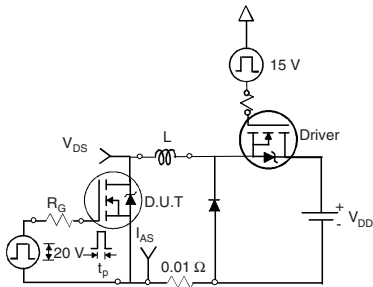


Fig. 12a - Unclamped Inductive Test Circuit

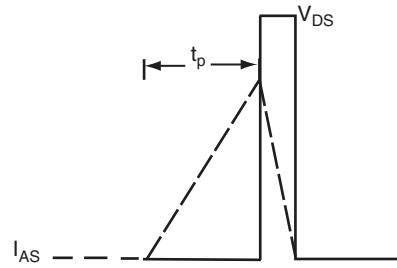


Fig. 12b - Unclamped Inductive Waveforms

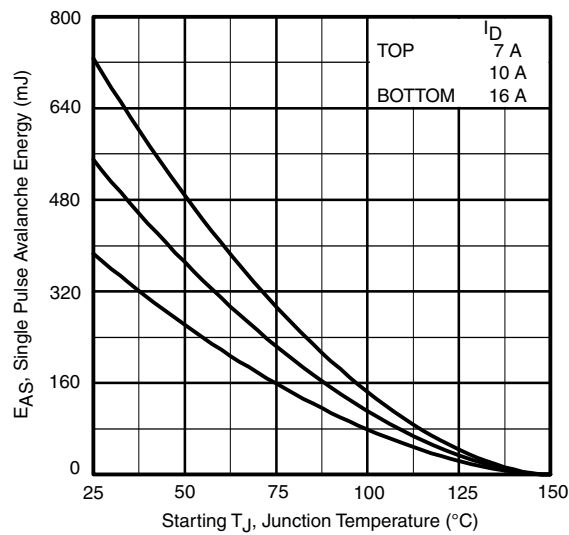


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

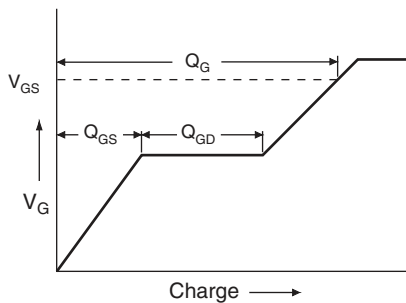


Fig. 13a - Basic Gate Charge Waveform

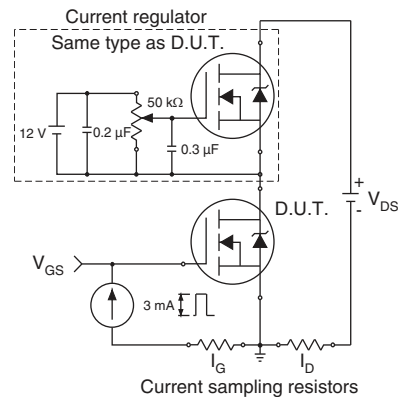


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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