

PI3WVR626

2:1 MIPI 2-Data Lane Switch

## Features

- 3-lane, 2:1 switches that support D-PHY and C-PHY
- Data rate support: up to 2.5Gbps C-PHY, up to 3Gb/s D-PHY.
- Bandwidth: 4.5 GHz Typical
- Low Crosstalk: -35 dB@1.25 GHz
- Input Signals 0 to 1.3V
- $R_{ON}$ : 5.0 $\Omega$  Typical LP & HS MIPI
- $\Delta R_{ON}$ : 0.2 $\Omega$  Typical LP & HS MIPI
- $R_{ON\_FLAT}$ : 0.1 $\Omega$  Typical LP & HS MIPI
- $I_{CC}$ : 11 $\mu$ A Typical
- Skew of Opposite Transitions of the Same Output: 5ps Typical
- $V_{DD}$  Operating Range: 1.5V to 3.6V
- ESD Tolerance: 2kV HBM
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.  
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green):
  - 24-Pin, X1QFN (2.5mm x 2.5mm) (XEB)

## Description

Diodes' PI3WVR626 is a two-data-lane MIPI switch. This 6 channel single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed (HS) or low-power (LP) MIPI signal. The PI3WVR626 is designed for the MIPI specification and allows connection to CSI/DSI, C-PHY/D-PHY module.

## Applications

- Cellular Phones, Smart Phone
- Tablets
- Laptops
- Displays

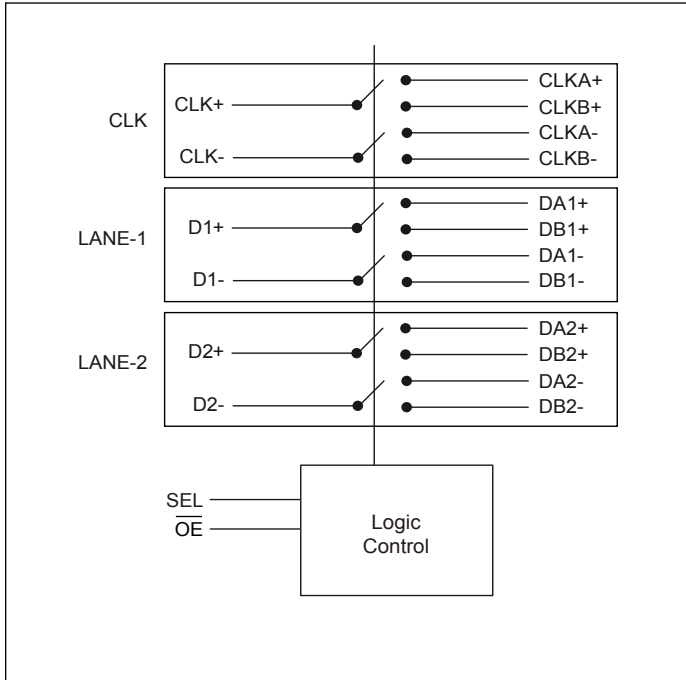
### Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

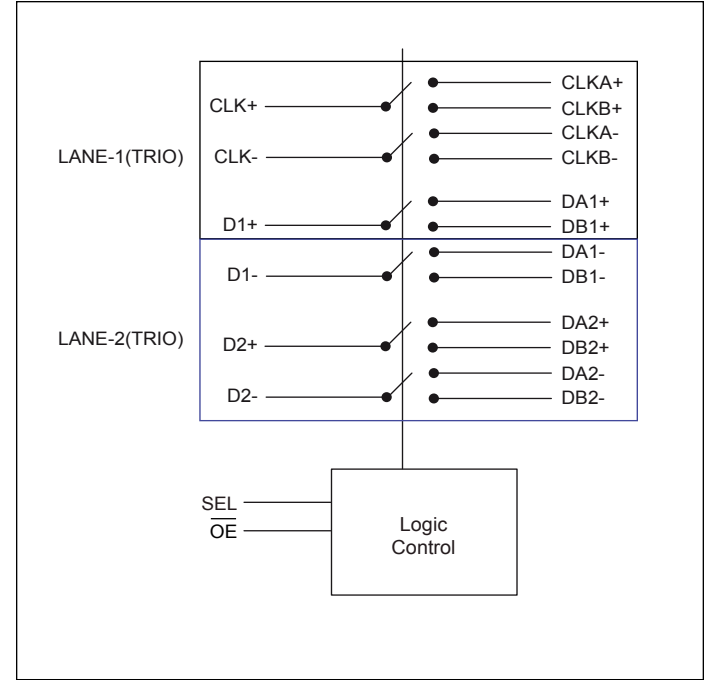
**PI3WVR626**

**Block Diagram**

PI3WVR626 D-PHY Application

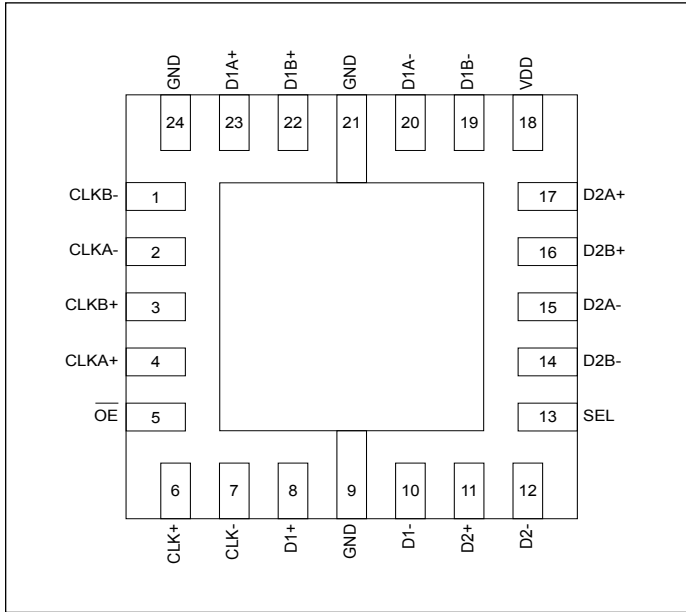


PI3WVR626 C-PHY Application

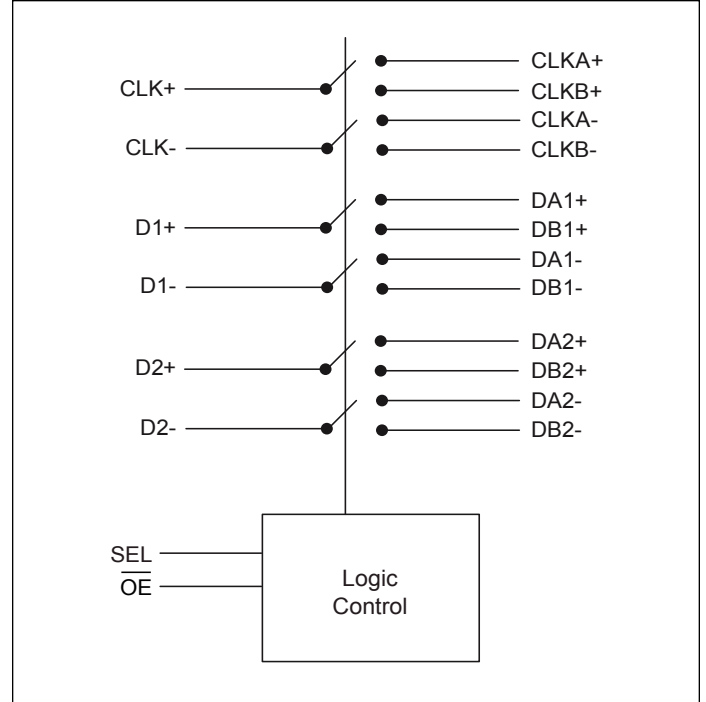


**PI3WVR626**

**Pin Configuration(Top View)**



**Block Diagram**



**Truth Table**

| SEL  | $\overline{\text{OE}}$ | Function                                       |
|------|------------------------|--|
| LOW  | LOW                    | CLK+ = CLKA+, CLK- = CLKA-, Dn(+/-) = DAn(+/-) |
| HIGH | LOW                    | CLK+ = CLKB+, CLK- = CLKB-, Dn(+/-) = DBn(+/-) |
| X    | HIGH                   | Clock and Data Ports High Impedance            |

## Pin Description

| Pin#      | Pin Name               | Signal Type | Description   |
|-----------|------------------------|-------------|---|
| 18        | V <sub>DD</sub>        | Power       | 1.5V to 3.3V power supply   |
| 9, 21, 24 | GND                    | Ground      | Ground  |
| 5         | $\overline{\text{OE}}$ | I           | Output enable. if OE is low, IC is enabled. if OE is high, IC is power down and all I/Os are Hi-Z |
| 13        | SEL                    | I           | Switch logic control  |
| 14        | D2B-                   | I/O         | Negative differential signal 2 for port B   |
| 16        | D2B+                   | I/O         | Positive differential signal 2 for port B   |
| 15        | D2A-                   | I/O         | Negative differential signal 2 for port A   |
| 17        | D2A+                   | I/O         | Positive differential signal 2 for port A   |
| 12        | D2-                    | I/O         | Negative differential signal 2 for COM port   |
| 11        | D2+                    | I/O         | Positive differential signal 2 for COM port   |
| 19        | D1B-                   | I/O         | Negative differential signal 1 for port B   |
| 22        | D1B+                   | I/O         | Positive differential signal 1 for port B   |
| 20        | D1A-                   | I/O         | Negative differential signal 1 for port A   |
| 23        | D1A+                   | I/O         | Positive differential signal 1 for port A   |
| 10        | D1-                    | I/O         | Negative differential signal 1 for COM port   |
| 8         | D1+                    | I/O         | Positive differential signal 1 for COM port   |
| 1         | CLKB-                  | I/O         | Clock negative differential signal for port B   |
| 3         | CLKB+                  | I/O         | Clock positive differential signal for port B   |
| 2         | CLKA-                  | I/O         | Clock negative differential signal for port A   |
| 4         | CLKA+                  | I/O         | Clock positive differential signal for port A   |
| 7         | CLK-                   | I/O         | Clock negative differential signal for COM port   |
| 6         | CLK+                   | I/O         | Clock positive differential signal for COM port   |

## Absolute Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

|   |                          |
|---|--------------------------|
| V <sub>CC</sub> , Supply Voltage, .....   | -0.5V to 4.5V            |
| V <sub>CNTRL</sub> , DC Input Voltage ( $\overline{OE}$ , SEL) <sup>(1)</sup> ..... | -0.5V to V <sub>CC</sub> |
| V <sub>SW</sub> , DC Switch I/O Voltage <sup>(1,2)</sup> .....                      | -0.3V to 2.5V            |
| I <sub>IK</sub> , DC Input Diodes Current .....                                     | -50mA                    |
| I <sub>OUT</sub> , DC Output Current .....  | 25mA                     |
| T <sub>STG</sub> , Storage Temperature .....  | -65°C to +150°C          |
| T <sub>j</sub> , Junction Temperature.....  | 125°C                    |
| ESD:  |                          |
| Human Body Model, JEDEC: JESD22-A114, All Pins.....                                 | 2.0kV                    |
| Charged Device Model, JEDEC: JESD22-C101.....                                       | 1.0kV                    |

### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. V<sub>SW</sub> refers to analog data switch paths.

## Recommended Operating Conditions

The Recommended operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

| Symbol             | Description  | Test Conditions | Min. | Max.            | Units |
|--------------------|--|-----------------|------|-----------------|-------|
| V <sub>CC</sub>    | Supply Voltage   |                 | 1.5  | 3.6             | V     |
| V <sub>CNTRL</sub> | Control Input Voltage (SEL, $\overline{OE}$ ) <sup>(1)</sup> |                 | 0    | V <sub>CC</sub> | V     |
| V <sub>SW</sub>    | Switch I/O Voltage (CLK-, D-, CLKA-, CLKB-, DA-, DB-)        | - HS Mode       | 0    | 0.5             | V     |
|                    |  | - LP Mode       | 0    | 1.3             | V     |
| T <sub>A</sub>     | Operating Temperature  |                 | -40  | +85             | °C    |

### Note:

1. The control inputs must be held HIGH or LOW; they must not float.

## DC and Transient Characteristics

All typical values are at T<sub>A</sub> = 25°C unless otherwise specified.

| Symbol                                       | Description   | Test Conditions                           | V <sub>CC</sub> (V) | T <sub>A</sub> = -40°C to +85°C |      |      | Units |
|--|---|---|---------------------|---------------------------------|------|------|-------|
|  |   |   |                     | Min.                            | Typ. | Max. |       |
| V <sub>IK</sub>                              | Clamp Diode Voltage ( $\overline{OE}$ , SEL)          | I <sub>IN</sub> = -18mA                   | 1.5                 | -1.2                            |      | -0.6 | V     |
| V <sub>IH</sub>                              | Input Voltage High                                    | SEL, $\overline{OE}$                      | 1.5 to 3.3          | -1.0                            |      |      | V     |
| V <sub>IL</sub>                              | Input Voltage Low                                     | SEL, $\overline{OE}$                      | 1.5 to 3.3          |                                 |      | 0.5  | V     |
| I <sub>IN</sub>                              | Control Input Leakage ( $\overline{OE}$ , SEL)        | V <sub>CNTRL</sub> = 0 to V <sub>CC</sub> | 3.3                 | -1.0                            |      | 1.0  | μA    |
| I <sub>NO(OFF)</sub><br>I <sub>NC(OFF)</sub> | Off Leakage Current of Port CLKA-, DA-, CLKB- and DB- | V <sub>SW</sub> = 0.0 ≤ DATA ≤ 1.3V       | 3.3                 | -1.0                            |      | 1.0  | μA    |
| I <sub>A(ON)</sub>                           | On Leakage Current of Common Ports (CLK-, D-)         | V <sub>SW</sub> = 0.0 ≤ DATA ≤ 1.3V       | 3.3                 | -1.0                            |      | 1.0  | μA    |

**DC and Transient Characteristics Cont.**

| Symbol                       | Description   | Test Conditions  | V <sub>CC</sub> (V) | T <sub>A</sub> = -40°C to +85°C |      |      | Units |
|------------------------------|---|--|---------------------|---------------------------------|------|------|-------|
|                              |   |  |                     | Min.                            | Typ. | Max. |       |
| I <sub>OFF</sub>             | Power-Off Leakage Current (All I/O Ports)                                   | V <sub>SW</sub> = 0.0 or 1.3V  | 0                   | -5                              |      | 5.0  | μA    |
| I <sub>OZ</sub>              | Off-State Leakage   | V <sub>SW</sub> = 0.0 ≤ DATA ≤ 1.3V,<br>OE = High  | 3.6                 | -5                              |      | 5.0  | μA    |
| R <sub>ON_MIPI_HS</sub>      | Switch On Resistance for HS MIPI  | I <sub>ON</sub> = -8mA, OE = 0V,<br>SEL = V <sub>CC</sub> or 0V, CLKA,<br>CLKB, DB- or DA- = 0.2V      | 1.5                 |                                 | 5    |      | Ω     |
|                              |   |  | 2.5                 |                                 |      |      |       |
|                              |   |  | 3.3                 |                                 |      |      |       |
| R <sub>ON_MIPI_LP</sub>      | Switch On Resistance for LP MIPI  | I <sub>ON</sub> = -8mA, OE = 0V,<br>SEL = V <sub>CC</sub> or 0V, CLKA,<br>CLKB, DB- or DA- = 1.2V      | 1.5                 |                                 | 5    |      | Ω     |
|                              |   |  | 2.5                 |                                 |      |      |       |
|                              |   |  | 3.3                 |                                 |      |      |       |
| ΔR <sub>ON_MIPI_HS</sub>     | On Resistance Matching Between HS MIPI Channels <sup>(1)</sup>              | I <sub>ON</sub> = -8mA, OE = 0V,<br>SEL = V <sub>CC</sub> or 0V, CLKA,<br>CLKB, DB- or DA- = 0.2V      | 1.5                 |                                 | 0.2  |      | Ω     |
|                              |   |  | 2.5                 |                                 |      |      |       |
|                              |   |  | 3.3                 |                                 |      |      |       |
| ΔR <sub>ON_MIPI_LP</sub>     | On Resistance Matching Between LP MIPI Channels <sup>(1)</sup>              | I <sub>ON</sub> = -8mA, OE = 0V,<br>SEL = V <sub>CC</sub> or 0V, CLKA,<br>CLKB, DB- or DA- = 1.2V      | 1.5                 |                                 | 0.2  |      | Ω     |
|                              |   |  | 2.5                 |                                 |      |      |       |
|                              |   |  | 3.3                 |                                 |      |      |       |
| R <sub>ON_FLAT_MIPI_HS</sub> | On Resistance Flatness for HS MIPI  | I <sub>ON</sub> = -8mA, OE = 0V,<br>SEL = V <sub>CC</sub> or 0V, CLKA,<br>CLKB, DB- or DA- = 0 to 0.5V | 1.5                 |                                 | 0.1  |      | Ω     |
|                              |   |  | 2.5                 |                                 |      |      |       |
|                              |   |  | 3.3                 |                                 |      |      |       |
| R <sub>ON_FLAT_MIPI_LP</sub> | On Resistance Flatness for LP MIPI  | I <sub>ON</sub> = -8mA, OE = 0V,<br>SEL = V <sub>CC</sub> or 0V, CLKA,<br>CLKB, DB- or DA- = 0 to 1.3V | 1.5                 |                                 | 0.1  |      | Ω     |
|                              |   |  | 2.5                 |                                 |      |      |       |
|                              |   |  | 3.3                 |                                 |      |      |       |
| I <sub>CC</sub>              | Quiescent Supply Current  | V <sub>SEL</sub> = 0 or V <sub>CC</sub> , I <sub>OUT</sub> = 0,<br>OE = 0V                             | 3.6                 |                                 | 11   | 20   | μA    |
| I <sub>CCZ</sub>             | Quiescent Supply Current (High Impedance)                                   | V <sub>SEL</sub> = 0 or V <sub>CC</sub> , I <sub>OUT</sub> = 0,<br>OE = 0V                             | 3.6                 |                                 |      | 1    | μA    |
| I <sub>CCCT</sub>            | Increase in I <sub>CC</sub> Current Per Control Voltage and V <sub>CC</sub> | V <sub>SEL</sub> = 0 or V <sub>CC</sub> , OE = 1.5V  | 3.6                 |                                 | 1    |      | μA    |

## AC Electrical Characteristics

All typical values are for  $V_{CC} = 3.3V$  and  $T_A = 25^\circ C$  unless otherwise specified.

| Symbol     | Description   | Test Conditions  | $V_{CC}$ (V) | $T_A = -40^\circ C$ to $+85^\circ C$ |      |      | Units   |
|------------|---|--|--------------|--------------------------------------|------|------|---------|
|            |   |  |              | Min.                                 | Typ. | Max. |         |
| $t_{INIT}$ | Initialization Time $V_{CC}$ to Output <sup>(1)</sup> | $R_L = 50\Omega, C_L = 0pF, V_{SW} = 0.6V$                         | 1.5 to 3.6   |                                      | 60   |      | $\mu s$ |
| $t_{EN}$   | Enable Time $\overline{OE}$ to Output                 | $R_L = 50\Omega, C_L = 0pF, V_{SW} = 0.6V$                         | 1.5 to 3.6   |                                      | 60   | 150  | $\mu s$ |
| $t_{DIS}$  | Disable Time $\overline{OE}$ to Output                | $R_L = 50\Omega, C_L = 0pF, V_{SW} = 0.6V$                         | 1.5 to 3.6   |                                      | 35   | 250  | ns      |
| $t_{ON}$   | Turn-On Time SEL to Output                            | $R_L = 50\Omega, C_L = 0pF, V_{SW} = 0.6V$                         | 1.5 to 3.6   |                                      | 350  | 1100 | ns      |
| $t_{OFF}$  | Turn-Off Time SEL to Output                           | $R_L = 50\Omega, C_L = 0pF, V_{SW} = 0.6V$                         | 1.5 to 3.6   |                                      | 125  | 800  | ns      |
| $t_{BBM}$  | Break-Before-Make Time                                | $R_L = 50\Omega, C_L = 0pF, V_{SW} = 0.6V$                         | 1.5 to 3.6   |                                      |      | 450  | ns      |
| $t_{PD}$   | Propagation Delay <sup>(1)</sup>                      | $C_L = 0pF, R_L = 50\Omega$  | 1.5 to 3.6   |                                      |      | 0.25 | ns      |
| $O_{IRR}$  | Off Isolation for MIPI <sup>(1)</sup>                 | $R_L = 50\Omega, f = 1250MHz, \overline{OE} = HIGH, V_{SW} = 0.5V$ | 1.5 to 3.6   |                                      | -28  |      | dB      |
| $X_{TALK}$ | Crosstalk for MIPI <sup>(1)</sup>                     | $R_L = 50\Omega, f = 1250MHz, SEL = HIGH, V_{SW} = 0.5V$           | 1.5 to 3.6   |                                      | -35  |      | dB      |
| $I_{LOSS}$ | Insertion Loss <sup>(1)</sup>                         | $R_L = 50\Omega, C_L = 0pF, f = 1250MHz, V_{SW} = 0.5V$            | 1.5 to 3.6   |                                      | -0.7 |      | dB      |
| BW         | -3db Bandwidth <sup>(1)</sup>                         | $R_L = 50\Omega, C_L = 0pF, V_{SW} = 0.5V$                         | 1.5 to 3.6   | 4                                    | 4.5  |      | GHz     |

**Note:**

1. Guaranteed by characterization.

**PI3WVR626**

### High-Speed-Related AC Electrical Characteristics

| Symbol             | Description  | Test Conditions  | V <sub>CC</sub> (V) | T <sub>A</sub> = -40°C to +85°C |      |      | Units |
|--------------------|--|--|---------------------|---------------------------------|------|------|-------|
|                    |  |  |                     | Min.                            | Typ. | Max. |       |
| t <sub>SK(P)</sub> | D-PHY HS Mode Skew of Opposite Transitions of the Same Output <sup>(1)</sup> | R <sub>L</sub> = 50Ω, C <sub>L</sub> = 0pF, V <sub>SW</sub> = 0.3V | 1.5 to 3.6          |                                 | 4    | 8    | ps    |
|                    | C-PHY HS Mode Skew of 3 channels in same lane                                | R <sub>L</sub> = 50Ω, C <sub>L</sub> = 0pF, V <sub>SW</sub> = 0.5V | 1.5 to 3.6          |                                 | 4    |      |       |
|                    | D-PHY HS Mode Skew of all group A or group B channels <sup>(1)</sup>         | R <sub>L</sub> = 50Ω, C <sub>L</sub> = 0pF, V <sub>SW</sub> = 0.3V | 1.5 to 3.6          |                                 | 6    | 10   |       |

**Note:**

1. Guaranteed by characterization.

### Capacitance

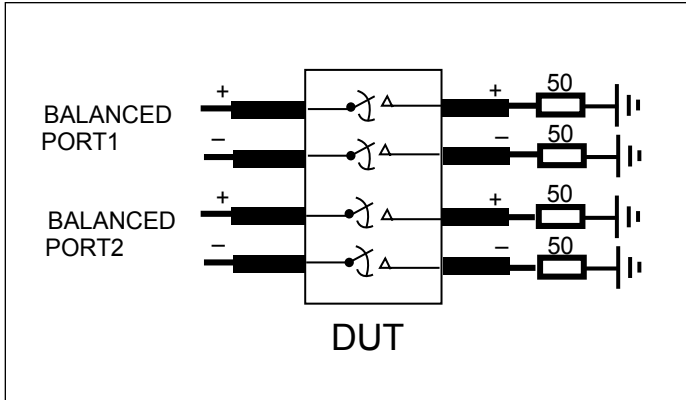
| Symbol           | Description                                  | Test Conditions  | T <sub>A</sub> = -40°C to +85°C |      |      | Units |
|------------------|--|--|---------------------------------|------|------|-------|
|                  |  |  | Min.                            | Typ. | Max. |       |
| C <sub>IN</sub>  | Control Pin Input Capacitance <sup>(1)</sup> | V <sub>CC</sub> = 0V, f = 1MHz   |                                 | 2.1  |      | pF    |
| C <sub>ON</sub>  | On Capacitance <sup>(1)</sup>                | V <sub>CC</sub> = 3.3V, $\overline{OE}$ = 0V, f = 1250MHz (In HS common value)         |                                 | 1.3  |      | pF    |
| C <sub>OFF</sub> | Off Capacitance <sup>(1)</sup>               | V <sub>CC</sub> or $\overline{OE}$ = 3.3V, f = 1250MHz (Both sides in HS common value) |                                 | 0.8  |      | pF    |

**Note:**

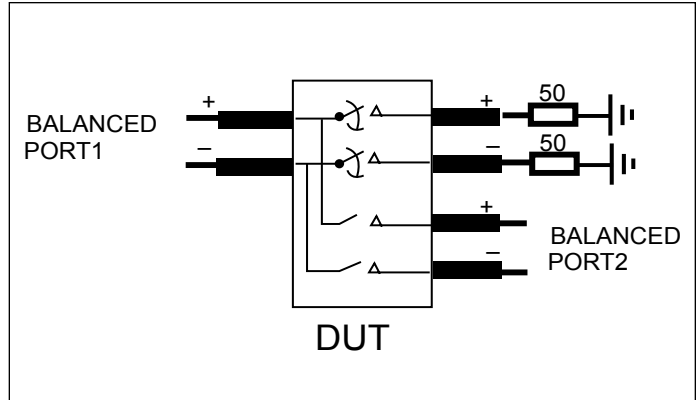
1. Guaranteed by characterization.



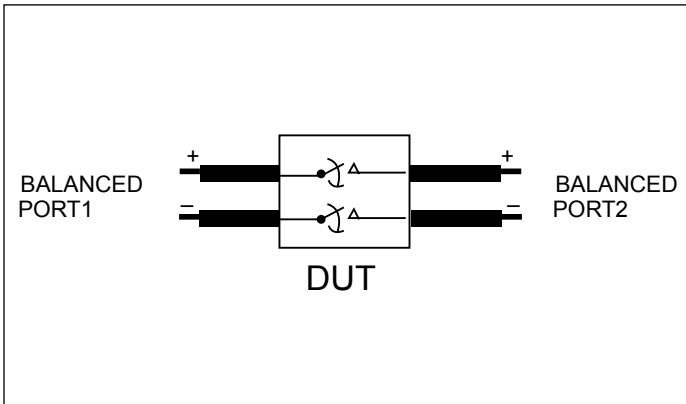
**PI3WVR626**



**Fig 1. Crosstalk Setup**

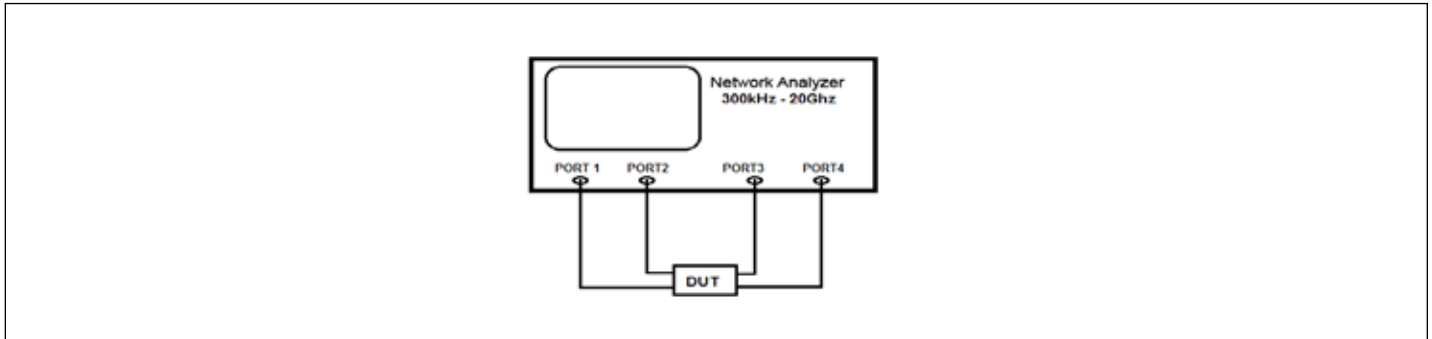


**Fig 2. Off-Isolation Setup**

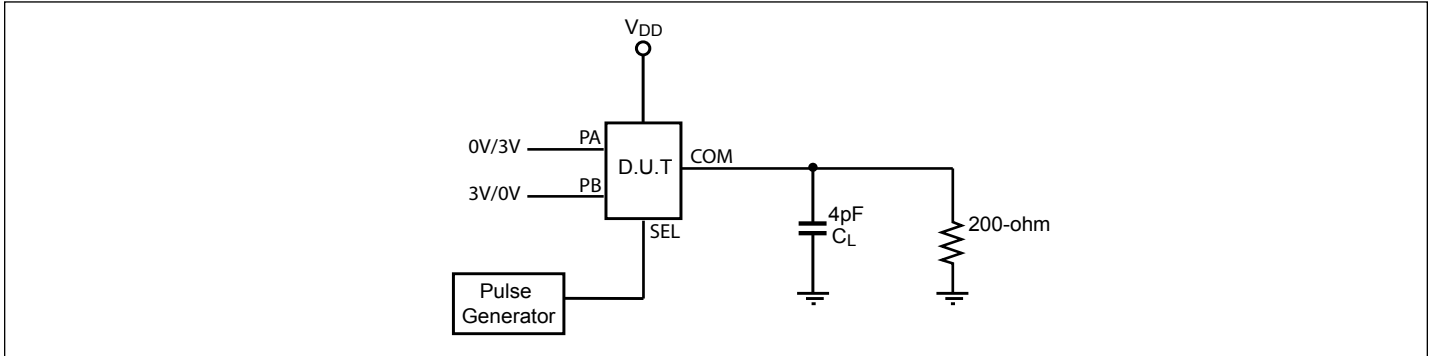


**Fig 3. Differential Insertion Loss**

**Test Circuit for Dynamic Electrical Characteristics**



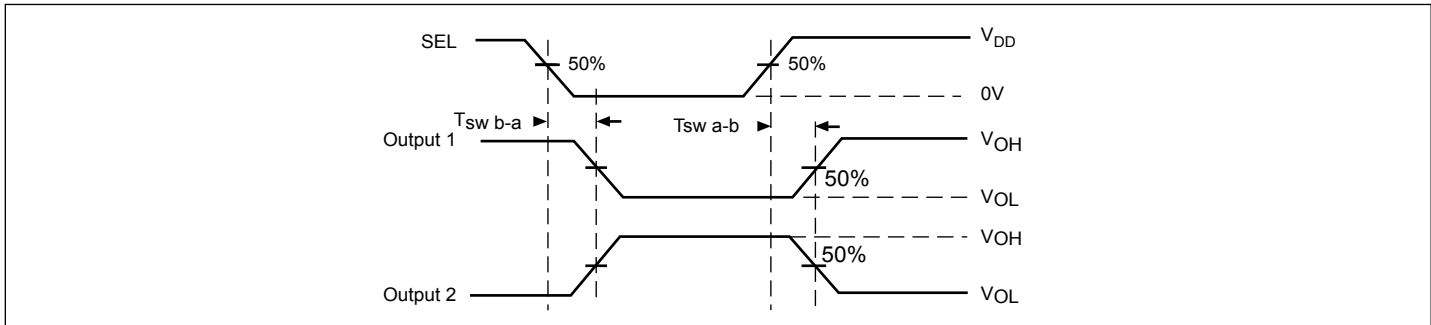
**Test Circuit for Electrical Characteristics<sup>(1-4)</sup>**



**Notes:**

1.  $C_L$  = Load capacitance: includes jig and probe capacitance.
2.  $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator
3. All input impulses are supplied by generators having the following characteristics:  $PRR \leq \text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_R \leq 2.5\text{ns}$ ,  $t_F \leq 2.5\text{ns}$ .
4. The outputs are measured one at a time with one transition per measurement.

**Switching Waveforms**



**Voltage Waveforms for Select Timing**

**Test Condition**

| Output 1 Test Condition | Output 2 Test Condition |
|-------------------------|-------------------------|
| PA = Low                | PA = High               |
| PB = High               | PB = Low                |

**Part Marking**

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

**PI3WVR626**

**Packaging Mechanical:**

24-X1QFN (XEB)

| SYMBOLS | MIN.       | NOM. | MAX. |
|---------|------------|------|------|
| A       | 0.40       | 0.45 | 0.50 |
| A1      | 0.00       | 0.02 | 0.05 |
| A3      | 0.127 REF. |      |      |
| b       | 0.12       | 0.17 | 0.22 |
| b1      | 0.07       | 0.12 | 0.17 |
| D       | 2.50 BSC   |      |      |
| E       | 2.50 BSC   |      |      |
| e       | 0.35 BSC   |      |      |
| L       | 0.20       | 0.25 | 0.30 |
| K       | 0.20       | —    | —    |
| D2      | 1.35       | 1.40 | 1.45 |
| E2      | 1.35       | 1.40 | 1.45 |

**NOTE :**

- ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
- COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
- REFER JEDEC MO-288
- RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
- THERMAL PAD SOLDERING AREA

**DIODES PERICOM** & PRODUCT LINE OF DIODES INCORPORATED  
ENABLING SERIAL CONNECTIVITY

**DESCRIPTION:** 24-Contact, Extra Thin Fine Pitch QFN, X1QFN  
**PACKAGE CODE:** XEB (XEB24)  
**DOCUMENT CONTROL #:** PD-2243

DATE: 06/26/19  
 REVISION: —

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

| Ordering Code  | Package Code | Package Description                           |
|----------------|--------------|---|
| PI3WVR626XEBEX | XEB          | 24-Contact, Extra Thin Fine Pitch (X1QFN) QFN |

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- E = Pb-free and Green
- X suffix = Tape/Reel

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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