



PIC16(L)F19155/56/75/76/85/86

PIC16(L)F19155/56/75/76/85/86 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F19155/56/75/76/85/86 family devices that you have received conform functionally to the current Device Data Sheet (DS40001923A), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the PIC16(L)F19155/56/75/76/85/86 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (A1).

Data Sheet clarifications and corrections start on [page 5](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select *Programmer > Reconnect*.
 - b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F19155/56/75/76/85/86 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾
		A1
PIC16F19155	3096h	2001h
PIC16LF19155	3097h	2001h
PIC16F19156	3098h	2001h
PIC16LF19156	3099h	2001h
PIC16F19175	309Ah	2001h
PIC16LF19175	309Bh	2001h
PIC16F19176	309Ch	2001h
PIC16LF19176	309Dh	2001h
PIC16F19185	30BAh	2001h
PIC16LF19185	30BBh	2001h
PIC16F19186	30BCh	2001h
PIC16LF19186	30BDh	2001h

- Note 1:** The Device and Revision IDs is located at the respective addresses 8006h and 8005h of configuration memory space.
- 2:** Refer to the "PIC16(L)F191XX Memory Programming Specification" (DS40001880) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Summary	Affected Revisions
				A1
Analog-to-Digital Converter with Computation (ADC ²)	ADC ² with Fixed Voltage Reference (FVR)	1.1	Using the FVR as the ADC positive voltage reference can cause missing codes.	X
	ADC ² with Guard Ring Outputs	1.2	The Guard Ring Output feature is not implemented.	X
Reset and VBAT	VBAT with ULPBOR	2.1	Higher current with ULPBOR active.	X
Liquid Crystal Display (LCD) Controller	Internal VLCD3 Measurement	3.1	Non stable readings.	X
Comparator (CMP)	C2 Low-Power Clocked Comparator	4.1	Unstable output.	X
Electrical Specifications	SMBus V _{IL} Level	5.1	The maximum V _{IL} level changes when V _{DD} is below 4.0V.	X
	Program Flash Memory (PFM) Endurance	5.2	The PFM endurance is lower than specified.	X
	Fixed Voltage Reference (FVR) Accuracy	5.3	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A1).

1. Module: Analog-to-Digital Converter with Computation (ADC²)

1.1 ADC² with Fixed Voltage Reference (FVR)

Using the FVR as the positive voltage reference (VREF+) for the ADC, can cause an increase in missing codes.

Work around

Method 1: Increase the bit conversion time, known as TAD, to 8 µs or higher.

Method 2: Use VDD as the positive voltage reference to the ADC.

Affected Silicon Revisions

A1								
X								

1.2 ADC² with Guard Ring Outputs

The two guard ring drive outputs ADGRDA and ADGRDB are not implemented on these devices.

Work around

None.

Affected Silicon Revisions

A1								
X								

2. Module: Reset and VBAT

2.1 VBAT with ULPBOR

In order to avoid high IBAT currents of 10 µA or greater, when utilizing VBAT to provide battery back-up the ULPBOR should not be activated. When the part is used in this fashion, VDD should also be either off (0 volts) or >1.5V.

Work around

Do not use VBAT along with ULPBOR.

Affected Silicon Revisions

A1								
X								

3. Module: Liquid Crystal Display (LCD) Controller

3.1 Internal VLCD3 Measurement

The ¼ scale tap point provided on the LP Resistor Ladder for use together with the ADC does not provide stable readings to support monitoring of the LCD pump output level.

Work around

Measure the VLCD3 via an external ADC.

Affected Silicon Revisions

A1								
X								

4. Module: Comparator (CMP)

4.1 C2 Low-Power Clocked Comparator

The output of the Low-Power Clocked Comparator (CMP2) is unstable and is not recommended for use.

Work around

None.

Affected Silicon Revisions

A1								
X								

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5. Module: Electrical Specifications

5.1 SMBus VIL Level

When the VDD voltage level supplied to the device is 4.0V and above, the maximum SMBus voltage level for the VIL parameter is 0.8V. When VDD drops below 4.0V, the maximum SMBus voltage level for VIL drops to 0.7V.

Work around

None.

Affected Silicon Revisions

A1							
X							

5.2 Program Flash Memory Endurance

The minimum value for the Program Flash Memory (PFM) endurance specification, called out as parameter number MEM30 in the data sheet, is 1K cycles.

Work around

None.

Affected Silicon Revisions

A1							
X							

5.3 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001923A):

<p>Note: Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.</p>

None.

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APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (06/2017)

Initial release of this document; issued for revision A1. Includes silicon issues 1.1 (ADC²), 2.1 (VBAT), 3.1 (LCD), 4.1 (CMP), Electrical Specifications: 5.1 SMBus, 5.2 Program Flash Memory, and 5.3 FVR.

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