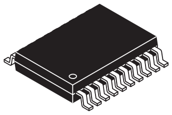


# 24-BIT, 192-kHz SAMPLING, 6-CHANNEL, ENHANCED MULTILEVEL, DELTA-SIGMA DIGITAL-TO-ANALOG CONVERTER

## FEATURES

- **24-Bit Resolution**
- **Analog Performance:**
  - **Dynamic Range: 103 dB, Typical**
  - **SNR: 103 dB, Typical**
  - **THD+N: 0.004%, Typical**
  - **Full-Scale Output: 3.1 Vp-p, Typical**
- **8× Oversampling Interpolation Filter:**
  - **Stopband Attenuation: –55 dB**
  - **Passband Ripple: ±0.03 dB**
- **Sampling Frequency:**
  - **5 kHz to 200 kHz (Channels 1 and 2)**
  - **5 kHz to 100 kHz (Channels 3, 4, 5, and 6)**
- **Accepts 16- and 24-Bit Audio Data**
- **Data Formats: Standard, I$^2$S, and Left-Justified, TDM**
- **System Clock: 128 $f_S$, 192 $f_S$, 256 $f_S$, 384 $f_S$, 512 $f_S$, or 768 $f_S$**
- **Digital De-Emphasis for 32 kHz, 44.1 kHz, 48 kHz**
- **Power Supply: 5-V Single Supply**
- **20-Lead SSOP Package**

## APPLICATIONS

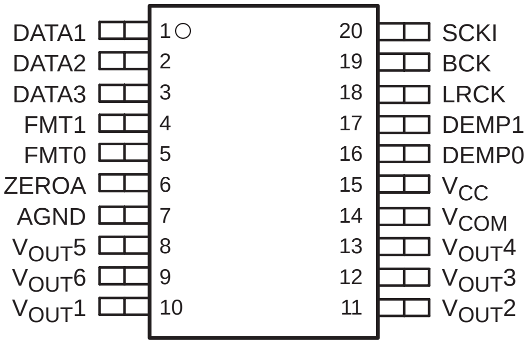
- **Integrated A/V Receivers**
- **DVD Movie and Audio Players**
- **HDTV Receivers**
- **Car Audio Systems**
- **DVD Add-On Cards for High-End PCs**
- **Digital Audio Workstations**
- **Other Multichannel Audio Systems**

## DESCRIPTION

The PCM1606 is a CMOS monolithic integrated circuit that features six 24-bit audio digital-to-analog converters and support circuitry in a small 20-lead SSOP package. The digital-to-analog converters utilize Texas Instruments' enhanced multilevel, delta-sigma architecture, which employs 2nd-order noise shaping and 8-level amplitude quantization to achieve excellent signal-to-noise performance and a high tolerance to clock jitter.

The PCM1606 accepts industry-standard audio data formats with 16- to 24-bit audio data. Sampling rates up to 200 kHz are supported.

**PCM1606**
**(TOP VIEW)**

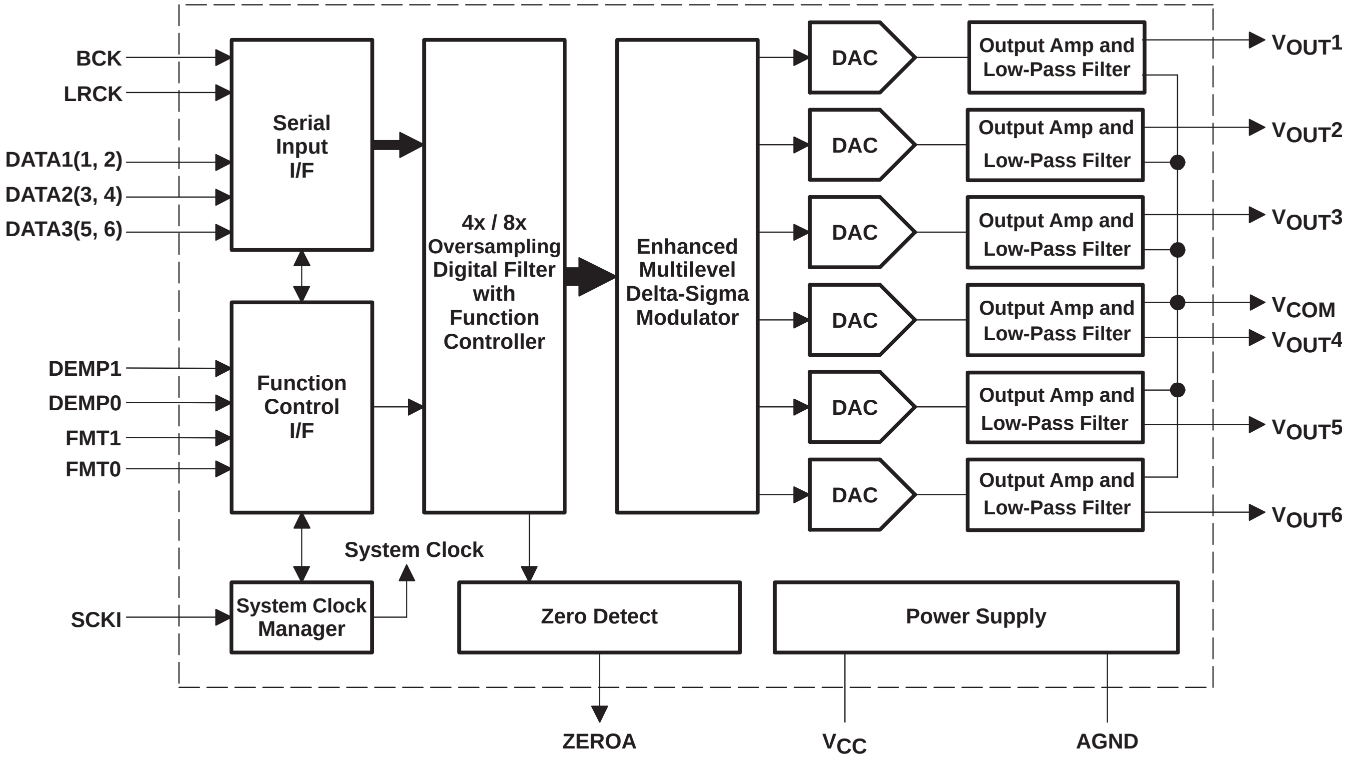


**PACKAGE/ORDERING INFORMATION**

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER | OPERATION TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[†] | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| PCM1606E | 20-Lead SSOP | ZZ334-1 | –25°C to 85°C | PCM1606E | PCM1606E | TUBE |
| | | | | | PCM1606E/2K | Tape and Reel |

[†] Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of PCM1606Y/2K gets a single 2000-piece tape and reel.

## functional block diagram



## Terminal Functions

| TERMINAL NAME | TERMINAL PIN | I/O | DESCRIPTIONS |
|---|---|---|---|
| AGND | 7 | — | Analog and digital ground |
| BCK | 19 | I | Shift clock input for serial audio data (see Note 2) |
| DATA1 | 1 | I | Serial audio data input for $V_{OUT}1$ and $V_{OUT}2$ (see Note 2) |
| DATA2 | 2 | I | Serial audio data input for $V_{OUT}3$ and $V_{OUT}4$ (see Note 2) |
| DATA3 | 3 | I | Serial audio data input for $V_{OUT}5$ and $V_{OUT}6$ (see Note 2) |
| DEMP0 | 16 | I | De-emphasis control (see Note 1) |
| DEMP1 | 17 | I | De-emphasis control (see Note 1) |
| FMT1 | 4 | I | Format select (see Note 1) |
| FMT0 | 5 | I | Format select (see Note 1) |
| LRCK | 18 | I | Left and right clock input. This clock is equal to the sampling rate, $f_S$ (see Note 2) |
| SCKI | 20 | I | System clock in. Input frequency is 128 $f_S$, 192 $f_S$, 256 $f_S$, 384 $f_S$, 512 $f_S$ or 768 $f_S$ (see Note 2) |
| $V_{CC}$ | 15 | — | Analog and digital power supply, 5 V |
| $V_{COM}$ | 14 | — | Common voltage output. This pin should be bypassed with a 10-µF capacitor to AGND |
| $V_{OUT}1$ | 10 | O | Voltage output for audio signal corresponding to L-channel on DATA1. Up to 192 kHz |
| $V_{OUT}2$ | 11 | O | Voltage output for audio signal corresponding to R-channel on DATA1. Up to 192 kHz |
| $V_{OUT}3$ | 12 | O | Voltage output for audio signal corresponding to L-channel on DATA2. Up to 96 kHz |
| $V_{OUT}4$ | 13 | O | Voltage output for audio signal corresponding to R-channel on DATA2. Up to 96 kHz |
| $V_{OUT}5$ | 8 | O | Voltage output for audio signal corresponding to L-channel on DATA3. Up to 96 kHz |
| $V_{OUT}6$ | 9 | O | Voltage output for audio signal corresponding to R-channel on DATA3. Up to 96 kHz |
| ZEROA | 6 | O | Zero-data flag. Logical AND of ZERO1 through ZERO6 |

NOTES: 1. Schmitt-trigger input with internal pulldown.
2. Schmitt-trigger input.

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|---|---|
| Supply voltage, $V_{CC}$ | 6.5 V |
| Digital input voltage | –0.3 V to $V_{CC}$ + 0.3 V |
| Analog input voltage | –0.3 V to $V_{CC}$ + 0.3 V |
| Input current (except power supply) | ±10 mA |
| Ambient temperature under bias | –40°C to 125°C |
| Storage temperature | –55°C to 150°C |
| Junction temperature | 150°C |
| Lead temperature (soldering, 5s) | 260°C, 5s |
| Package temperature (IR reflow, 10s) | 235°C, 10s |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## electrical characteristics, all specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $f_S$ = 44.1 kHz, system clock = 384 $f_S$ and 24-bit data (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | PCM1606E | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| **RESOLUTION** | | | | | 24 | | Bits |
| **DATA FORMAT** | | | | | | | |
| | Audio data interface format | | | Standard, $I^2S$, Left-Justified, TDM | | | |
| | Audio data bit length | | | 16 or 24 bits, selectable | | | |
| | Audio data format | | | MSB first, 2s complement | | | |
| $f_S$ | Sampling frequency | | $V_{OUT}1$, $V_{OUT}2$ | 5 | | 200 | kHz |
| | | | $V_{OUT}3$, $V_{OUT}4$, $V_{OUT}5$, $V_{OUT}6$ | 5 | | 100 | |
| | System clock frequency | | | 128, 192, 256, 384, 512, 768 $f_S$ | | | |
| **DIGITAL INPUT/OUTPUT** | | | | | | | |
| | Logic family (TTL compatible) | | | | | | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $I_{IH}$ | High-level input current | | $V_{IN} = V_{CC}$ | | 67 | 100 | µA |
| $I_{IL}$ | Low-level input current | | $V_{IN}$ = 0 V | | | −10 | µA |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = −4 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA | | | 1 | V |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| THD+N | Total harmonic distortion plus noise | $V_{OUT}$ = 0 dB | $f_S$ = 44.1 kHz/384 $f_S$ | | 0.004% | 0.01% | |
| | | | $f_S$ = 96 kHz/256 $f_S$ | | 0.005% | | |
| | | | $f_S$ = 192 kHz/128 $f_S$ | | 0.002% | | |
| | | $V_{OUT}$ = −60 dB | $f_S$ = 44.1 kHz/348 $f_S$ | | 1% | | |
| | | | $f_S$ = 96 kHz / 256 $f_S$ | | 1.2% | | |
| | | | $f_S$ = 192 kHz/128 $f_S$ | | 1% | | |
| | Dynamic range | | EIAJ, A-weighted, $f_S$ = 44.1 kHz/384 $f_S$ | 98 | 103 | | dB |
| | | | A-weighted, $f_S$ = 96 kHz/256 $f_S$ | | 99 | | |
| | | | A-weighted, $f_S$ = 192 kHz/128 $f_S$ | | 101 | | |
| | Signal-to-noise ratio | | EIAJ, A-weighted, $f_S$ = 44.1 kHz/384 $f_S$ | 98 | 103 | | dB |
| | | | A-weighted, $f_S$ = 96 kHz/256 $f_S$ | | 100 | | |
| | | | A-weighted, $f_S$ = 192 kHz/128 $f_S$ | | 101 | | |
| | Channel separation | | $f_S$ = 44.1 kHz/384 $f_S$ | 95 | 100 | | dB |
| | | | $f_S$ = 96 kHz/256 $f_S$ | | 95 | | |
| | | | $f_S$ = 192 kHz/128 $f_S$ | | 100 | | |
| | Level linearity error | | $V_{OUT}$ = −90 dB | | ±0.5 | | dB |
| **DC ACCURACY** | | | | | | | |
| | Gain error | | | | ±1 %FSR | | |
| | Gain mismatch, channel-to-channel | | | | ±1.3 %FSR | | |
| | Bipolar zero error | | $V_{OUT}$ = 0.5 $V_{CC}$ at BPZ | | ±30 | | mV |
| **ANALOG OUTPUT** | | | | | | | |
| | Output voltage | | Full scale (−0 dB) | | 62% of $V_{CC}$ | | Vp-p |
| | Center voltage | | | | 50% of $V_{CC}$ | | Vdc |
| | Load impedance | | Ac load | 5 | | | kΩ |

## electrical characteristics, all specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $f_S$ = 44.1 kHz, system clock = 384 $f_S$ and 24-bit data (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS | PCM1606E | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **DIGITAL FILTER PERFORMANCE** | | | | | | |
| **FILTER CHARACTERISTICS** | | | | | | |
| | Passband | ±0.03 dB | | | 0.454 $f_S$ | |
| | | −3 dB | | | 0.487 $f_S$ | |
| | Stopband | | 0.546 $f_S$ | | | |
| | Passband ripple | | | | ±0.03 | dB |
| | Stopband attenuation | Stopband = 0.546 $f_S$ | −50 | | | dB |
| | | Stopband = 0.567 $f_S$ | −55 | | | |
| **ANALOG FILTER PERFORMANCE** | | | | | | |
| | Frequency response | At 20 kHz | | −0.03 | | dB |
| **POWER SUPPLY REQUIREMENTS (see Note 4)** | | | | | | |
| $V_{CC}$ | Voltage range | | 4.5 | 5 | 5.5 | VDC |
| $I_{CC}$ | Supply current | $f_S$ = 44.1 kHz/384 $f_S$ | | 50 | 65 | mA |
| | | $f_S$ = 96 kHz/256 $f_S$ | | 72 | | |
| | | $f_S$ = 192 kHz/128 $f_S$ | | 68 | | |
| | Power dissipation | $f_S$ = 44.1 kHz/384 $f_S$ | | 250 | 358 | mW |
| | | $f_S$ = 96 kHz/256 $f_S$ | | 360 | | |
| | | $f_S$ = 192 kHz/128 $f_S$ | | 340 | | |
| **TEMPERATURE RANGE** | | | | | | |
| | Operation temperature | | −25 | | 85 | °C |
| $\theta_{JA}$ | Thermal resistance | 20-pin SSOP | | 115 | | °C/W |

NOTES: 3. Analog performance specs are tested using System Two Cascade Plus by Audio Precision with 400-Hz HPF, 30-kHz LPF on at RMS with 20-kHz LPF, 400-Hz HPF in calculation.
Shibasoku #725 THD meter, 400 Hz HPF, 30 kHz LPF on, at average mode with 20-kHz bandwidth limiting. The load connected to the analog output is 5 kΩ or larger via capacitance coupling.
4. Condition in 192-kHz operation is channel 3 through channel 6 are disabled.

## timing requirements

### system clock input

The PCM1606 requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCKI (pin 20). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. Texas Instruments’ PLL1700 multiclock generator is an excellent choice for providing the PCM1606 system clock source.

The 192-kHz sampling frequency operation is available on DATA1 for $V_{OUT}1$ and $V_{OUT}2$. When the system clock of 128 $f_S$ or 192 $f_S$ is detected, $V_{OUT}3$, $V_{OUT}4$, $V_{OUT}5$ and $V_{OUT}6$ are automatically forced to the bipolar zero level (= 0.5 $V_{CC}$). Table 1 lists the typical system clock frequency.

## timing requirements (continued)

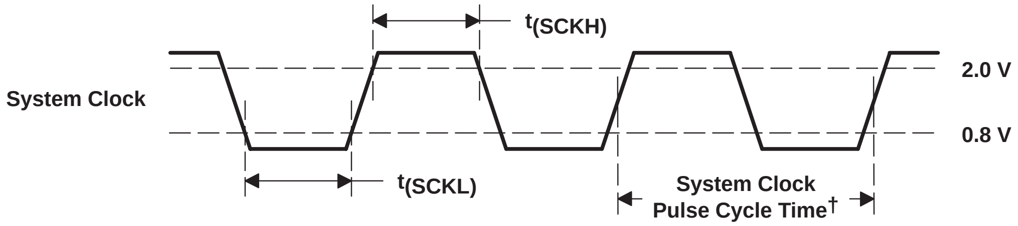
### power-on reset functions

The PCM1606 includes a power-on reset function. Figure 2 shows the operation of this function. With the system clock active and $V_{CC}$ > 3 V typical (2.2 V to 3.7 V), the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time $V_{CC}$ > 3 V. After the initialization period, the PCM1606 is set to its reset default state.

**Table 1. System Clock Rates for Common Audio Sampling Frequencies**

| SAMPLING FREQUENCY | SYSTEM CLOCK FREQUENCY ($f_{SCLK}$) (MHz) | | | | | |
|---|---|---|---|---|---|---|
| | 128 $f_S$ | 192 $f_S$ | 256 $f_S$ | 384 $f_S$ | 512 $f_S$ | 768 $f_S$ |
| 8 kHz | — | — | 2.048 | 3.072 | 4.096 | 6.144 |
| 16 kHz | — | — | 4.096 | 6.144 | 8.192 | 12.288 |
| 32 kHz | — | — | 8.192 | 12.288 | 16.384 | 24.576 |
| 44.1 kHz | — | — | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 48 kHz | — | — | 12.288 | 18.432 | 24.576 | 36.864 |
| 96 kHz | — | — | 24.576 | 36.864 | 49.152 | See Note 5 |
| 192 kHz | 24.576 | 36.864 | See Note 6 | See Note 6 | See Note 6 | See Note 6 |

NOTES: 5. The 768-$f_S$ system clock rate is not supported for $f_S$ > 64 kHz.
6. This system clock is not supported for the given sampling frequency.



† 1/128 $f_S$, 1/256 $f_S$, 1/384 $f_S$, 1/512 $f_S$ and 1/768 $f_S$.

| PARAMETERS | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{(SCKH)}$ | System clock pulse duration HIGH | 10 | | ns |
| $t_{(SCKL)}$ | System clock pulse duration LOW | 10 | | ns |

Figure 1. System Clock Timing

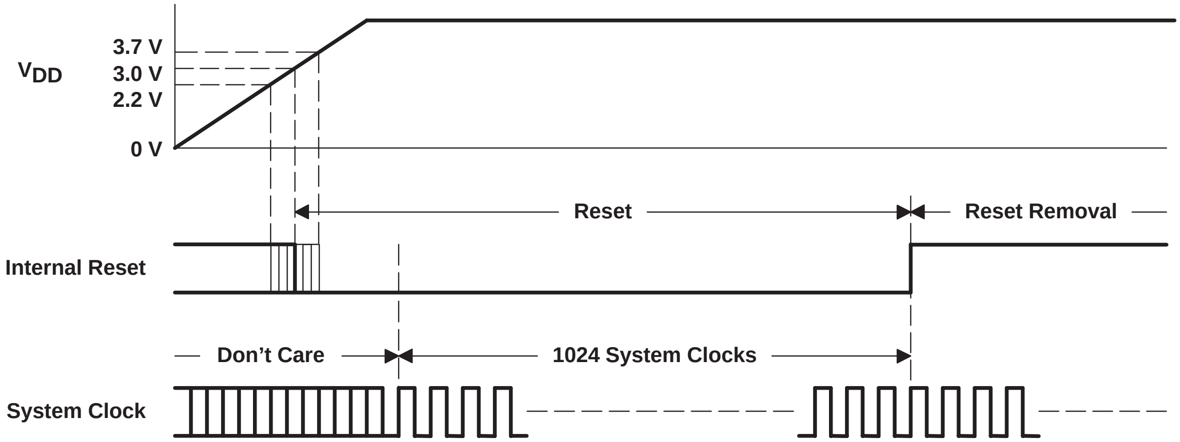


Figure 2. Power-On Reset Timing

## timing requirements (continued)

### audio serial interface

The audio serial interface for the PCM1606 comprises a 5-wire synchronous serial port. It includes LRCK (pin 18), BCK (pin 19), DATA1 (pin 1), DATA2 (pin 2) and DATA3 (pin 3). BCK is the serial audio bit clock and is used to clock the serial data present on DATA1, DATA2, and DATA3 into the audio interface serial shift registers. Serial data is clocked into the PCM1606 on the rising edge of BCK. LRCK is the serial audio left/right word clock. LRCK is used to latch serial data into the serial audio interface internal registers.

Both LRCK and BCK must be synchronous to the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input or output, SCKI. The left/right clock, LRCK, is operated at the sampling frequency ($f_S$). The bit clock, BCK, may be operated at 32, 48, or 64 times the sampling frequency.

### audio data formats and timing

The PCM1606 supports industry-standard audio data formats, including standard, $I^2S$, left-justified, and TDM. The data formats are shown in Figure 6. Data formats are selected using the format pins, FMT1 (pin 4) and FMT0 (pin 5). All formats require binary 2s complement, MSB-first audio data. Figure 3 shows a detailed timing diagram for the serial audio interface, with the exception of TDM format.

DATA1, DATA2, and DATA3 each carry two audio channels, designated as the left and right channels. The left channel data always precedes the right channel data in the serial data stream for all data formats. Table 2 shows the mapping of the digital input data to the analog output pins.

TDM format is able to interface by 3-wire synchronous serial port. All data inputs from DATA1, BCK can be operated at 128, 256, and 512 times the sampling frequency. The rising edge of LRCK means the start of a data frame. Only channel 1 and channel 2 data are acceptable at the 192-kHz sampling frequency ($f_S$); channel 3, channel 4, channel 5, and channel 6 data are don’t care.

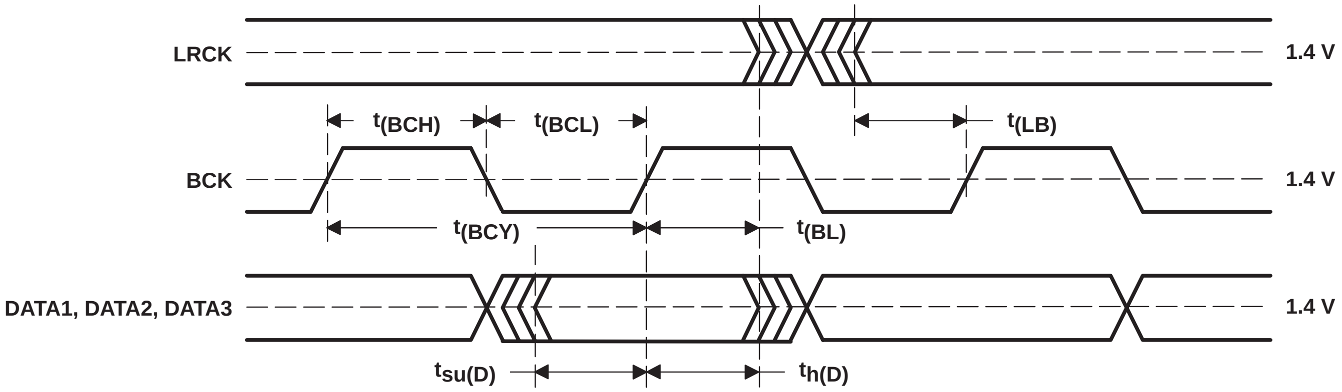
Figure 4 shows the timing requirements for BCK input for TDM format. Figure 5 shows the detailed timing diagram for TDM format.

**Table 2. Audio Input Data to Analog Output Mapping**

| DATA INPUT | CHANNEL | ANALOG OUTPUT |
|---|---|---|
| DATA1 | Left | $V_{OUT}1^{\dagger}$ |
| DATA1 | Right | $V_{OUT}2^{\dagger}$ |
| DATA2 | Left | $V_{OUT}3^{\ddagger}$ |
| DATA2 | Right | $V_{OUT}4^{\ddagger}$ |
| DATA3 | Left | $V_{OUT}5^{\ddagger}$ |
| DATA3 | Right | $V_{OUT}6^{\ddagger}$ |

† Up to 192 kHz
‡ Up to 96 kHz

## timing requirements (continued)



| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{(BCY)}$ | BCK pulse cycle time | 32 $f_S$ / 48 $f_S$ / 64 $f_S$† | | |
| $t_{(BCH)}$ | BCK high-level time | 35 | | ns |
| $t_{(BCL)}$ | BCK low-level time | 35 | | ns |
| $t_{(BL)}$ | BCK rising edge to LRCK edge | 10 | | ns |
| $t_{(LB)}$ | LRCK falling edge to BCK rising edge | 10 | | ns |
| $t_{su(D)}$ | DATA setup time | 10 | | ns |
| $t_{h(D)}$ | DATA hold time | 10 | | ns |

† $f_S$ is the sampling frequency (e.g., 44.1 kHz, 48 kHz, 96 kHz, etc.)

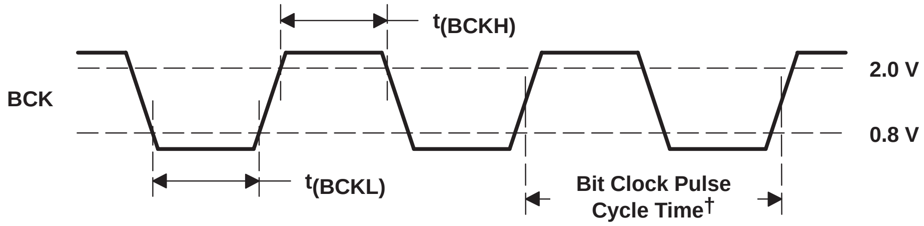
**Figure 3. Audio Interface Timing**

**Table 3. Bit Clock Rates for TDM Format Sampling Frequencies**

| SAMPLING FREQUENCY | SYSTEM CLOCK FREQUENCY ($f_{SCKI}$) (MHz) | | |
|---|---|---|---|
| | 128 $f_S$ | 256 $f_S$ | 512 $f_S$ |
| 8 kHz | — | 2.048 | 4.096 |
| 16 kHz | — | 4.096 | 8.192 |
| 32 kHz | — | 8.192 | 16.384 |
| 44.1 kHz | — | 11.2896 | 22.5792 |
| 48 kHz | — | 12.288 | 24.576 |
| 96 kHz | — | 24.576 | 49.152 |
| 192 kHz | 24.576 | See Note 7 | See Note 7 |

NOTE 7: This bit clock is not supported for the given sampling frequency.

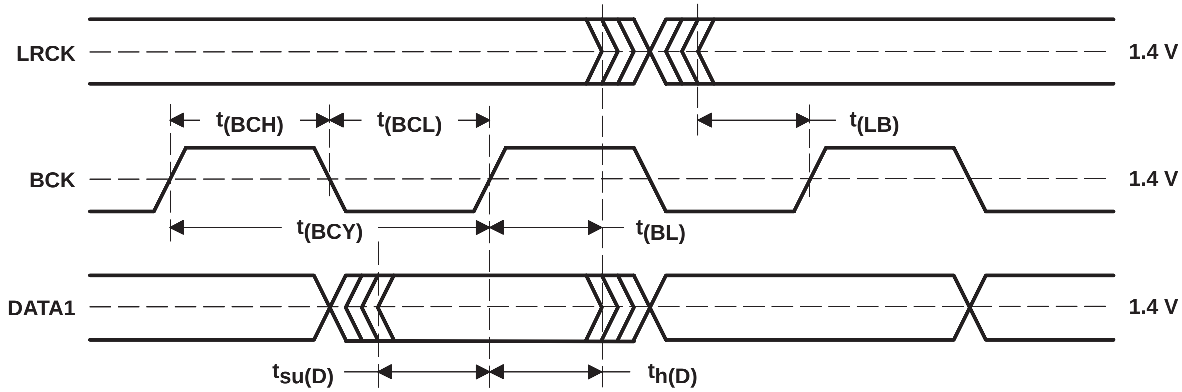
## timing requirements (continued)



| PARAMETERS | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{(BCKH)}$ | Bit clock pulse duration HIGH | 10 | | ns |
| $t_{(BCKL)}$ | Bit clock pulse duration LOW | 10 | | ns |

† 1/128 $f_S$, 1/256 $f_S$, and 1/512 $f_S$.

Figure 4. Bit Clock Timing for TDM Format

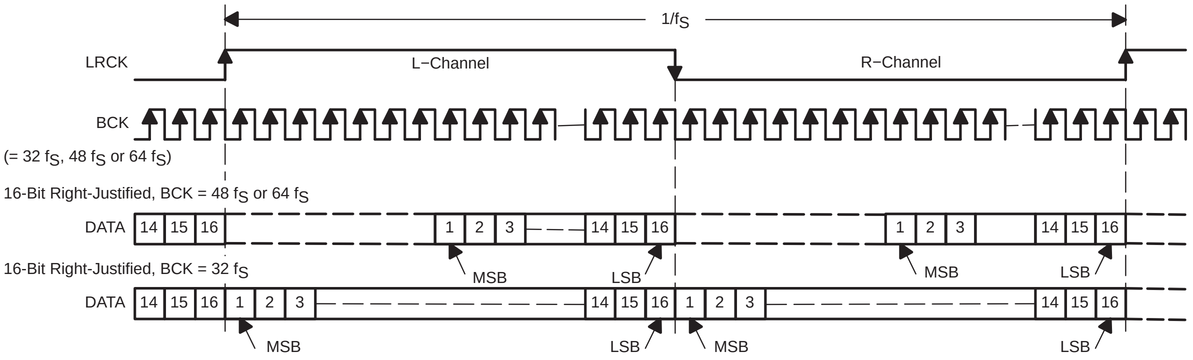


| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{(BCY)}$ | BCK pulse cycle time | 20 | | ns |
| $t_{(BCH)}$ | BCK high-level time | 10 | | ns |
| $t_{(BCL)}$ | BCK low-level time | 10 | | ns |
| $t_{(BL)}$ | BCK rising edge to LRCK edge | 7 | | ns |
| $t_{(LB)}$ | LRCK falling edge to BCK rising edge | 7 | | ns |
| $t_{su(D)}$ | DATA setup time | 7 | | ns |
| $t_{h(D)}$ | DATA hold time | 7 | | ns |

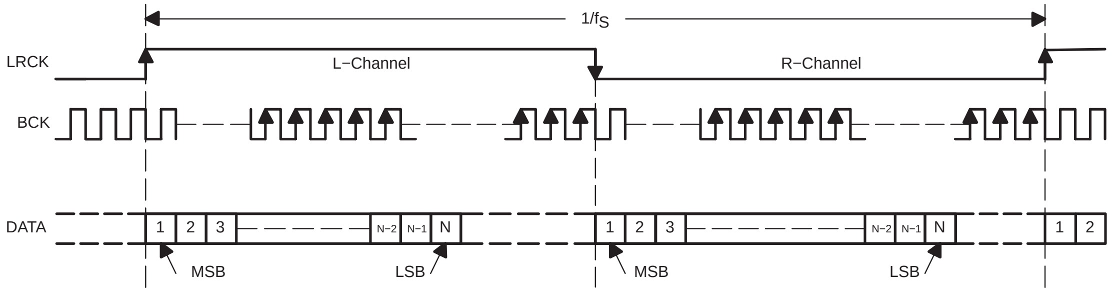
Figure 5. Audio Interface Timing for TDM Format

## timing requirements (continued)

### (1) Standard Data Format; L-Channel = HIGH, R-Channel = LOW



### (2) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



### (3) I$^2$S Data Format; L-Channel = LOW, R-Channel = HIGH

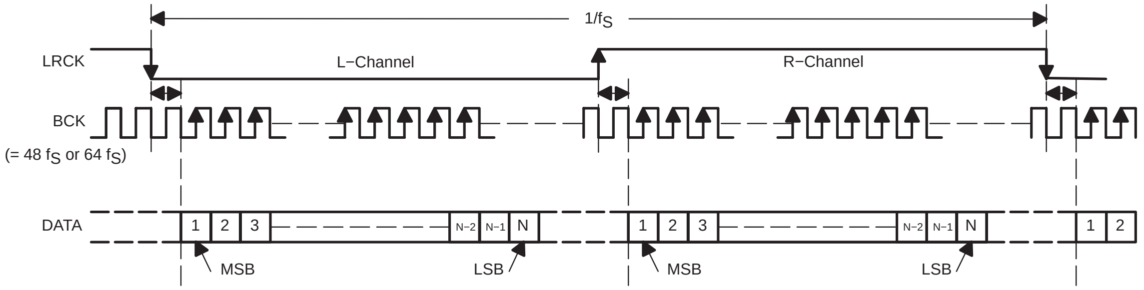


**Figure 6. Audio Data Input Format**

## timing requirements (continued)

### (4) TDM Data Format

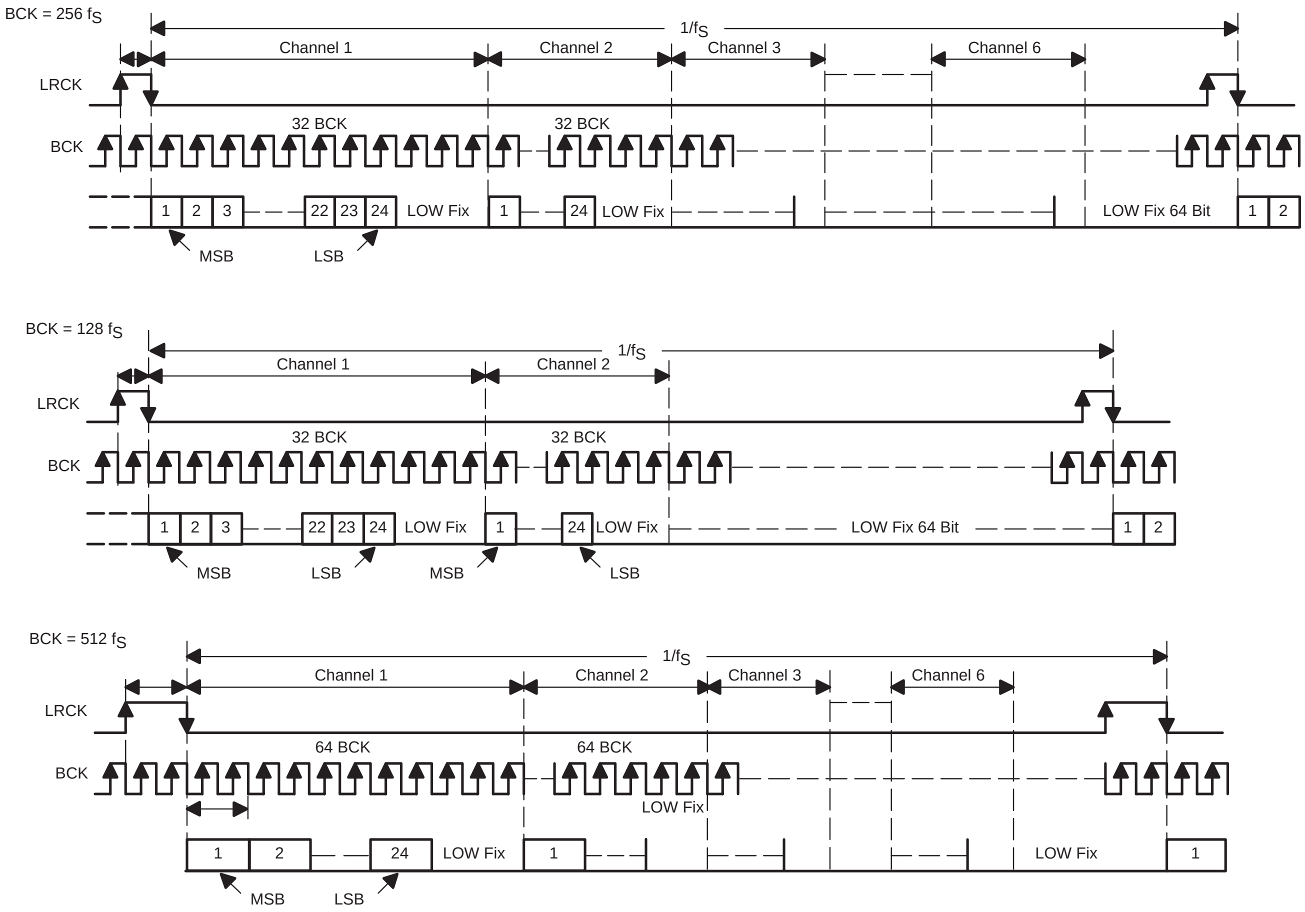


Figure 6. Audio Data Input Format (Continued)

## functional description

The PCM1606 has several built-in functions including digital input data format selection and digital de-emphasis. These functions are hardware controlled with static control signals and used on pin FMT1 (pin 4), pin FMT0 (pin 5), pin DEMP1 (pin 17), and DEMP0 (pin 16).

### data format selection

The PCM audio data format can be selected by pin FMT1 (pin 4) and FMT0 (pin 5) as shown in Table 4.

**Table 4. Data Format Control**

| FMT1 (pin 4) | FMT0 (pin 5) | AUDIO INTERFACE |
|---|---|---|
| LOW | LOW | $I^2S$ |
| LOW | HIGH | TDM |
| HIGH | LOW | Standard |
| HIGH | HIGH | Left-justified |

## functional description (continued)

### de-emphasis control

The de-emphasis control can be selected by DEMP1 (pin 17) and DEMP0 (pin 16). See Table 5.

**Table 5. De-Emphasis Control**

| DEMT1 (pin 17) | DEMT0 (pin 16) | AUDIO INTERFACE |
|---|---|---|
| LOW | LOW | OFF |
| LOW | HIGH | 48 kHz |
| HIGH | LOW | 44.1 kHz |
| HIGH | HIGH | 32 kHz |

### analog outputs

The PCM1606 includes six independent output channels, $V_{OUT}1$ through $V_{OUT}6$. These are unbalanced outputs, each capable of driving 3.1 Vp-p typical into a 5-kΩ ac load with $V_{CC} = 5$ V. The internal output amplifiers for $V_{OUT}1$ through $V_{OUT}6$ are dc-biased to the common-mode (or bipolar zero) voltage, equal to $V_{CC}/2$.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the PCM1606's delta-sigma D/A converters. The frequency response of this filter is shown in Figure 7. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the *Application Information* section of this data sheet.

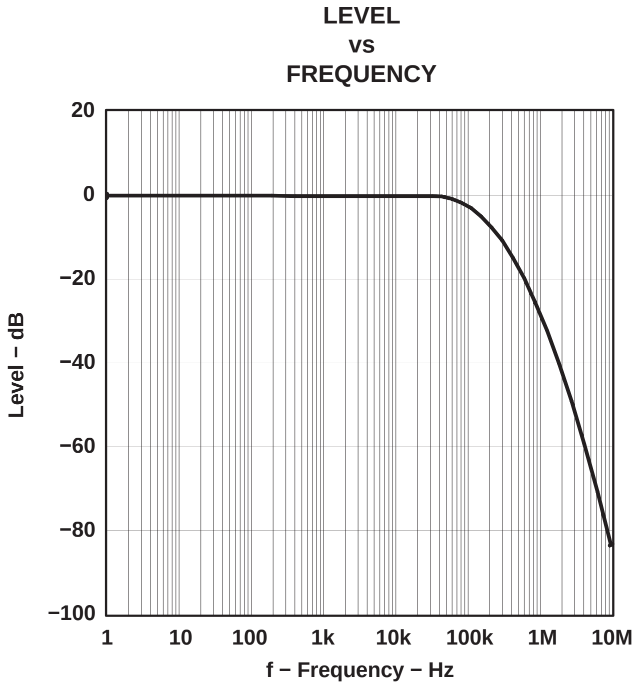


Figure 7. Output Filter Frequency Response

## functional description (continued)

### $V_{COM}$ output

One unbuffered common-mode voltage output pin, $V_{COM}$ (pin 14) is brought out for decoupling purposes. This pin is nominally biased to a dc voltage level equal to $V_{CC}/2$. If this pin is to be used to bias external circuitry, a voltage follower is required for buffering purposes. Figure 8 shows an example of using the $V_{COM}$ pin for external biasing applications.

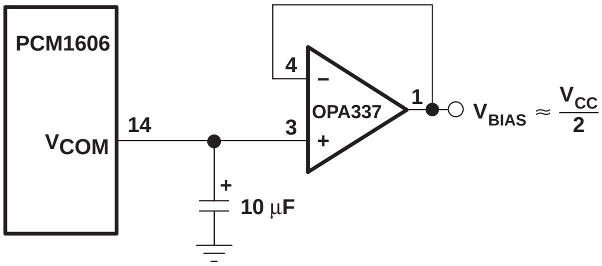


**Figure 8. Biasing External Circuits Using the $V_{COM}$ Pin**

## zero flag

### zero detect condition

Zero detection for each output channel is independent from the others. If the data for a given channel remains at a 0 level for 1024 sample periods (or LRCK clock periods), a zero detect condition exists for that channel.

### zero output flag

When the data for all channels remains at a 0 level for 1024 sample periods (or LRCK clock periods), the ZEROA (pin 6) is set to a logic 1 state. The zero flag pin can be used to operate external mute circuits, or used as a status indicator for a microcontroller, audio signal processor, or other digitally controlled functions.

## TYPICAL CHARACTERISTICS—DIGITAL FILTER

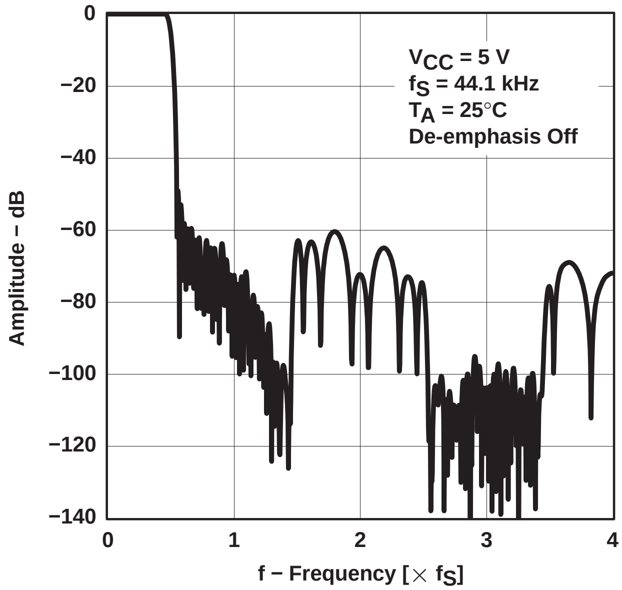

AMPLITUDE
vs
FREQUENCY

Figure 9

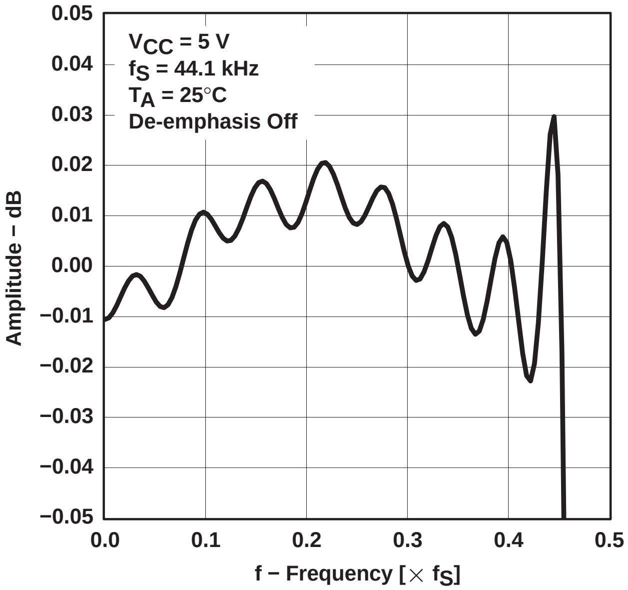

AMPLITUDE
vs
FREQUENCY

Figure 10

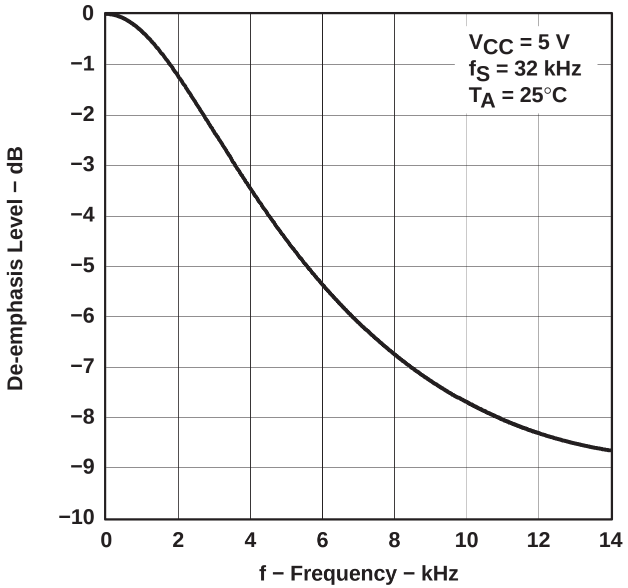

DE-EMPHASIS LEVEL
vs
FREQUENCY

Figure 11

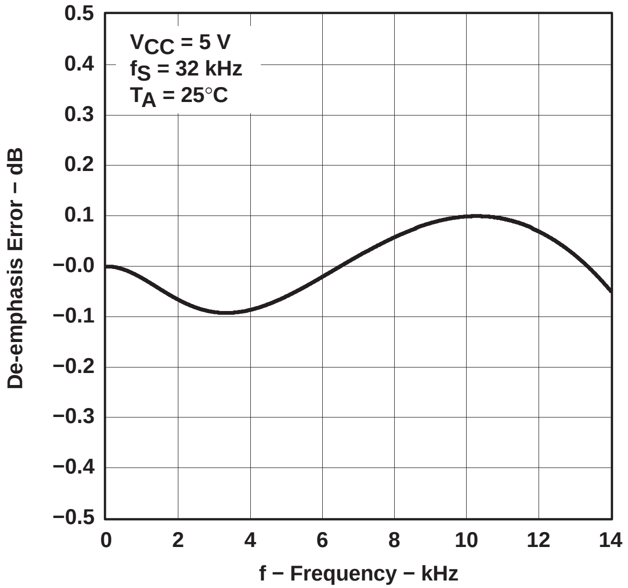

DE-EMPHASIS ERROR
vs
FREQUENCY

Figure 12

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $f_S$ = 44.1 kHz, system clock = 384 $f_S$ and 24-bit data, unless otherwise noted.

## TYPICAL CHARACTERISTICS—DIGITAL FILTER

**DE-EMPHASIS LEVEL**
**vs**
**FREQUENCY**

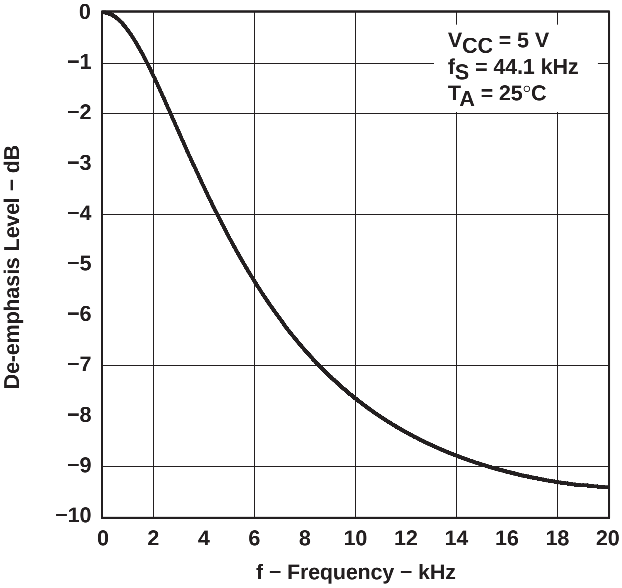


**Figure 13**

**DE-EMPHASIS ERROR**
**vs**
**FREQUENCY**

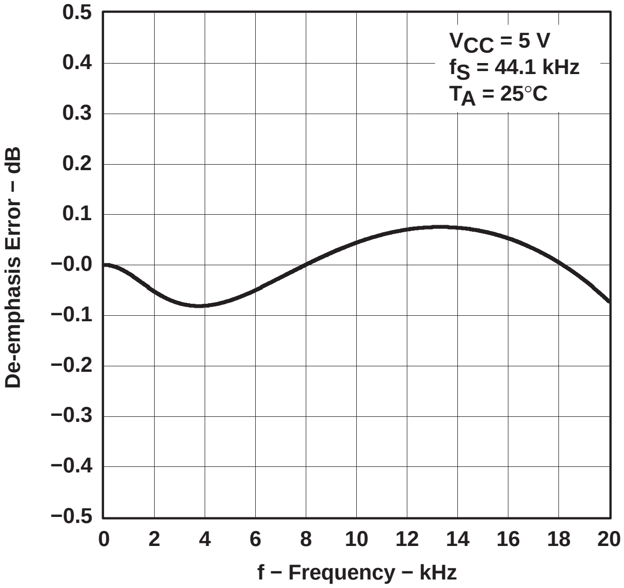


**Figure 14**

**DE-EMPHASIS LEVEL**
**vs**
**FREQUENCY**

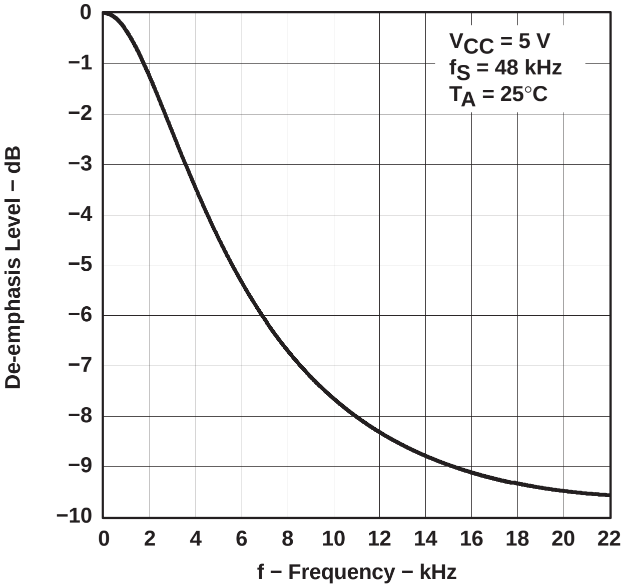


**Figure 15**

**DE-EMPHASIS ERROR**
**vs**
**FREQUENCY**

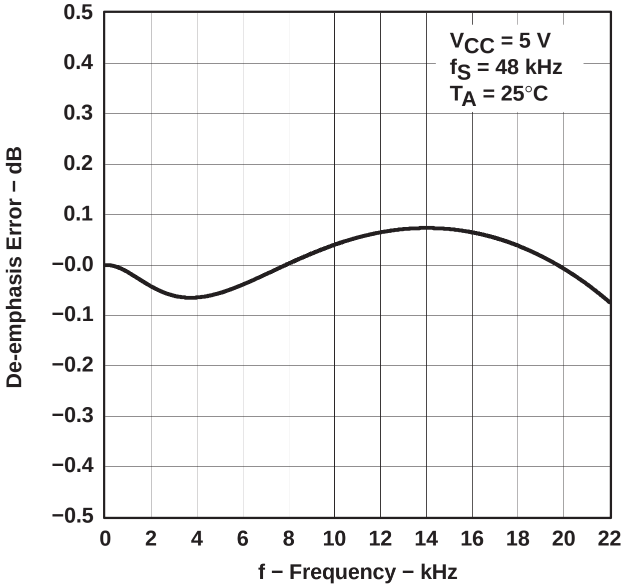


**Figure 16**

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $f_S$ = 44.1 kHz, system clock = 384 $f_S$ and 24-bit data, unless otherwise noted.

## TYPICAL CHARACTERISTICS—ANALOG DYNAMIC PERFORMANCE

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**SUPPLY VOLTAGE**

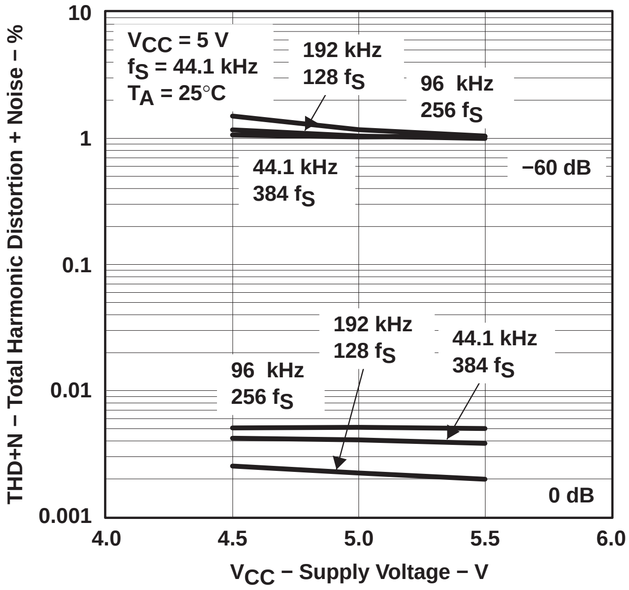


Figure 17

**DYNAMIC RANGE**
**vs**
**SUPPLY VOLTAGE**

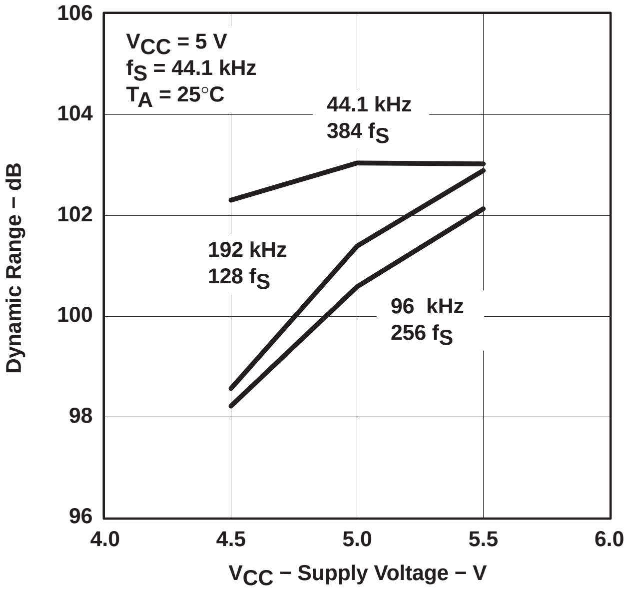


Figure 18

**SNR**
**vs**
**SUPPLY VOLTAGE**

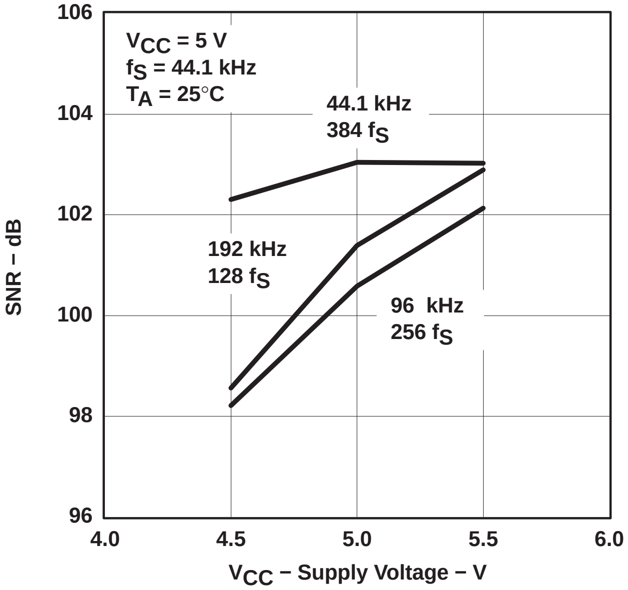


Figure 19

**CHANNEL SEPARATION**
**vs**
**SUPPLY VOLTAGE**

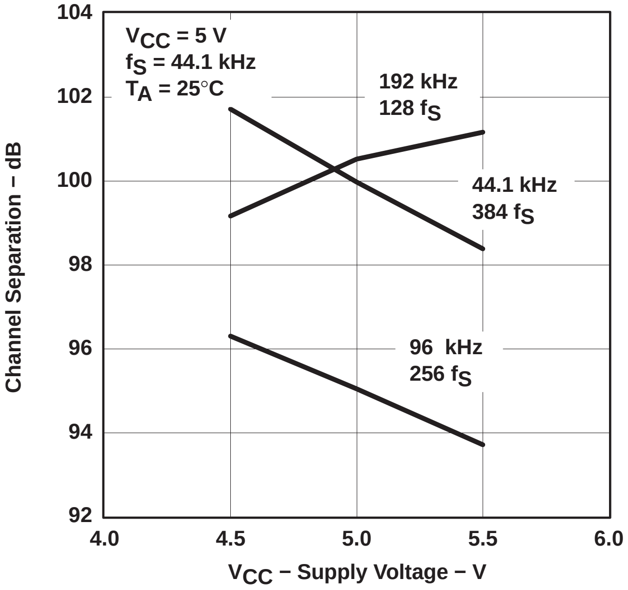


Figure 20

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $f_S$ = 44.1 kHz, system clock = 384 $f_S$ and 24-bit data, unless otherwise noted.

## TYPICAL CHARACTERISTICS—ANALOG DYNAMIC PERFORMANCE

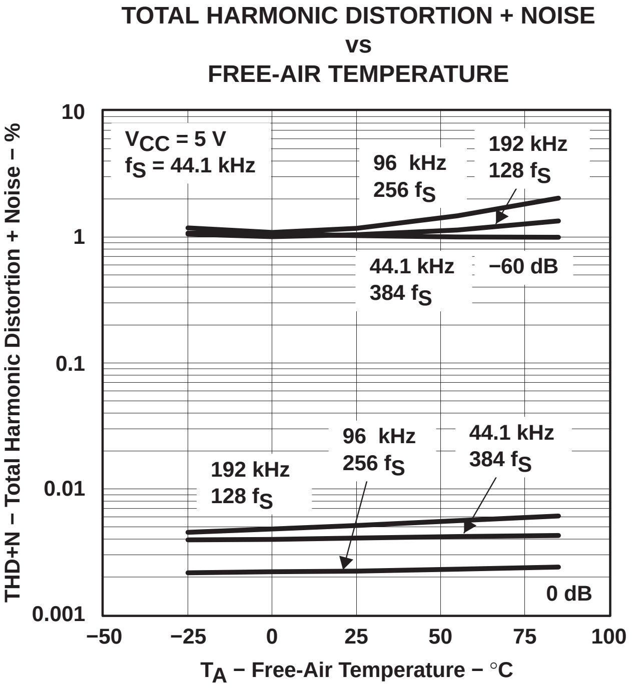


Figure 21

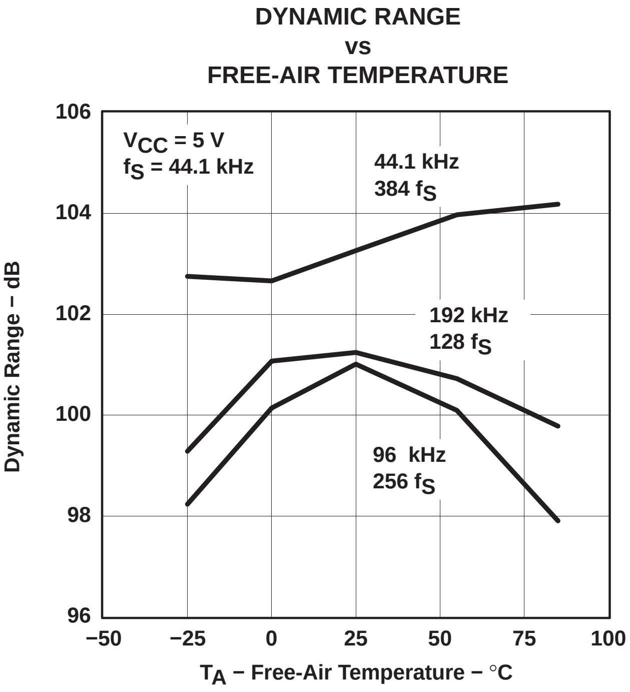


Figure 22

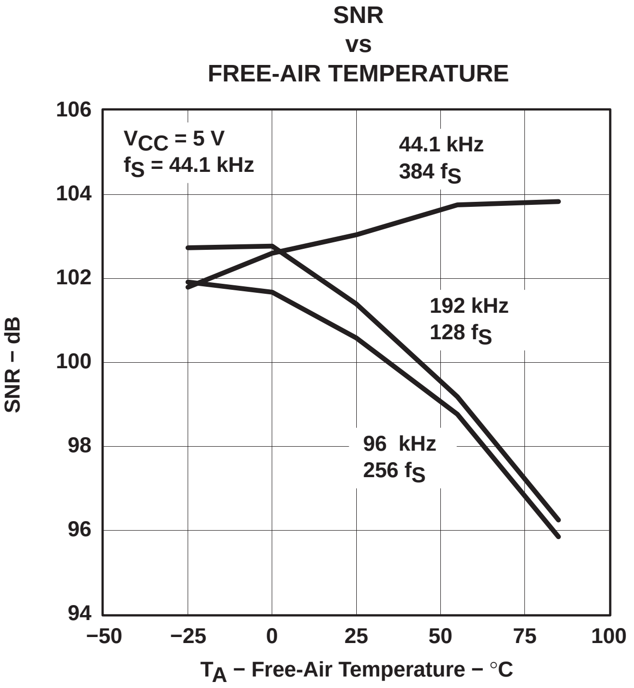


Figure 23

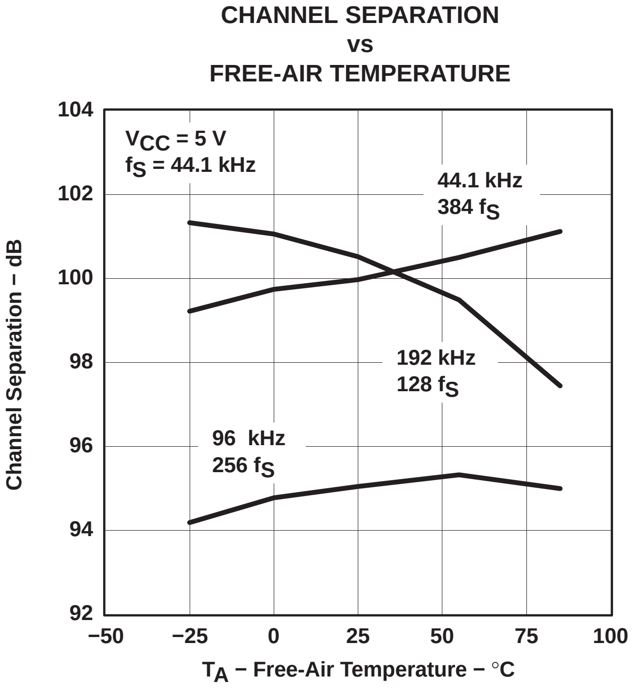


Figure 24

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $f_S$ = 44.1 kHz, system clock = 384 $f_S$ and 24-bit data, unless otherwise noted.

## TYPICAL CHARACTERISTICS—ANALOG DYNAMIC PERFORMANCE

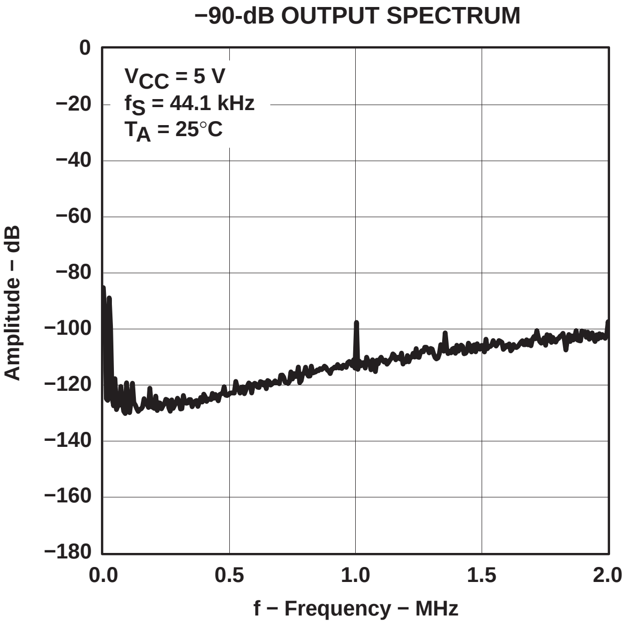


Figure 25

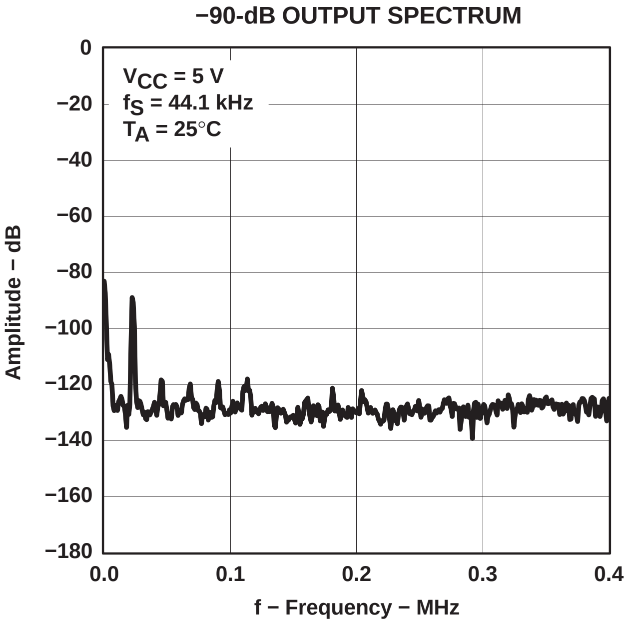


Figure 26

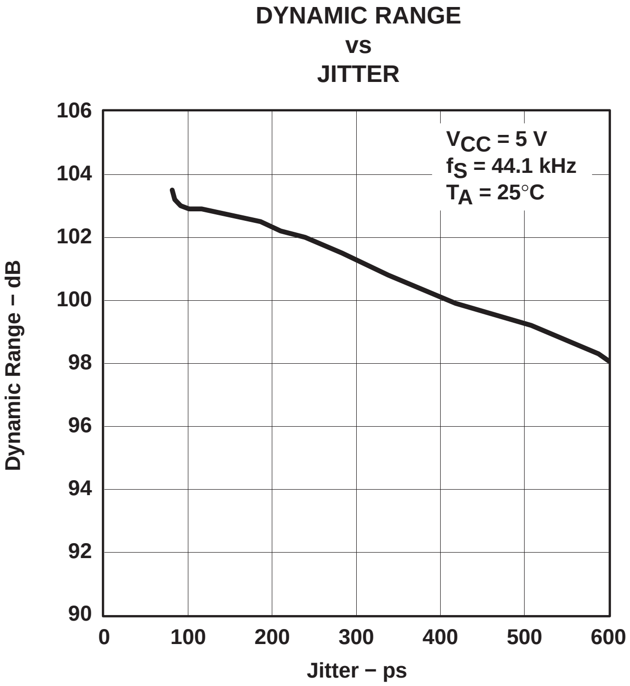


Figure 27

All specifications at $T_A$ = 25°C, $V_{CC}$ = 5 V, $f_S$ = 44.1 kHz, system clock = 384 $f_S$ and 24-bit data, unless otherwise noted.

## APPLICATION INFORMATION

### connection diagrams

A basic connection diagram is shown in Figure 28, with the necessary power supply bypassing and decoupling components. Texas Instruments recommends using the component values shown in Figure 28 for all designs.

A typical application diagram is shown in Figure 29. Texas Instruments' PLL1700 is used to generate the system clock input at SCKI, as well as generating the clock for the audio signal processor.

The use of series resistors (22 Ω to 100 Ω) is recommended for SCKI, LRCK, BCK, DATA1, DATA2, and DATA3. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter which removes high-frequency noise from the digital signal, thus, reducing high-frequency emission.

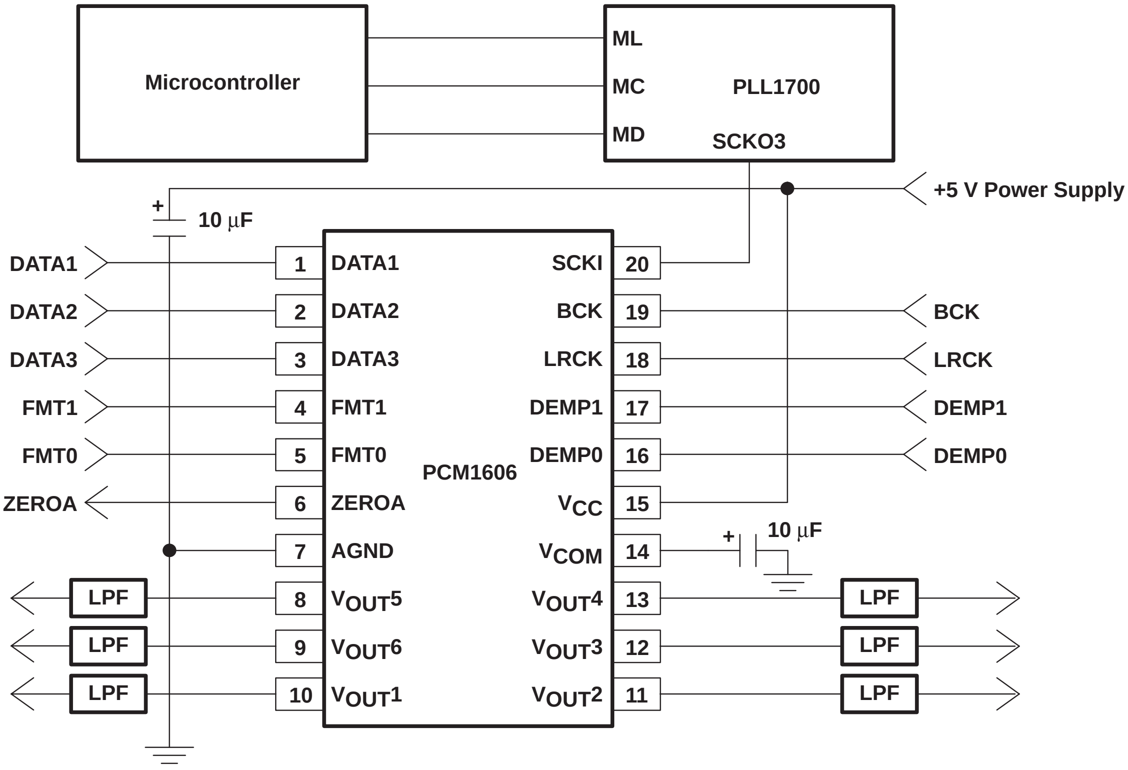
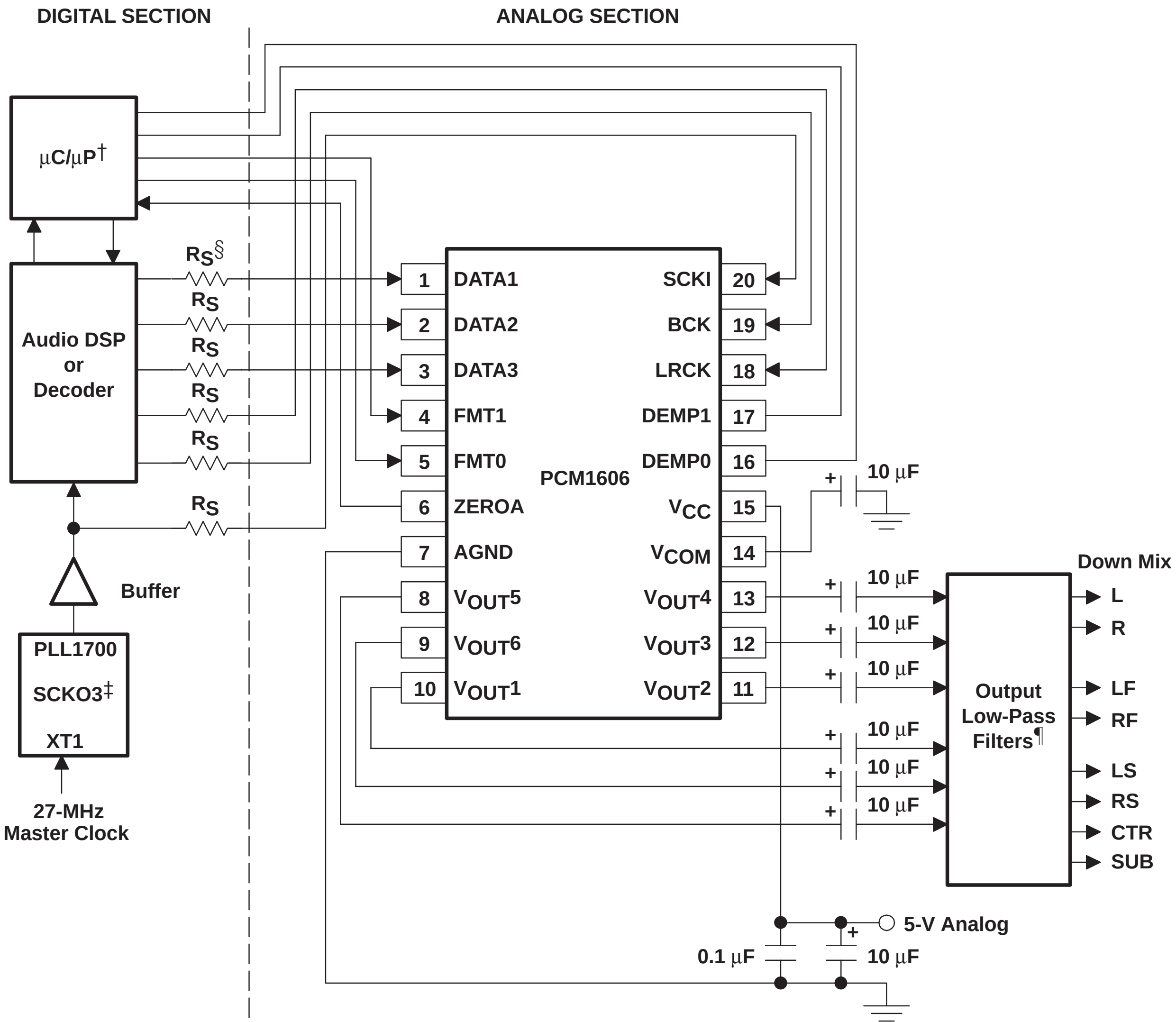


Figure 28. Basic Connection Diagram

## APPLICATION INFORMATION



† Format and de-emphasis control can be provided by the DSP/decoder.

‡ Actual clock output used is determined by the application.

§ $R_S$ = 22 Ω to 100 Ω

¶ See the *Application Information* section of this data sheet for more information.

**Figure 29. Typical Application Diagram**

### power supply and grounding

The PCM1606 requires a 5-V supply. The 5-V supply is used to power the DAC analog output-filter circuitry, the digital filter, and the serial interface circuitry.

Two capacitors are required for supply bypassing, as shown in Figure 29. These capacitors should be located as close as possible to the PCM1606 package. The 10-µF capacitors should be tantalum or aluminum electrolytic, while the 0.1-µF capacitors are ceramic (X7R type is recommended for surface-mount applications).

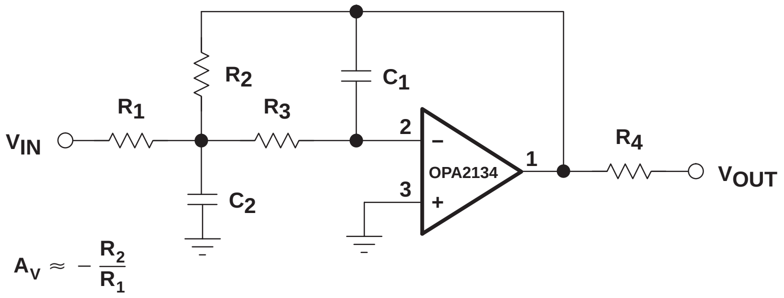
## APPLICATION INFORMATION

### D/A output filter circuits

Delta-sigma D/A converters utilize noise shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figure 30 and Figure 31 show the recommended external low-pass active filter circuits for dual- and single-supply applications. These circuits are 2nd-order Butterworth filters using the multiple feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, see your local Texas Instruments sales office.

Because the overall system performance is defined by the quality of the D/A converters and their associated analog output circuitry, high-quality audio op amps are recommended for the active filters. Texas Instruments' OPA2134 and OPA2353 dual op amps are shown in Figure 30 and Figure 31, and are recommended for use with the PCM1606.



$$A_V \approx -\frac{R_2}{R_1}$$

Figure 30. Dual-Supply Filter Circuit

$$A_V \approx -\frac{R_2}{R_1}$$

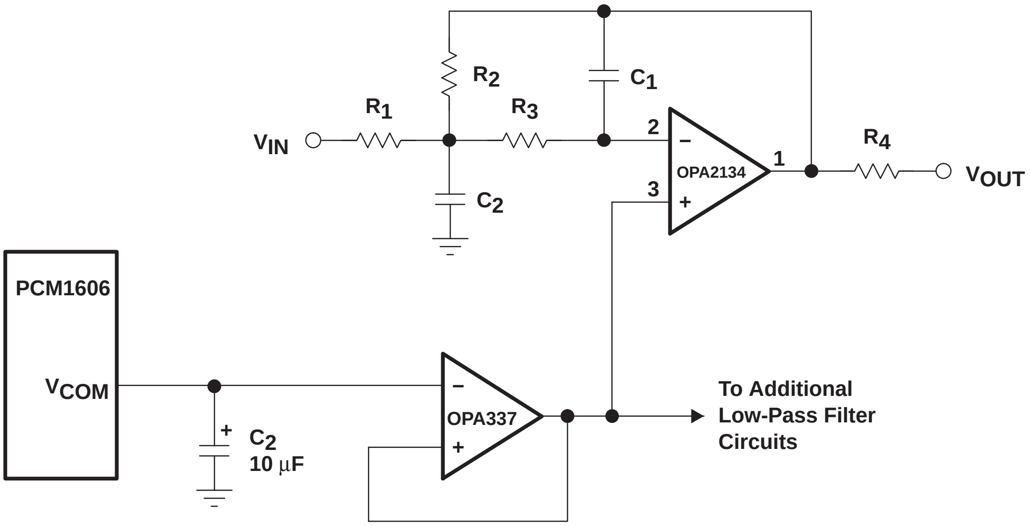


Figure 31. Single-Supply Filter Circuit

## APPLICATION INFORMATION

### PCB layout guidelines

A typical PCB layout for the PCM1606 is shown in Figure 32. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1606 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the D/A converters. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 33 shows the recommended approach for single-supply applications.

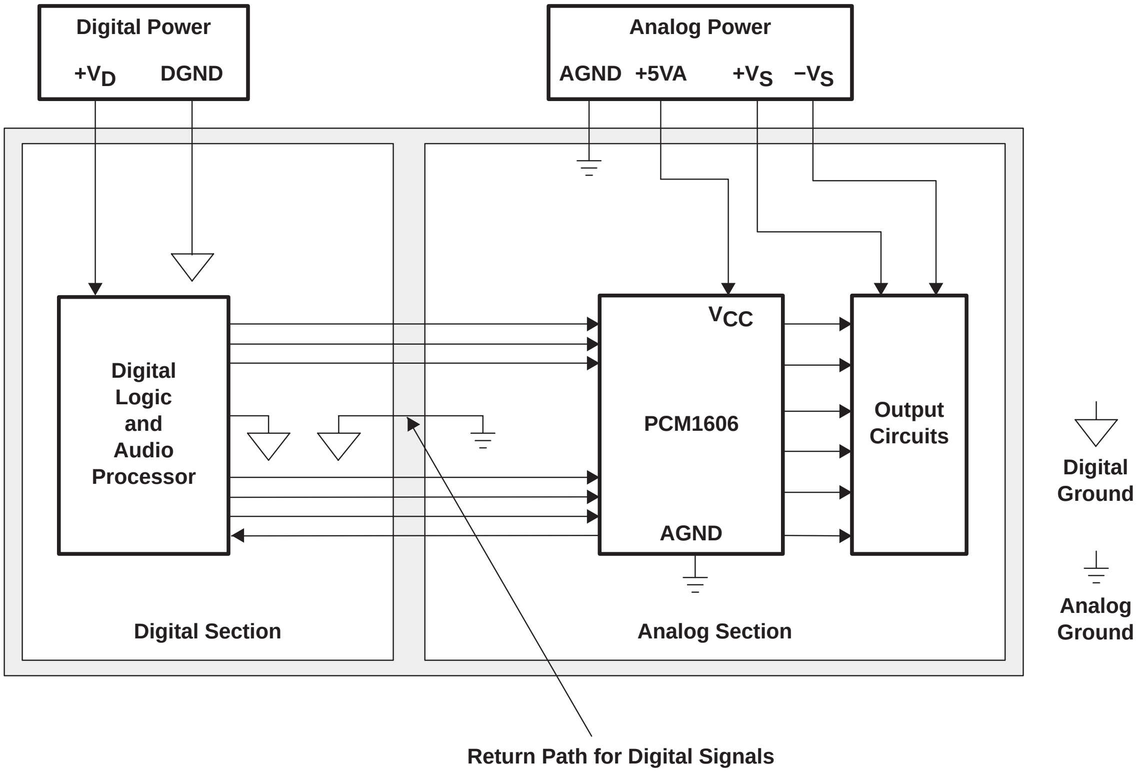


Figure 32. Recommended PCB Layout

## APPLICATION INFORMATION

### PCB layout guidelines (continued)

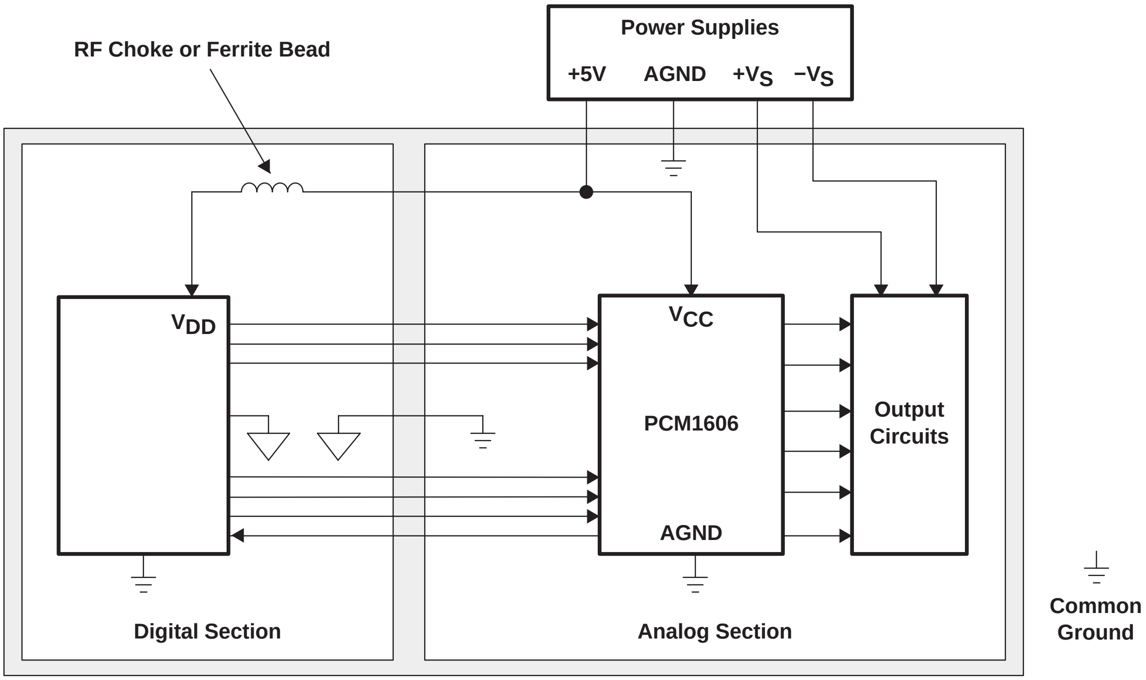


Figure 33. Single-Supply PCB Layout

### key performance parameters measurement

This section provides information on how to measure key dynamic performance parameters for the PCM1606. In all cases, a System Two Cascade Plus by Audio Precision or equivalent audio measurement system is used to perform the testing.

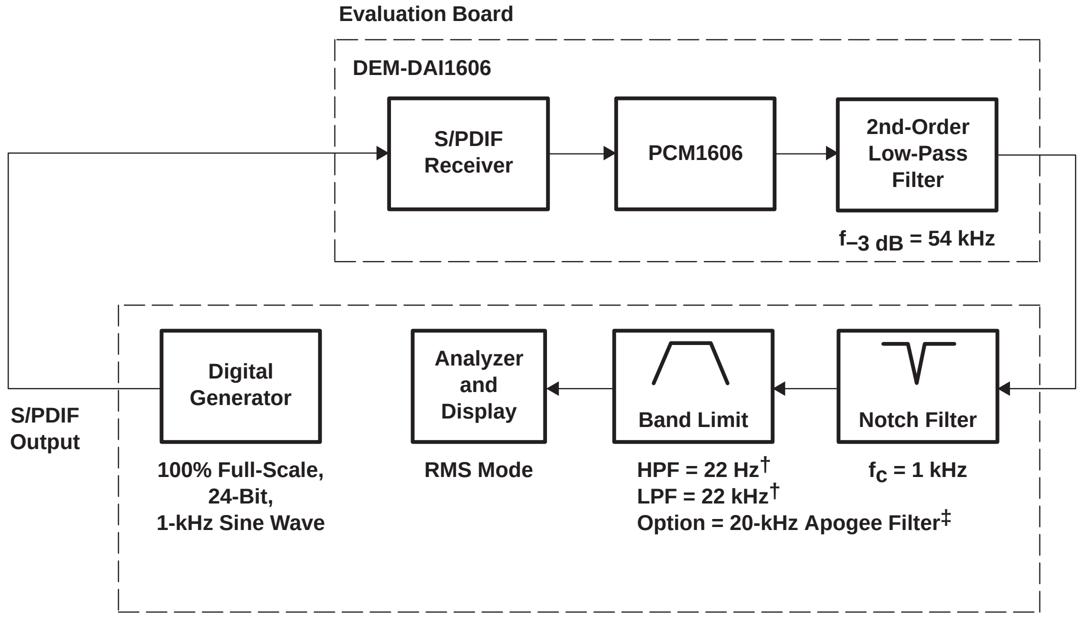
#### total harmonic distortion + noise

Total harmonic distortion + noise (THD+N) is a significant figure of merit for audio D/A converters, because it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The true rms value of the distortion and noise is referred to as THD+N.

For the PCM1606 D/A converters, THD+N is measured with a full scale, 1-kHz digital sine wave as the test stimulus at the input of the DAC. The digital generator is set to 24-bit audio word length and a sampling frequency of 44.1 kHz or 96 kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via coaxial cable to the digital audio receiver on the DEM−DAI1606 demo board. The receiver is then configured to output 24-bit data in either $I^2S$ or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band-limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

## APPLICATION INFORMATION

### total harmonic distortion + noise (continued)



† There is little difference in measured THD+N when using the various settings for these filters..

‡ Required for THD+N test.

Figure 34. Test Setup for THD+N Measurements

### dynamic range

Dynamic range is specified as A-weighted, THD+N measured with a –60 dB of full-scale (FS), 1-kHz digital sine wave stimulus at the input of the D/A converter. This measurement is designed to give a good indicator of how the DAC performs given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 35, and is similar to the THD+N test setup discussed previously. The differences include the band limit filter selection, the additional A-weighting filter, and the –60-dB FS input level.

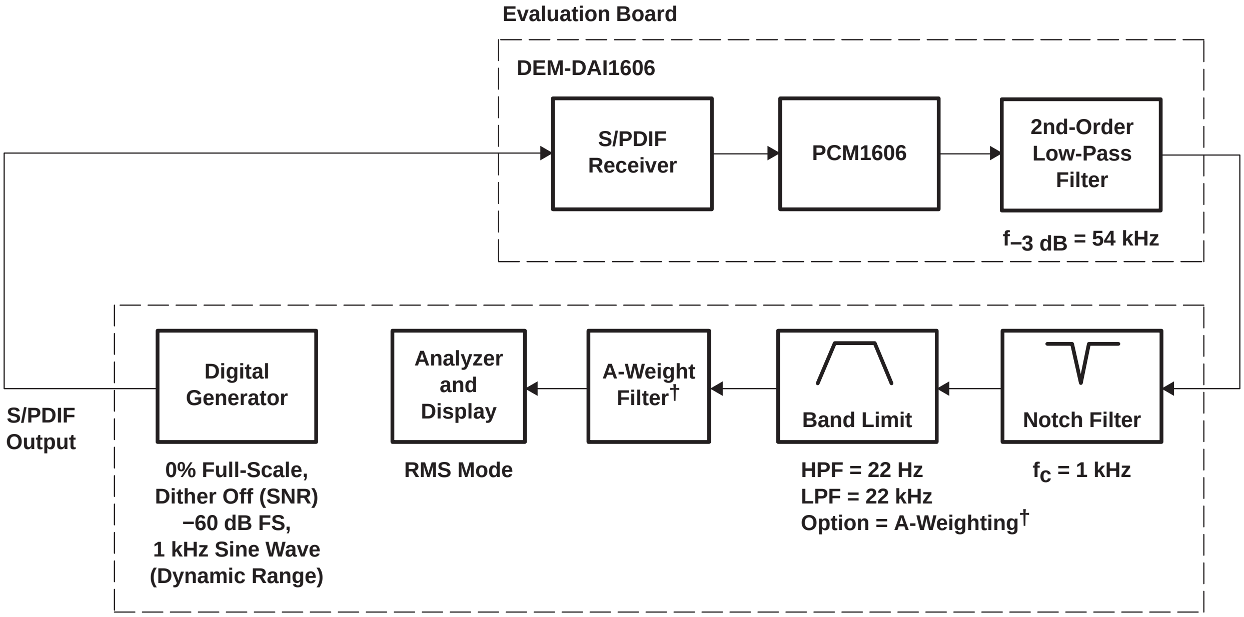
### idle channel signal-to-noise ratio

The signal-to-noise ratio (SNR) test provides a measure of the noise floor of the D/A converter. The input to the D/A is all 0s data. This ensures that the delta-sigma modulator output is connected to the output amplifier circuit so that idle tones (if present) can be observed and affect the SNR measurement. The dither function of the digital generator must also be disabled to ensure an all 0s data stream at the input of the D/A converter.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level. (See the note provided in Figure 35).

## APPLICATION INFORMATION

### idle channel signal-to-noise ratio (continued)



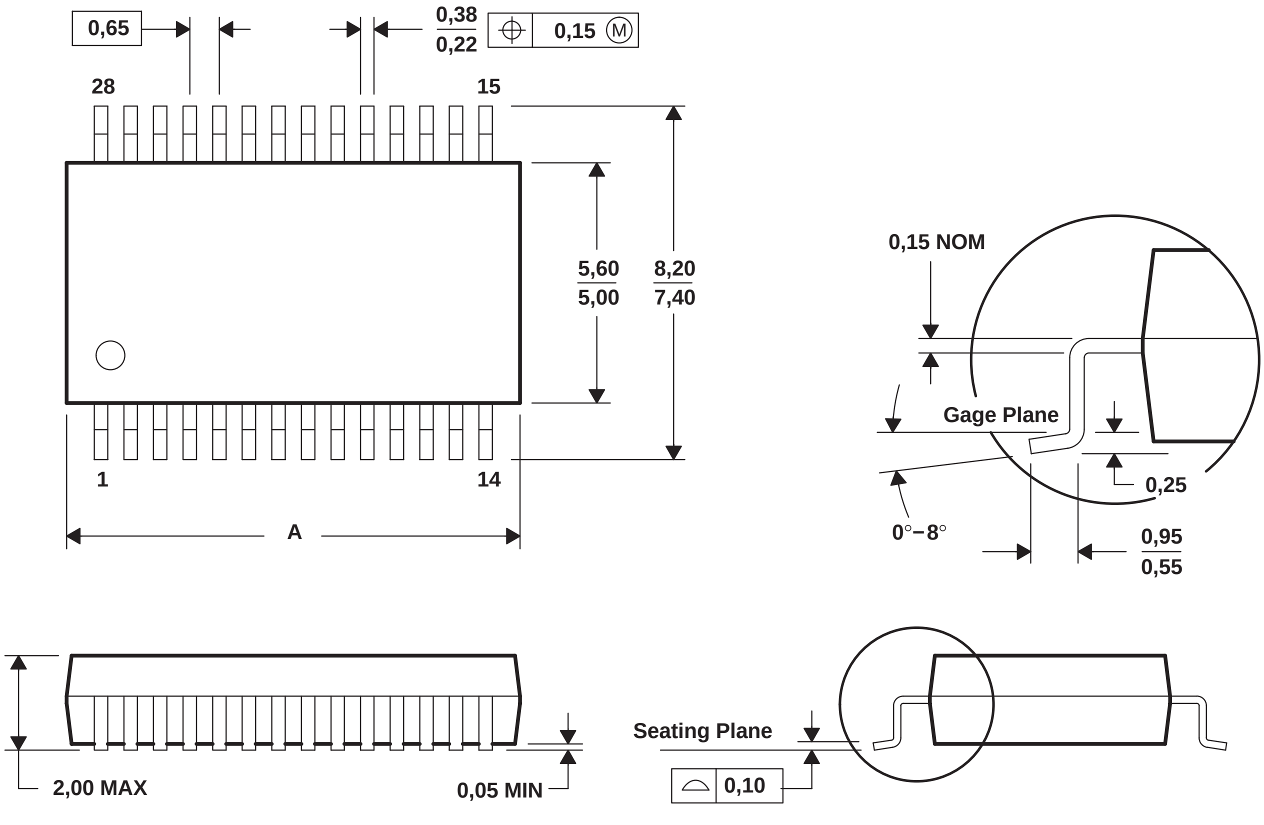
† Results without A-Weighting will be approximately 3 dB worse.

Figure 35. Test Setup for Dynamic Range and SNR Measurements

## MECHANICAL DATA

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



| PINS ** DIM | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /D 09/00**

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15 mm.
- D. Falls within JEDEC MO-150

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| PCM1606E | ACTIVE | SSOP | DB | 20 | 65 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1606E/2K | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1606E/2KG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM1606EG4 | ACTIVE | SSOP | DB | 20 | 65 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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| DLP® Products | www.dlp.com | Broadband | www.ti.com/broadband |
| DSP | dsp.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Clocks and Timers | www.ti.com/clocks | Medical | www.ti.com/medical |
| Interface | interface.ti.com | Military | www.ti.com/military |
| Logic | logic.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Power Mgmt | power.ti.com | Security | www.ti.com/security |
| Microcontrollers | microcontroller.ti.com | Telephony | www.ti.com/telephony |
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| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Wireless | www.ti.com/wireless |

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