

N-channel 650 V, 0.160  $\Omega$  typ., 18 A MDmesh M5  
Power MOSFETs in TO-220FP, I<sup>2</sup>PAKFP and TO-3PF packages

Datasheet - production data

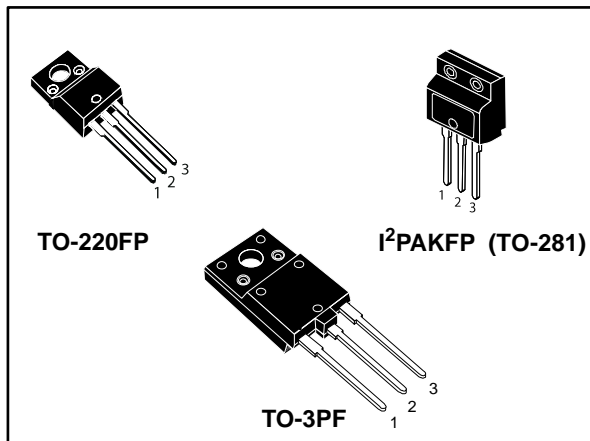
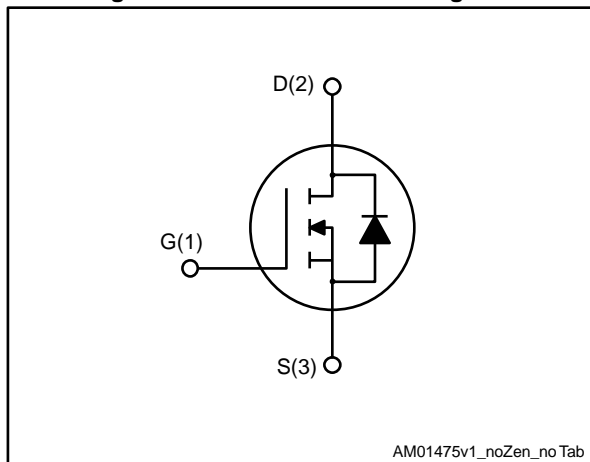


Figure 1: Internal schematic diagram



## Features

Order code	V <sub>DS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STF20N65M5	710 V	0.190 $\Omega$	18 A
STF120N65M5			
STFW20N65M5			

- Extremely low R<sub>DS(on)</sub>
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

## Applications

- Switching applications

## Description

These devices are N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF20N65M5	20N65M5	TO-220FP	Tube
STF120N65M5		I <sup>2</sup> PAKFP (TO-281)	
STFW20N65M5		TO-3PF	

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP, I <sup>2</sup> PAKFP	TO-3PF	
V <sub>GS</sub>	Gate- source voltage	±25		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	18 <sup>(1)</sup>		A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	11.3 <sup>(1)</sup>		A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	36 <sup>(1)</sup>		A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	30	48	W
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15		V/ns
V <sub>ISO</sub> <sup>(4)</sup>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)	2500	3500	V
T <sub>stg</sub>	Storage temperature range	- 55 to 150		°C
T <sub>j</sub>	Operating junction temperature range			

**Notes:**

(1)Limited by maximum junction temperature.

(2)Pulse width limited by safe operating area

(3) $I_{SD} \leq 18$  A,  $di/dt = 400$  A/ $\mu$ s,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400$  V

(4) $V_{DS} \leq 520$  V

Table 3: Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP, I <sup>2</sup> PAKFP	TO-3PF	
R <sub>thj-case</sub>	Thermal resistance junction-case	4.17	2.6	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient	62.5	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>jmax</sub> )	4	°C/W
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	270	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5: On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 650\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$		0.160	0.190	$\Omega$

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	1434	-	pF
$C_{oss}$	Output capacitance		-	38	-	pF
$C_{rss}$	Reverse transfer capacitance		-	3.7	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0\text{ to }520\text{ V}$	-	118	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	35	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	3.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 9\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see <a href="#">Figure 18: "Test circuit for gate charge behavior"</a> )	-	36	-	nC
$Q_{gs}$	Gate-source charge		-	7.5	-	nC
$Q_{gd}$	Gate-drain charge		-	18	-	nC

**Notes:**

<sup>(1)</sup> $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

<sup>(2)</sup> $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400 \text{ V}$ , $I_D = 12 \text{ A}$ , $R_G = 4.7 \text{ } \Omega$ , $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 19: "Test circuit for inductive load switching and diode recovery times"</a> and <a href="#">Figure 22: "Switching time waveform"</a> )	-	43	-	ns
$t_{r(V)}$	Voltage rise time		-	7.5	-	ns
$t_{f(i)}$	Current fall time		-	7.5	-	ns
$t_{c(off)}$	Crossing time		-	11.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 18 \text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 18 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$ (see <a href="#">Figure 19: "Test circuit for inductive load switching and diode recovery times"</a> )	-	288		ns
$Q_{rr}$	Reverse recovery charge		-	4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	27		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 18 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 19: "Test circuit for inductive load switching and diode recovery times"</a> )	-	342		ns
$Q_{rr}$	Reverse recovery charge		-	4.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	28		A

**Notes:**

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curve)

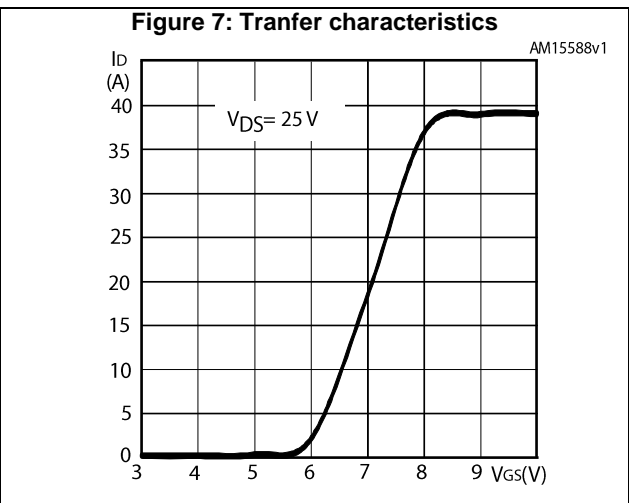
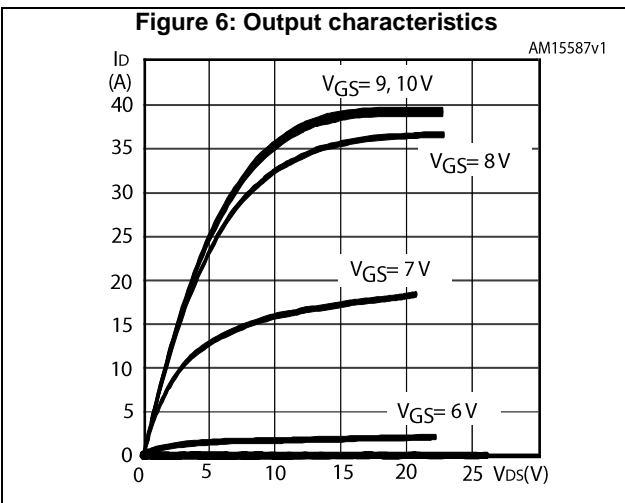
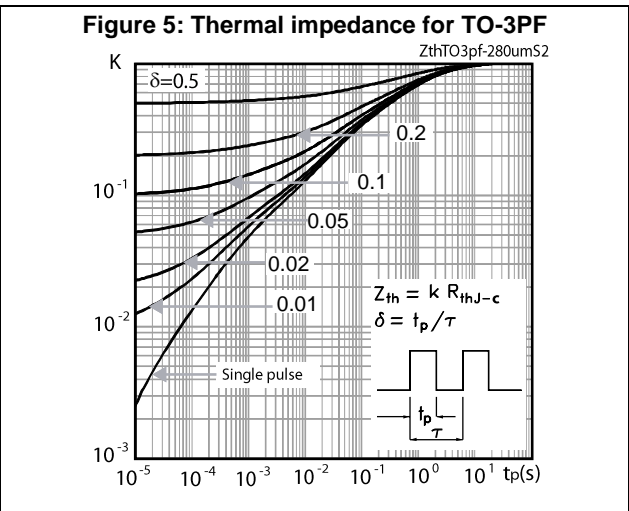
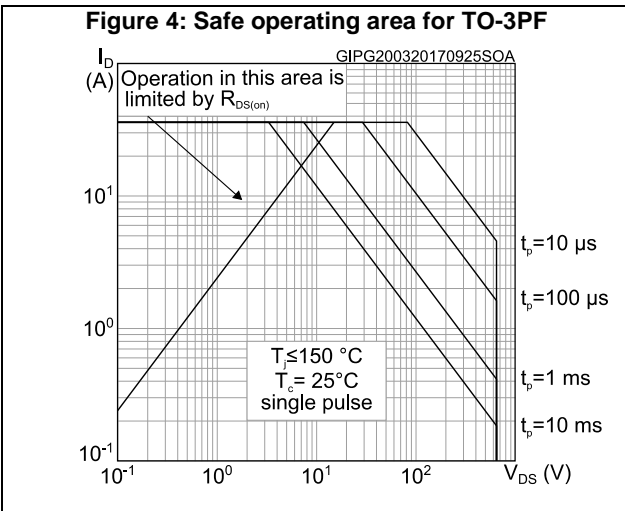
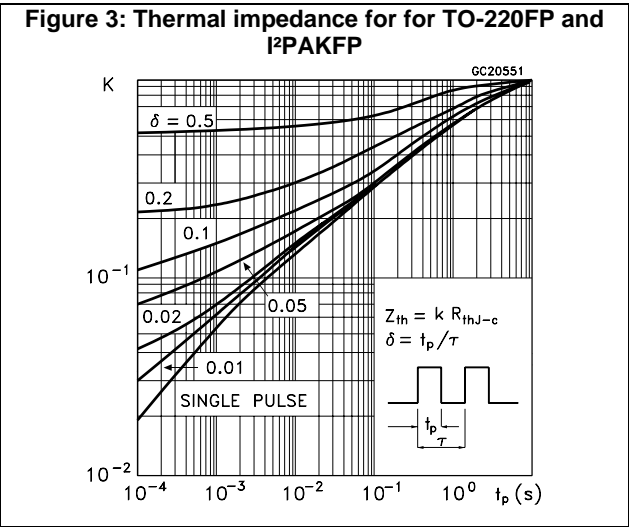
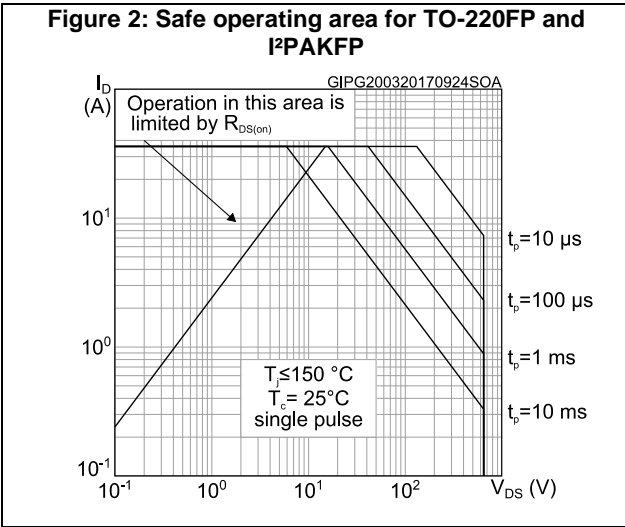


Figure 8: Gate charge vs gate-source voltage

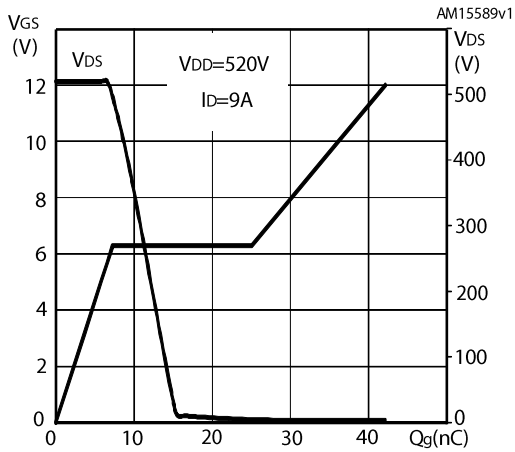


Figure 9: Static drain-source on-resistance

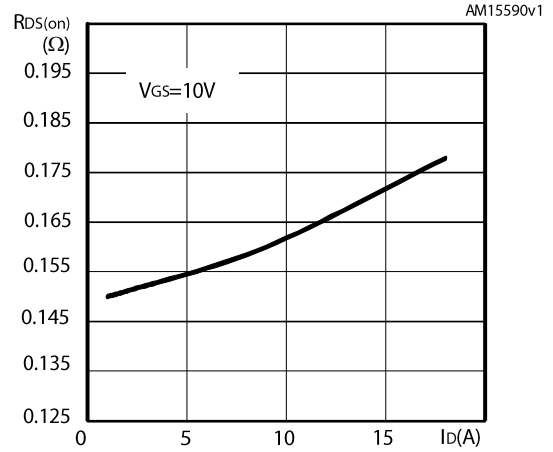


Figure 10: Capacitance variations

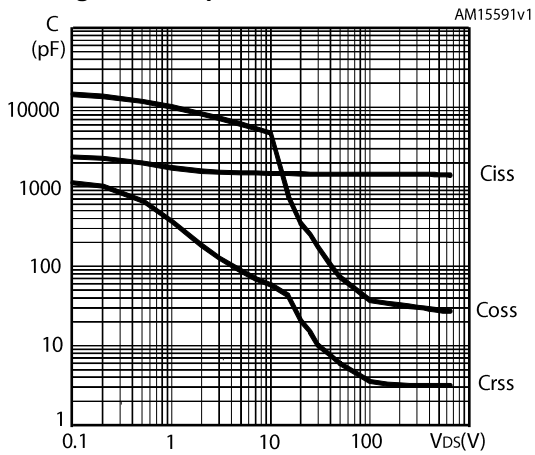


Figure 11: Output capacitance stored energy

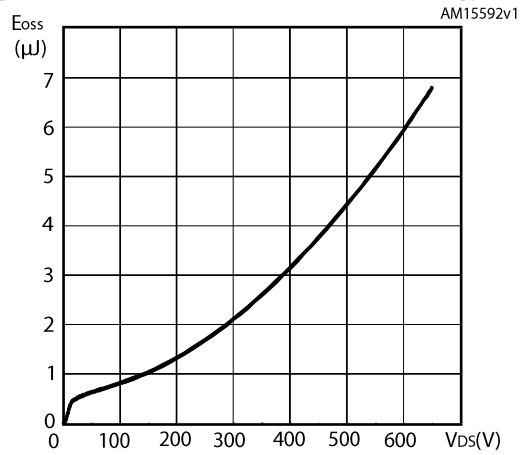


Figure 12: Normalized gate threshold voltage vs temperature

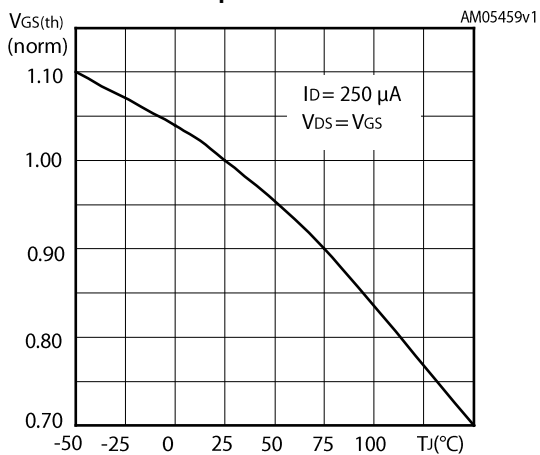
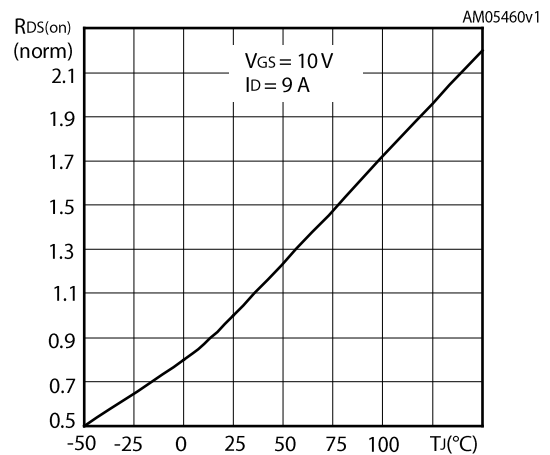
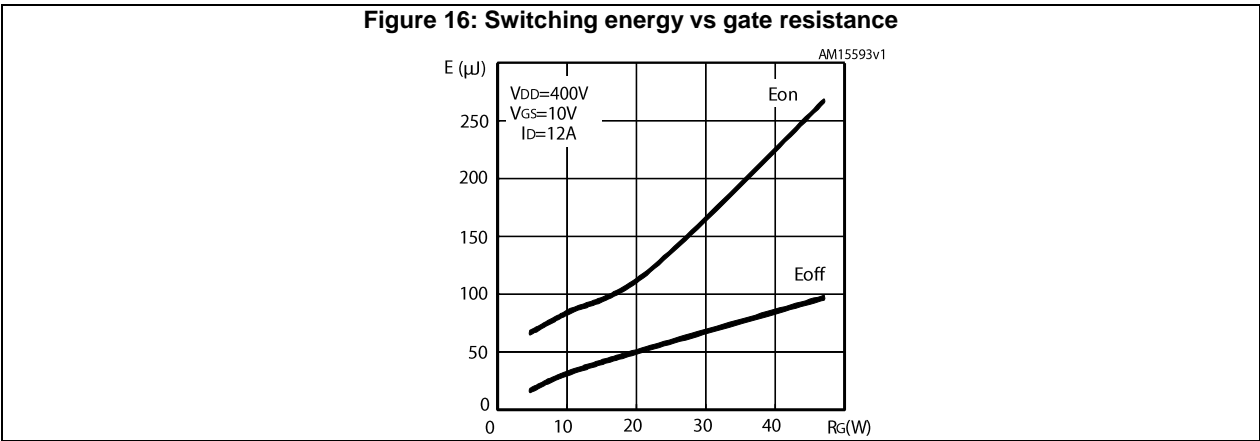
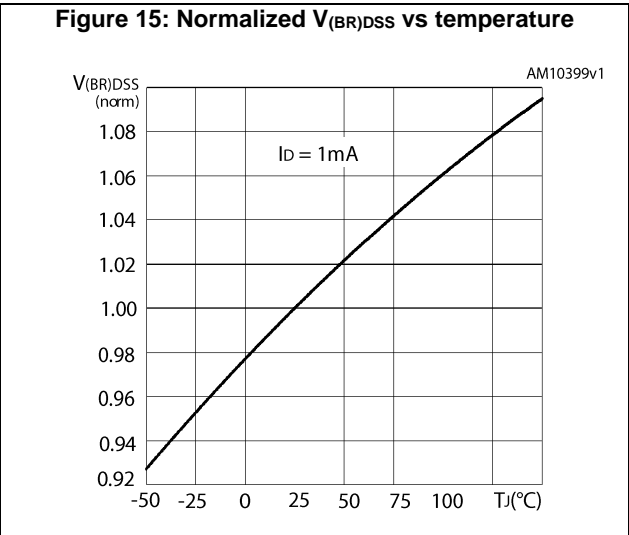
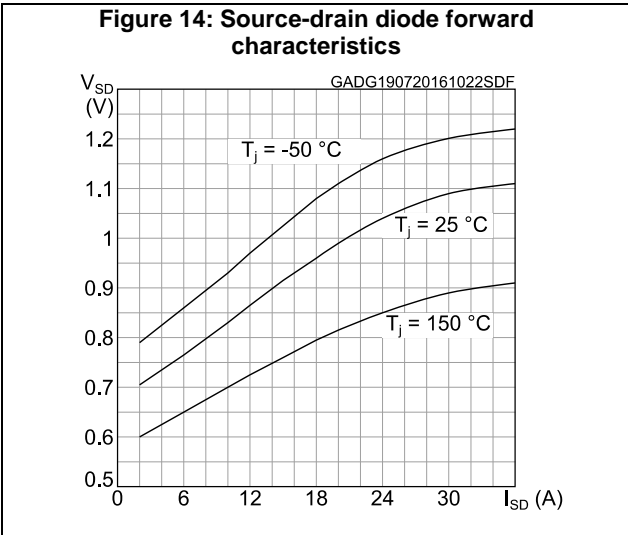


Figure 13: Normalized on-resistance vs temperature



Electrical characteristics

STF20N65M5,STFI20N65M5,STFW20N65M5

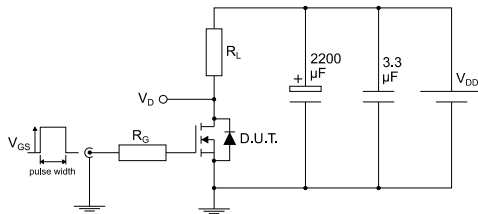


$E_{on}$  including reverse recovery of a SiC diode.



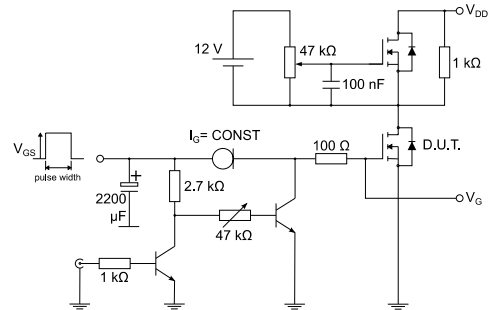
### 3 Test circuits

**Figure 17: Test circuit for resistive load switching times**



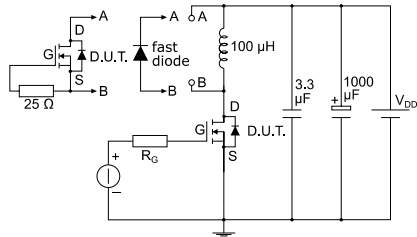
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**Figure 18: Test circuit for gate charge behavior**



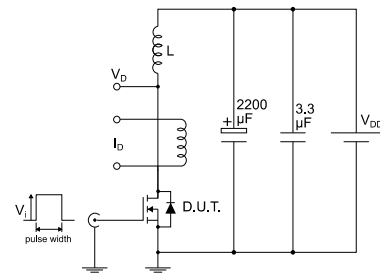
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**Figure 19: Test circuit for inductive load switching and diode recovery times**



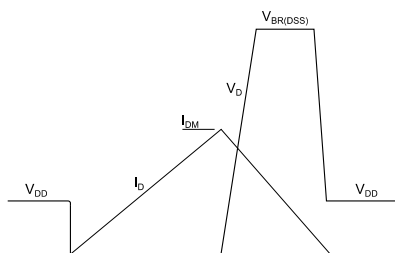
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**Figure 20: Unclamped inductive load test circuit**



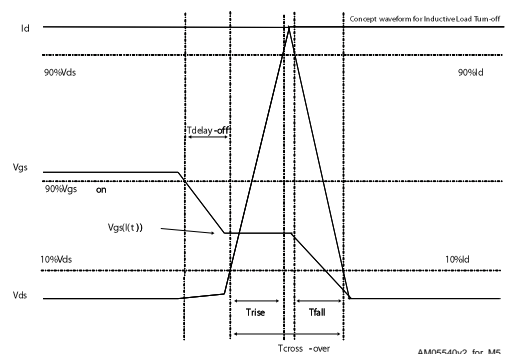
AM01471v1

**Figure 21: Unclamped inductive waveform**



AM01472v1

**Figure 22: Switching time waveform**



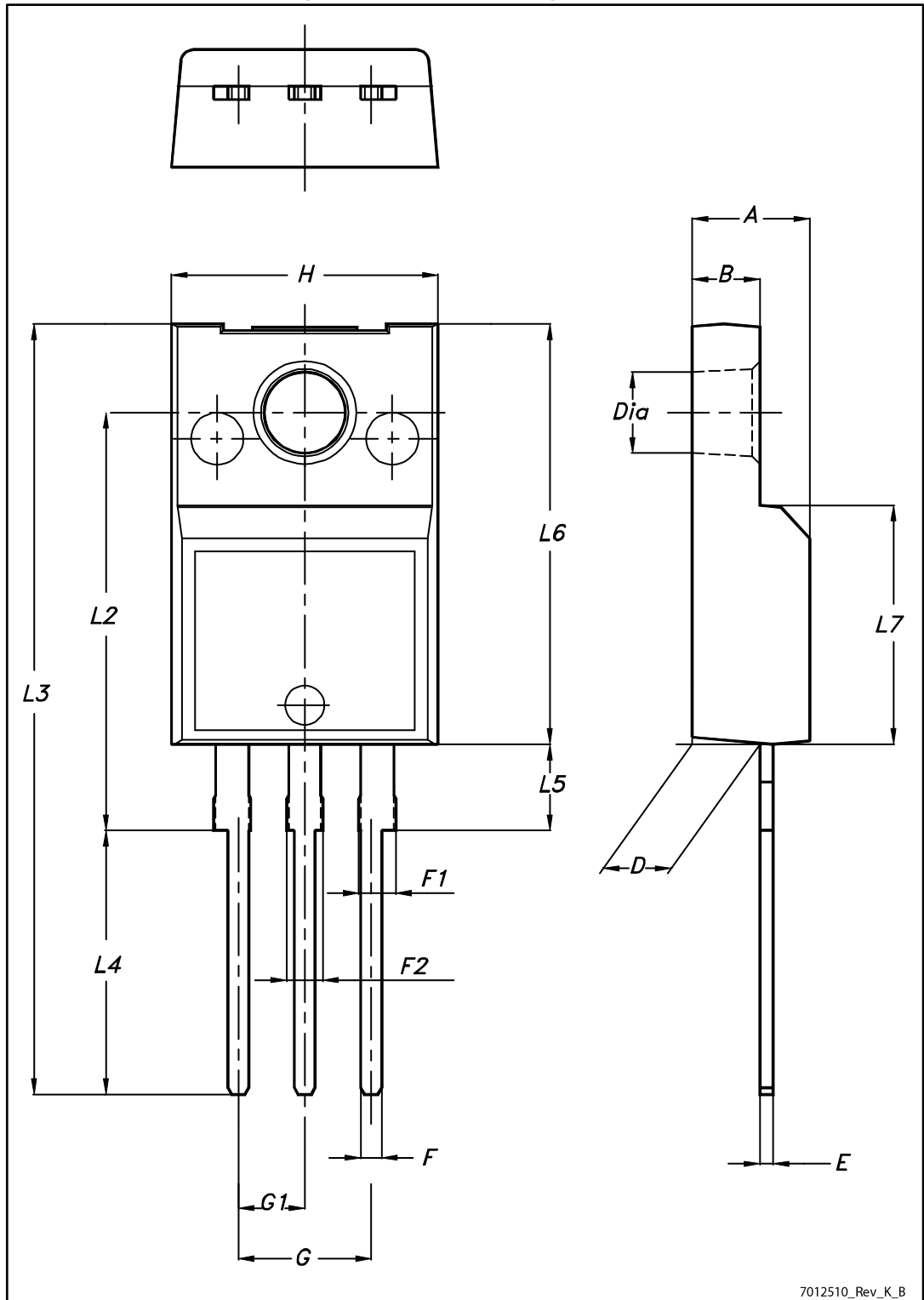
AM05540v2\_for\_M5

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-220FP package information

Figure 23: TO-220FP package outline



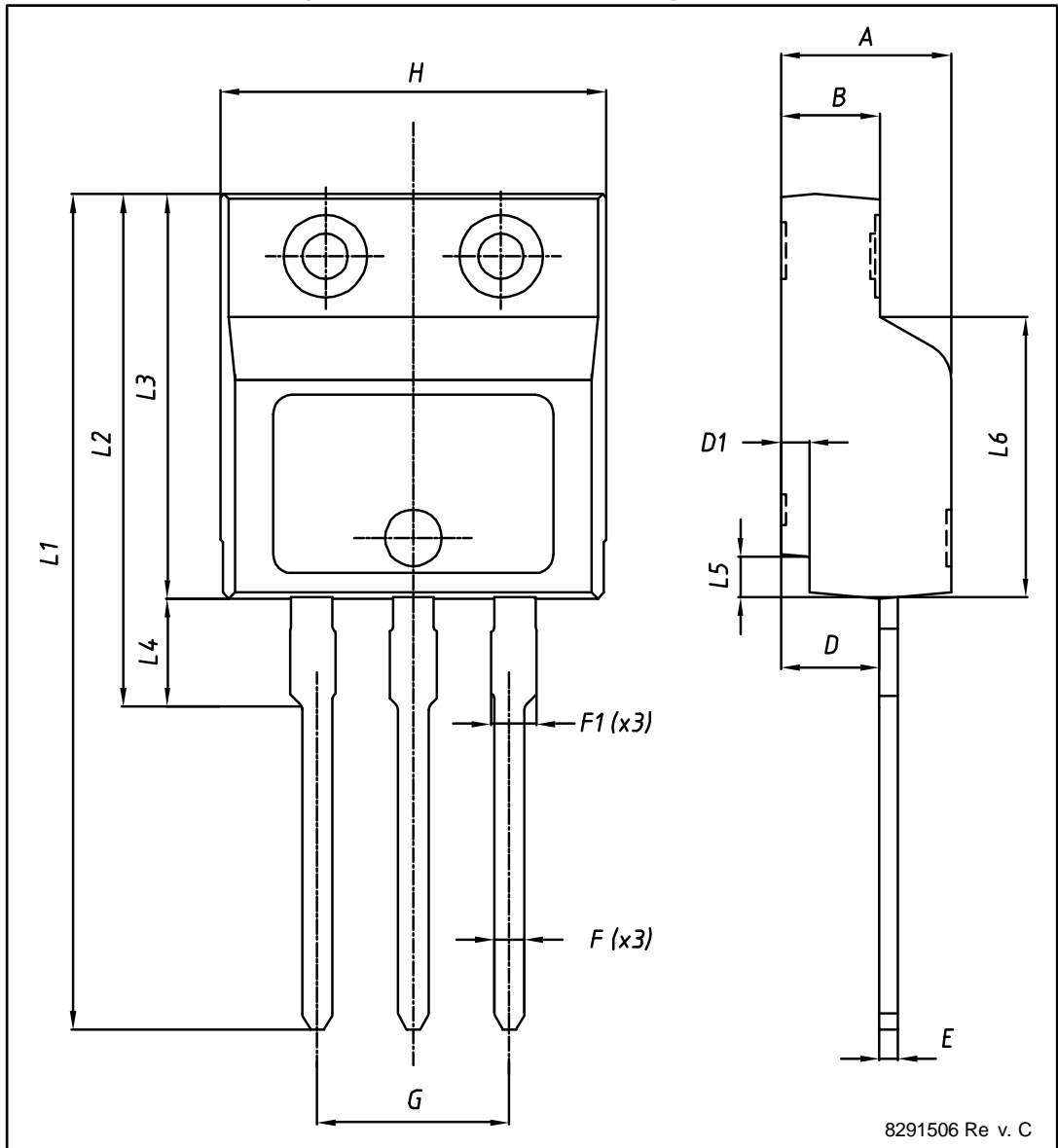
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Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

### 4.2 I<sup>2</sup>PAKFP (TO-281) package information

Figure 24: I<sup>2</sup>PAKFP (TO-281) package outline



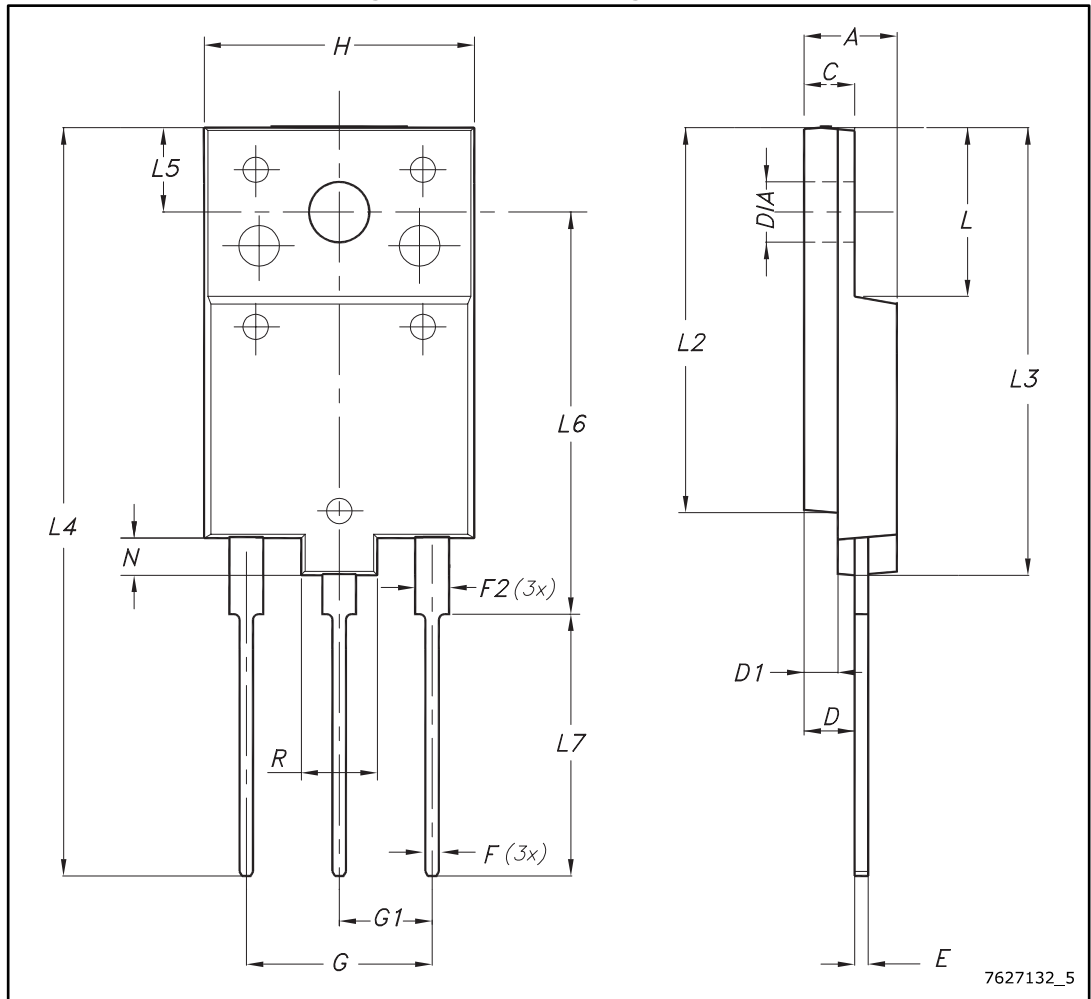
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Table 10: I<sup>2</sup>PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

### 4.3 TO-3PF package information

Figure 25: TO-3PF package outline



7627132\_5

Table 11: TO-3PF mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80



## 5 Revision history

**Table 12: Document revision history**

Date	Revision	Changes
01-Feb-2013	1	First release. Part numbers previously included in datasheet DM00049308
21-Jul-2016	2	Added device in TO-3PF. Modified: <i>Table 2: "Absolute maximum ratings", Table 5: "On /off states"</i> . Modified: <i>Figure 2: "Safe operating area for TO-220FP and I<sup>2</sup>PAKFP", Figure 4: "Safe operating area for TO-3PF", Figure 5: "Thermal impedance for TO-3PF"</i> . Minor text changes
22-Mar-2017	3	Modified <i>Table 2: "Absolute maximum ratings", Table 8: "Source drain diode"</i> . Modified <i>Figure 2: "Safe operating area for TO-220FP and I<sup>2</sup>PAKFP", Figure 4: "Safe operating area for TO-3PF", Figure 12: "Normalized gate threshold voltage vs temperature ", Figure 13: "Normalized on-resistance vs temperature" and Figure 14: "Source-drain diode forward characteristics "</i> . Minor text changes.

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