## UM11853 KITPF5030FRDMEVM evaluation board Rev. 1.0 — 7 March 2023

**User manual** 

#### **Document information**

Information	Content
Keywords	PF5030, KITPF5030FRDMEVM, KL25Z, I <sup>2</sup> C, spf-53090
Abstract	The KITPF5030FRDMEVM provides flexibility to explore all the features of the device and make measurements on the main part of the application.



#### Revision history

Rev	Date	Description
v.1.0	20230307	Initial release

## Important notice

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This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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## 1 Introduction

The KITPF5030FRDMEVM board user manual is intended for the engineers involved in the evaluation, design, implementation, and validation of PF5030 Configurable Power Management IC.

The KITPF5030FRDMEVM enables development on PF5030 family of devices. The kit can be connected to the NXP GUI software, which allows you to explore registers, try OTP configurations, and burn the part.

The devices can be placed and removed easily from the board by using the socket. This board supports PF5030 family of devices. The board delivered comprises a soldered device with empty OTP content in order to leave the opportunity to the user to burn the OTP configuration. The board contains a superset device PPF5030BMDA0ES, allowing tests on all the PF5030 derivatives. Each device OTP can be burned twice, which provides flexibility.

## 2 Finding resources and information on the NXP website

NXP Semiconductors provides online resources for this evaluation board and its supported devices on <u>http://www.nxp.com</u>.

The information page for KITPF5030FRDMEVM board is available at <u>www.nxp.com/KITPF5030FRDMEVM</u>. The information page provides overview information, documentation, software and tools, parametric data, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the KITPF5030FRDMEVM board, including the downloadable assets referenced in this document.

The information page for "NXP GUI for Automotive PMIC Families" is at <u>http://www.nxp.com/NXP GUI for</u> <u>Automotive PMIC Families</u>. The information page provides overview information, documentation, downloads, and development tools.

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## 3 Getting ready

Working with the KITPF5030FRDMEVM requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

## 3.1 Kit contents

- · Assembled and tested KITPF5030FRDMEVM connected to a FRDM-KL25Z in an anti-static bag
- 2 ft or 3 ft USB-STD A to USB-B-mini cable
- 1x Pluggable terminal block, two positions, straight, 3.81 mm pitch
- 3x Pluggable terminal block, three positions, straight, 3.81 mm pitch
- Jumpers mounted on board
- Quick Start Guide

### 3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

• One or two power supplies with a range from 3.3 V to 5.0 V, and a current limit set initially to 1.0 A

## 3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

• USB-enabled computer with Windows 7 or Windows 10

## 3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation boards information page.

- www.nxp.com/KITPF5030FRDMEVM
- NXP GUI for automotive PMIC families latest version

## 4 Getting to know the hardware

The KITPF5030FRDMEVM provides flexibility to explore all the features of the device and make measurements on the main part of the application. In combination with the FRDM-KL25Z MCU board, the NXP GUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. DC-DC switching nodes and other nonuser signals are mapped on test points. Digital signals (I<sup>2</sup>C, RSTB) are accessible through connectors. Pin PWRON has a switch to control them. A supply switch is available to power on or off the device.

The main purpose of this kit is to burn the OTP configuration. The main purpose of this kit is to evaluate PF5030 in automotive applications. The device always starts loading the fused configuration (OTP) (that may be blank) to the mirror registers, then the user can override the mirrors using Emulation mode. The device can be programmed/fused two times. This board is able to fuse the OTP without any extra tools or board. In Emulation mode, as long as the power is supplied, the board configuration stays valid. However, the main and fail-safe configurations are lost when the device restarts or goes into deep fail-safe (DEEP-FS) state, because OTP is reloaded and overwrite the mirrors content.

Note: Due to the socket, this kit is not optimized for performance measurement or current higher than 1.0 A.

### 4.1 Kit overview

The KITPF5030FRDMEVM is a hardware evaluation tool that allows OTP burning. Due to the socket, PF5030 part can be configured without the need to solder it. Devices can be programmed two times. The KITPF5030FRDMEVM is a hardware evaluation tool that allows performance test. PF5030 can be evaluated with this board because it is populated with a superset part. The PPF5030BMDA0ES part soldered on the board can be fused twice.

An Emulation mode is possible to test as many configurations as needed. From USB voltage, an external DC-DC provides VDDIO\_SEL voltage with a choice of 1.8 V, 3.3 V (default), or 5.0 V. Furthermore, another external DC-DC generates the OTP programming voltage (7.95 V) without any need for an external power supply.

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## 4.2 KITPF5030FRDMEVM features

- VIN power supply connector (1x or 2x 3.3 V to 5.0 V)
- BUCK1 and BUCK2: 0.7 V to 1.5 V up to 1.0 A (socket limit)
- BUCK3: 1.0 V to 3.3 V up to 1.0 A (socket limit)
- LDO1 and LDO2: 1.5 V to 5.0 V
- PWRON switch
- FS0B external safety pin
- Embedded USB connection for easy connection to software NXP GUI (access to I<sup>2</sup>C bus, IOs, RSTB, FS0B, INTB, debug, AMUX\_OUT, regulators, register access, OTP emulation, and OTP programming)
- · LEDs that indicate signals and regulator status
- Support OTP fuse capabilities
- Voltage monitoring jumper setting

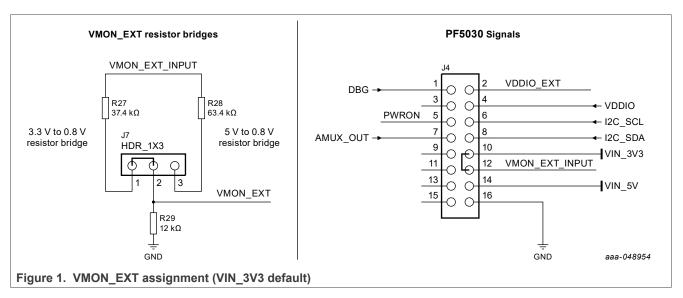
### 4.3 Schematic, board layout, and bill of materials

The schematic, board layout, and bill of materials for the KITPF5030FRDMEVM board are available at <a href="https://www.nxp.com/KITPF5030FRDMEVM">www.nxp.com/KITPF5030FRDMEVM</a>.

#### 4.3.1 VMON board configuration

The VMON configuration is highly dependent on the use case. This kit is delivered with a default configuration.

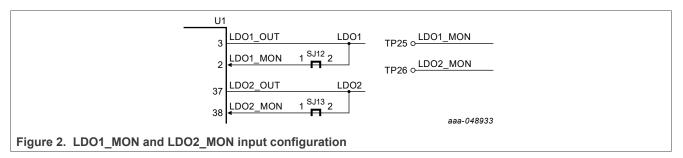
The user can assign VMON\_EXT differently to address the use case using J4 and J7 connectors shown in <u>Figure 1</u>. J7 is used to select the VMON\_EXT (VMON0) external resistor divider to monitor 3.3 V or 5.0 V. J4 is used to connect the VMON\_EXT external resistor divider input VMON\_EXT\_INPUT to an external voltage, VIN\_3V3, or VIN\_5V. By default, VMON\_EXT is monitoring VIN\_3V3.



By default, BUCK2\_FB (VMON2) is connected to BUCK2 though SJ2. However, When BUCK2 is disabled or used in multiphase with BUCK1, BUCK2\_FB can be connected to an external voltage. R17 and SJ4 must be open in this case and the internal DAC must be configured to the voltage monitoring target.

By default, LDO1\_MON (VMON4) and LDO2\_MON (VMON5) pins are tied to LDO1 and LDO2, respectively. LDO1\_MON and LDO2\_MON can be used to monitor an external voltage using test points TP25 (LDO1\_MON) and TP26 (LDO2\_MON). Solder joints SJ12 and/or SJ13 must be opened in this case. Figure 2 shows the

corresponding part of the schematic. The internal resistors dividers can be configured to select the voltage monitoring target.



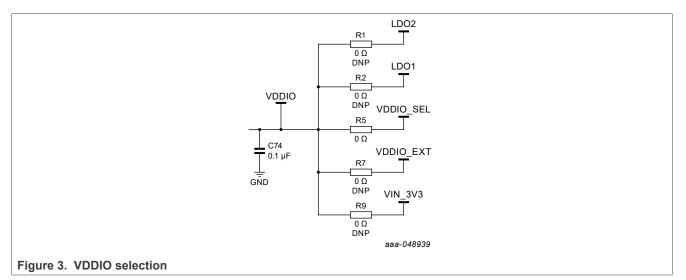
## 4.3.2 I<sup>2</sup>C

The I<sup>2</sup>C bus is connected to KL25Z MCU to communicate with NXP GUI. Another MCU can be connected to the I<sup>2</sup>C bus on J4 connector, but R58 and R59 must be removed. In addition to this change, make sure that the VDDIO voltage domain and ground are the same on MCU side and KITPF5030FRDMEVM side.

### 4.3.3 VDDIO

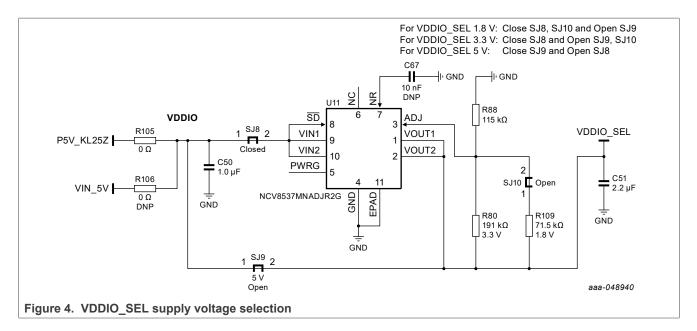
The VDDIO pin is powered through VDDIO net and is used to supply internal buffers and  $I^2C$  communication.

The selection of VDDIO is made using R1, R2, R5, R7, and R9 resistors as shown in <u>Figure 3</u>. By default, an external LDO is provided to feed VDDIO through the VDDIO\_SEL net.



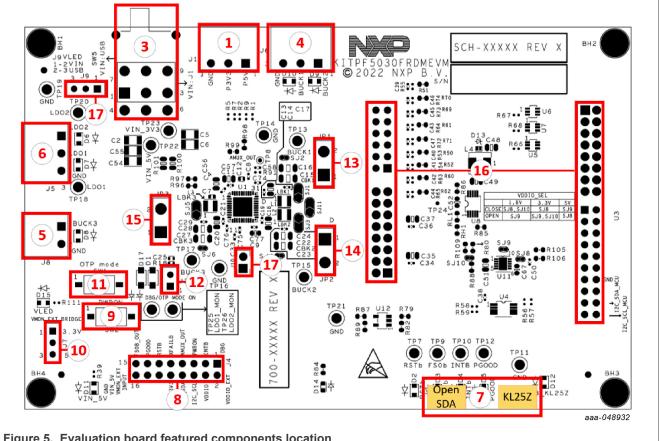
The I<sup>2</sup>C is compatible with 1.8 V, 3.3 V, and 5.0 V, therefore VDDIO\_SEL voltage is configurable between 1.8 V, 3.3 V, or 5.0 V using SJ8, SJ9, and SJ10 connectors (3.3 V by default) shown in <u>Figure 4</u>.

### **KITPF5030FRDMEVM** evaluation board



## 4.4 Kit featured components

Figure 5 identifies important components and Table 1 provides details.



### KITPF5030FRDMEVM evaluation board

Number	Description
1	VIN_5V and VIN_3V3 power supply input
3	<ul> <li>VIN three position switch</li> <li>Left position: VIN from USB</li> <li>Middle position: board not supplied</li> <li>Right position: VIN from J1</li> </ul>
4	BUCK1/2 regulators output
5	BUCK3 regulator output
6	LDO1/2 regulators output
7	USB connectors (OpenSDA for MCU flash; KL25Z for NXP GUI control)
8	Debug connectivity. Access to PF5030 signals
9	PWRON switch
10	VMON_EXT resistor bridge configuration (choice between monitoring 3.3 V or 5.0 V)
11	OTP mode switch
12	DBG pin to ground if unplugged
13	BUCK1 inductor current measurement jumper
14	BUCK2 inductor current measurement jumper
15	BUCK3 inductor current measurement jumper
16	KL25Z freedom board connectors
17	VLED supply configuration

#### Table 1. Evaluation board featured components location

### 4.4.1 Connectors

Figure 6 shows the location of connectors on the board.

#### KITPF5030FRDMEVM evaluation board

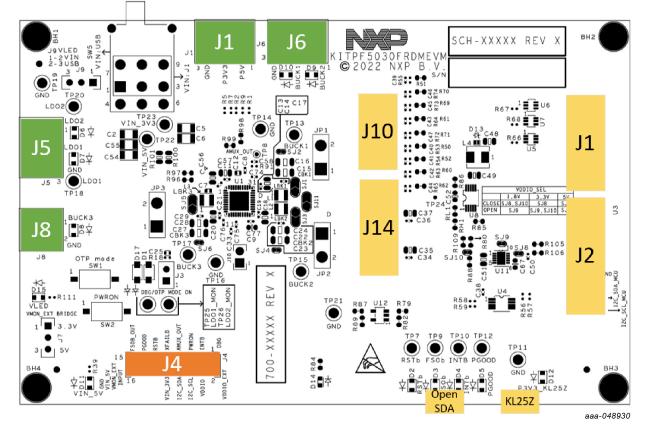


Figure 6. Evaluation board connectors location

## 4.4.1.1 VIN connector (J1)

#### Table 2. VIN\_5V and VIN\_3V3 connector (J1)

Schematic label	Signal name	Description
J1-1	VIN_5V	5 V voltage supply input
J1-2	VIN_3V3	3.3 V voltage supply input
J1-3	GND	Ground

### 4.4.1.2 Output power supply connectors

#### Table 3. LDO1/2 connector (J5)

Schematic label	Signal name	Description
J5-1	LDO2	LDO2 regulator output
J5-2	LDO1	LDO1 regulator output
J5-3	GND	Ground

### KITPF5030FRDMEVM evaluation board

Table 4. BUCK1/2 connector (J6)		
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Schematic label	Signal name	Description
J6-1	BUCK2	BUCK2 regulator output
J6-2	BUCK1	BUCK1 regulator output
J6-3	GND	Ground

#### Table 5. BUCK3 connector (J8)

Schematic label	Signal name	Description
J8-1	BUCK3	BUCK3 regulator output
J8-2	GND	Ground

## 4.4.1.3 Debug connector (J4)

able 6. Debug connector (J4)			
Schematic label	Signal name	Description	
J4-1	n.c.	Not connected	
J4-2	VDDIO_EXT	External VDDIO voltage supply	
J4-3	INTB	Interrupt output pin (active low)	
J4-4	n.c.	Not connected	
J4-5	PWRON	PWRON input pin	
J4-6	I2C_SCL	l <sup>2</sup> C serial clock	
J4-7	AMUX_OUT	Analog multiplexer output	
J4-8	I2C_SDA	l <sup>2</sup> C serial data	
J4-9	n.c.	Not connected	
J4-10	VIN_3V3	VIN_3V3 voltage supply	
J4-11	n.c.	Not connected	
J4-12	VMON_EXT_INPUT	VMON_EXT voltage divider input	
J4-13	n.c.	Not connected	
J4-14	VIN_5V	VIN_5V voltage supply	
J4-15	n.c.	Not connected	
J4-16	GND	Ground	

### 4.4.1.4 FRDM-KL25Z board connectors

### Table 7. FRDM-KL25Z safety output connector (J1)

Schematic label	Signal name	Description
J1-1 to J1-9	n.c.	Not connected
J1-6	INTB_MCU	Interruption (active low-logic level)
J1-7	n.c.	Not connected
J1-8	RSTB_MCU	Reset (active low-logic level)

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### KITPF5030FRDMEVM evaluation board

Schematic label	Signal name	Description
J1-9 to J1-11	n.c.	Not connected
J1-12	FS0b_MCU	Fail-safe (active low-logic level)
J1-13 to J1-16	n.c.	Not connected

#### Table 7 EDDM KI 257 asfaty autput a otor (11)

## Table 8. FRDM-KL25Z I<sup>2</sup>C connector (J2)

Schematic label	Signal name	Description
J2-1 to J2-13	n.c.	Not connected
J2-14	GND	Ground
J2-15 to J2-17	n.c.	Not connected
J2-18	I2C_SDA_MCU	I <sup>2</sup> C serial data line
J2-19	n.c.	Not connected
J2-20	I2C_SCL_MCU	I <sup>2</sup> C serial clock line

### Table 9. FRDM-KL25Z ADC connector (J10)

Schematic label	Signal name	Description
J10-1	BUCK2_ADC	BUCK2 regulator output to KL25Z ADC
J10-2	DBG_ADC	DBG pin voltage to KL25Z ADC
J10-3	BUCK1_ADC	BUCK1 regulator output to KL25Z ADC
J10-4	AMUX_ADC	AMUX pin to KL25Z ADC
J10-5	BUCK3_ADC	BUCK3 regulator output to KL25Z ADC
J10-6	LDO1_ADC	LDO1 regulator output to KL25Z ADC
J10-7	n.c.	Not connected
J10-8	LDO2_ADC	LDO2 regulator output to KL25Z ADC
J10-9	n.c.	Not connected
J10-10	VIN_ADC	VIN pin voltage to KL25Z ADC
J10-11	n.c.	Not connected
J10-12	VDDIO_ADC	VDDIO pin voltage to KL25Z ADC

## Table 10. FRDM-KL25Z supply connector (J14)

Schematic label	Signal name	Description
J14-1 to J14-3	n.c.	Not connected
J14-4	P3V3_KL25Z	3.3 V generated from KL25Z
J14-5 to J14-7	n.c.	Not connected
J14-8	P3V3_KL25Z	3.3 V generated from KL25Z
J14-9	n.c.	Not connected

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#### KITPF5030FRDMEVM evaluation board

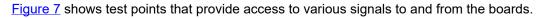
Schematic label	Signal name	Description
J14-10	P5V_KL25Z	5.0 V generated from USB
J14-11	n.c.	Not connected
J14-12	GND	Ground
J14-13	n.c.	Not connected
J14-14	GND	Ground
J14-15	n.c.	Not connected
J14-16	n.c.	not connected

#### Table 10. FRDM-KL25Z supply connector (J14)...continued

#### Table 11. FRDM-KL25Z USB connectors

Schematic label	Signal name	Description
KL25Z	NA	USB connector used to communicate with the PF5030 part
OpenSDA	NA	USB connector used to flash the KL25Z MCU

## 4.4.2 Test points



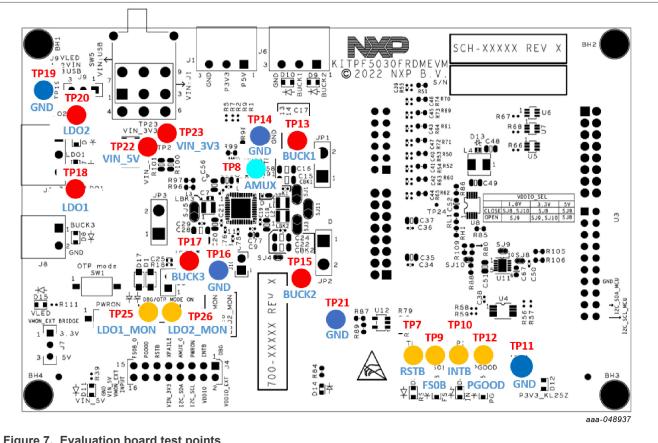


Figure 7. Evaluation board test points

## KITPF5030FRDMEVM evaluation board

Test point name	Signal name	Description
TP7	RSTB	Reset pin (active low)
TP8	AMUX	Analog multiplexer output
TP9	FS0B	Fail-safe pin (active low)
TP10	INTB	Interruption pin (active low)
TP12	PGOOD	Power good pin (active high)
TP13	BUCK1	BUCK1 regulator output
TP15	BUCK2	BUCK2 regulator output
TP17	BUCK3	BUCK3 regulator output
TP18	LDO1	LDO1 regulator output
TP20	LDO2	LDO2 regulator output
TP22	VIN_5V	VIN pin voltage
TP23	VIN_3V3	BUCK1/2_IN pin voltage
TP25	LDO1_MON	LDO1_MON pin voltage
TP26	LDO2_MON	LDO2_MON pin voltage
TP11, TP14, TP16, TP19, TP21	GND	Ground

#### Table 12. Evaluation board test points description

## 4.4.3 Jumpers

Figure 8 shows jumper locations for board configuration.

## KITPF5030FRDMEVM evaluation board

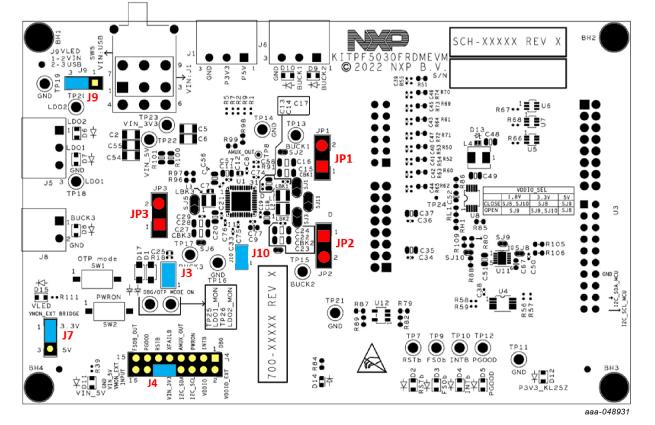


Figure 8. Evaluation board jumpers location (with default position)

Table 13.	Evaluation	board	jumpers	description
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Function	Pin number	Description		
Apply voltage to DBG pin	1-2	Either 4.5 V (DBG mode) or 7.95 V (OTP / test mode). See SW1 position		
4 VMON_EXT input selection		VIN_3V3		
	12-14	VIN_5V		
VLED selection	1-2	VIN_3V3		
	2-3	P3V3_KL25Z		
VMON_EXT resistor bridge	1-2	Monitors 3.3 V		
selection	2-3	Monitors 5.0 V		
FS0B pull-up jumper	1-2	FS0B pull-up connection to VDDIO or another rail		
BUCK1 inductor jumper	1-2	BUCK1 inductor current measurement		
BUCK2 inductor jumper	1-2	BUCK2 inductor current measurement		
BUCK3 inductor jumper	1-2	BUCK3 inductor current measurement		
	Apply voltage to DBG pin         VMON_EXT input selection         VLED selection         VMON_EXT resistor bridge selection         FS0B pull-up jumper         BUCK1 inductor jumper         BUCK2 inductor jumper	Apply voltage to DBG pin1–2VMON_EXT input selection10–1212–1412–14VLED selection1–22–32–3VMON_EXT resistor bridge selection1–22–32–3FS0B pull-up jumper1–2BUCK1 inductor jumper1–2BUCK2 inductor jumper1–2		

### 4.4.4 LED signaling

Figure 9 shows the LEDs provided as visual output devices for the evaluation board:

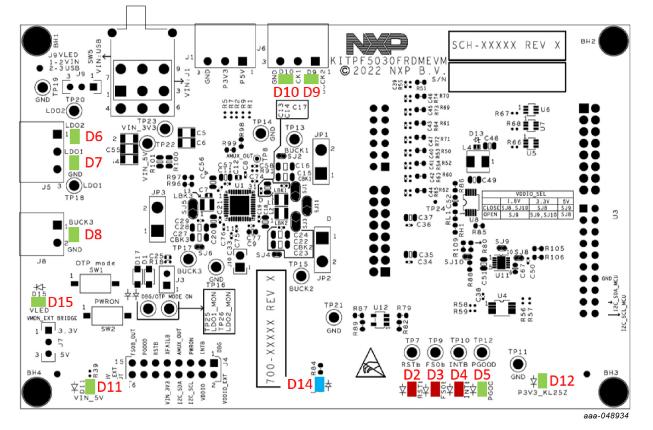


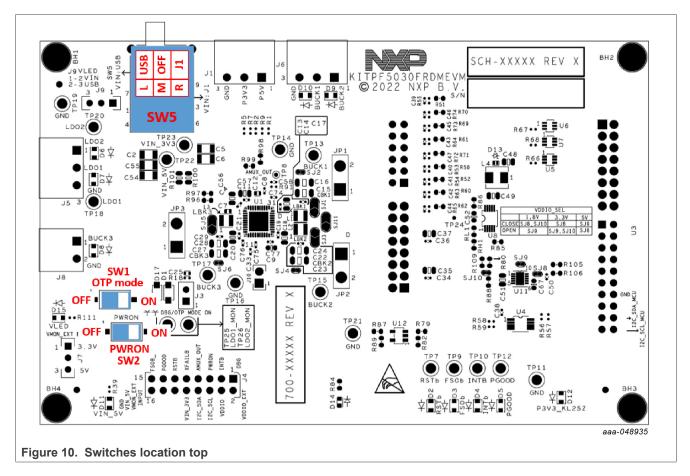
Figure 9. Evaluation board LED signaling location

#### Table 14. Evaluation board LED signaling description

Label	Name	Color	Description
D2	RSTB	Red	RSTB asserted (low-logic level)
D3	FS0B	Red	FS0B asserted (low-logic level)
D4	INTB	Red	INTB asserted (low-logic level)
D5	PGOOD	Green	PGOOD released
D6	LDO2	Green	LDO2 ON
D7	LDO1	Green	LDO1 ON
D8	BUCK3	Green	BUCK3 ON
D9	BUCK2	Green	BUCK2 ON
D10	BUCK1	Green	BUCK1 ON
D11	VIN_5V	Green	VIN_5V ON
D12	P3V3_KL25Z	Green	P3V3_KL25Z ON
D14	DBG ≥ 7.85 V	Blue	DBG pin voltage ≥ 7.85 V (OTP programming)
D15	VLED	Green	VLED ON

### 4.4.5 Switches

Figure 10 and Figure 11 show switches locations for board operation.



## KITPF5030FRDMEVM evaluation board

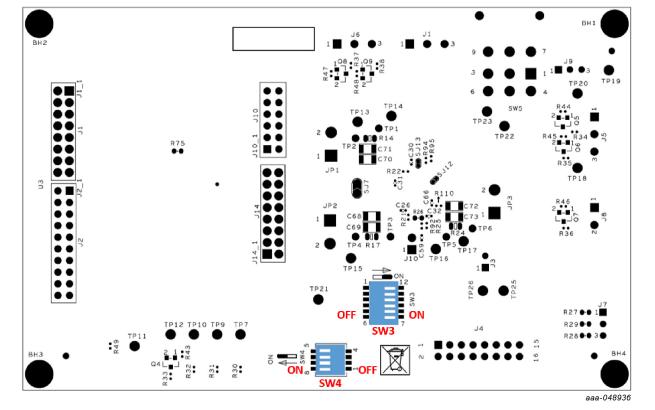


Figure 11. Switches location bottom

### Table 15. SW1 description

Position	Function	Description
RIGHT		PF5030 OTP can be emulated and programmed when J3 populated
LEFT		PF5030 OTP cannot be emulated and programmed

#### Table 16. SW2 description

Position	Function	Description
RIGHT	PWRON pin high	PF5030 can power up
LEFT	PWRON pin low	PF5030 cannot power up

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Switch number	Voltage rail	LED	Description		
1	VIN_5V	D11			
2	BUCK1	D10	Each LED is connected through an independent switch. Disconnecting		
3	BUCK2	D9	them allows more accurate efficiency measurement. The switches also disconnect the FRDM-KL25Z ADC inputs.		
4	BUCK3	D8			
5	LDO1	D7			
6	LDO2	D6			

#### Table 17. SW3 description

#### Table 18. SW4 description

Position	Device output	LED	Description	
1	PGOOD	D5	Each LED is connected through an	
2	INTB	D4	independent switch. Disconnecting them allows more accurate	
3	FS0B	D3	efficiency measurement.	
4	RSTB	D2	The switches also disconnect the level shifters to the FRDM-KL25Z inputs.	

#### Table 19. SW5 description

Position	Function	Description
RIGHT	VIN ON	PF5030 supplied from USB
MIDDLE	VIN OFF	PF5030 not supplied
LEFT	VIN ON	PF5030 supplied from J1

## 5 Installing and configuring software and tools

The programming/evaluation boards are always delivered with the GUI firmware already flashed. If MCU firmware is already flashed, you can ignore this section. If it is specified that firmware must be updated or it is malfunctioning, follow these instructions.

## 5.1 Flashing or updating the FRDM-KL25Z GUI firmware

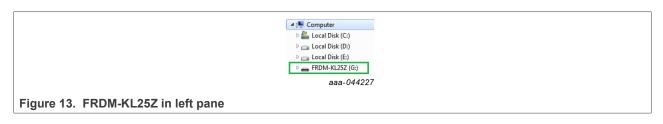
If bootloader is already loaded in the FRDM-KL25Z board, steps 1-3 are not required. Start from step 4.

1. Disable the Storage Service and Windows Search: Run Services, double click, and stop them as shown in Figure 12.

#### KITPF5030FRDMEVM evaluation board

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	Stop the service	Server	Supports fil	Running	Automatic	Loc	Stop	the service		Optimizes p	Running	Manual	Loc
	Distance	Shared PC Account Manager	Manages pr		Disabled	Loc	Library	and service	Windows Push Notification	This service	Running	Automatic	Loc
		Shell Hardware Detection	Provides no	Running	Automatic	Loc			Windows Push Notification	This service	Running	Automatic	Loc
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		SSDP Discovery	Discovers n		Disabled	Loc			Work Folders	This service		Manual	Loc
		State Repository Service	Provides re	Running	Manual	Loc			Workstation	Creates and	Running	Automatic	Net
		Still Image Acquisition Events	Launches a		Manual	Loc			WWAN AutoConfig	This service		Manual	Loc
		Storage Service	Provides en	Running	Manual (Trig	Loc			Xbox Accessory Manageme	This service		Manual	Loc
		Storage Tiers Management	Optimizes t		Manual	Loc			Abox Game Monitoring	This service		Manual (Trig	Loc
		Superfetch	Maintains a	Running	Automatic	Loc			Abox Live Auth Manager	Provides au		Manual	Loc
		Symantec Endpoint Protecti	Provides m	Running	Automatic	Loc			Abox Live Game Save	This service		Manual (Trig	Loc
		Symantec Network Access	Checks that		Manual	Loc			Abox Live Networking Service	This service		Manual	Loc
		Sync Host_15c8b4	This service	Running	Automatic (D	Loc Y							•
		<				>			<				>
	Extended Standard						Exter	nded Standard					
1 m m m													
												aaa-04	422

- 2. Press the RST push button and connect the USB cable to the SDA port on the FRDM-KL25Z board.
  - A new "bootloader" device appears on the left pane of the file explorer
- 3. Drag and drop the file "MSD-DEBUG-FRDM-KL25Z\_Pemicro\_v118.SDA" to the bootloader drive Ensure that there is enough time for the firmware to be saved in the bootloader
- 4. Disconnect the USB cable, then reconnect it to the SDA port **WITHOUT** pressing the RST push button
  - This time, FRDM\_KL25Z device appears on the left pane of the file explorer as in Figure 13.



- 5. Locate the file "nxp-gui-fw-frdmkl25z-usb\_hid-device\_<version>.bin" from the package. Drag and drop this file into the FRDM\_KL25Z device.
- Ensure that there is enough time for the firmware to be saved.
- 6. Freedom board firmware is successfully loaded. Disconnect the USB-cable and reconnect it to the KL25Z USB port.

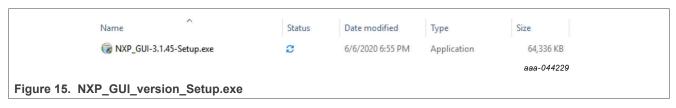
## 5.2 Installing NXP GUI software package

To install the "NXP GUI for Automotive PMIC Families" or obtain the NXP GUI package, unzip an open "1 - NXP\_GUI\_Setup" folder as shown in Figure 14.

Name	Status	Date modified	Туре	Size
0 - Documentation	$\odot$	6/8/2020 10:57 AM	File folder	
1 - NXP_GUI_Setup	S	6/8/2020 5:26 PM	File folder	
2 - KL25Z_FW	$\odot$	6/4/2020 1:42 PM	File folder	
LICENSE.txt	$\odot$	6/4/2020 11:14 AM	Text Document	3 KB
				aaa-044228
Figure 14. NXP_GUI_Setup folder				

### KITPF5030FRDMEVM evaluation board

Then double click on the "NXP\_GUI-version-Setup.exe" shown in Figure 15 and follow the instructions.



To install the application on Windows PC, proceed with the pop-up windows shown in Figure 16 and Figure 17.

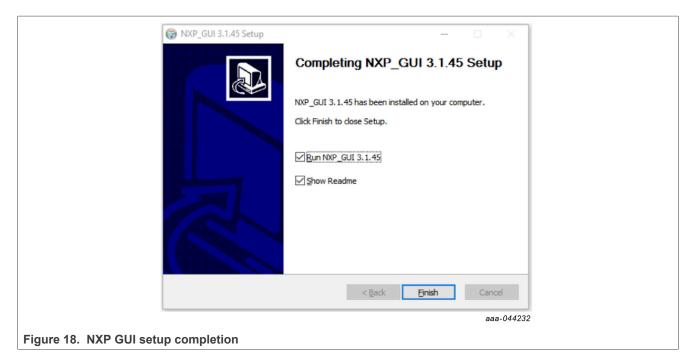
Welcom	e to NXP_GUI 3.1.45 Setup	WXP_GUI 3.1.45 Setup     -     ×       License Agreement     Please review the license terms before installing NXP_GUI 3.1.45.     Image: Comparison of the line of the lin
3.1.45. It is recomme before startin	le you through the installation of NXP_GUI nded that you close all other applications g Setup. This will make it possible to update em files without having to reboot your continue.	Press Page Down to see the rest of the agreement.
	Next > Cancel	< Back I Agree Cancel

NXP_GUI 3.1.45 Setup		- · ×	Choose Install Location
Choose which features of NXI	P_GUI 3.1.45 you want to ins	tall.	Choose the folder in which to install NXP_GUI 3.1.45.
Check the components you w install. Click Next to continue.		components you don't want to	Setup will install NVP_GUI 3.1.45 in the following folder. To install in a different folder, click Browse and select another folder. Click Install to start the installation.
Select components to install:	MainSection Optional	Description Position your mouse over a component to see its description.	Destination Folder           E::         Program Files (x85) \\\\PGUI\\         Browse
Space required: 164.4 MB			Space required: 164.4 MB Space available: 26.9 GB
illsoft Install System v3.05			Nulsoft Install System v3.05
	< Back	Next > Cancel	< Back Install Cancel

Select the options shown in Figure 18 before completing the installation of the setup:

- Run NXP\_GUI
- Show Readme

#### KITPF5030FRDMEVM evaluation board



Select Finish to complete the installation.

When installation is finished, you can search the application on the Windows search bar as "NXPGUI". Click to launch.

## 6 Using PF5030 NXP GUI

To follow the steps in this section, ensure that the board is connected using the appropriate hardware configuration.

Always use the latest version of the NXP GUI.

## 6.1 Starting the PF5030 NXP GUI

When your kit is ready and the NXP GUI is installed, click to launch the GUI from your Windows search bar. When the kit selection window appears, as shown in Figure 19, select PF5030.

#### KITPF5030FRDMEVM evaluation board

NP Kit Sele	ection	×
Select the Kit and Devic	e kit,on board device(s), target MCU and USB interface	e
PF	7100	^
✓ KITFS2	:6	
FS2	26	
✓ KITFS5	600	
FS:	5600	
✓ KITFS8	600	_
FS	8600	
✓ KITPF5		Ŧ
	PMIC evaluation	
Advanced Se	ettings	
Feature Set	t debug-i2c	
Target MCU	J FRDM-KL25Z	
USB Interfa	ace usb-hid	
Use this	configuration and Donot ask again!	
	OK Cance	el
<u>.</u>	aaa-044	4225
ection window		

To avoid the kit selection window on every launch, you can check the box "Use this configuration and do not ask again". The window shown in <u>Figure 20</u> opens.

	Settings I(DEV_build)-F59000-3.1.233	Device Mana	.0-1							- 🗆 ×
	DO Start Test Mode Exit OTP I	Made 🗢 🗢 12C Freque	ency(KHz):400 M		C - Fail Cafe	ADD: [0.5 a]] I	Enable WatchD	ng Defrech 🗔	Period 3 ms	DEV_build
	og Window 비원	III Register Map		Ø Diag Safety		© Regulators			Period 13 ms	
POWER	Filter Messages 👻 🛃 👔	Functional	M_FLAG (0x0		0x0000		x0000			-
OTP		Safety Write_INIT_Safety	COM_ERR	WU_G	VPRE_G	BOOST_G	RESERVED	RESERVED	VBUCK_G	VLDO1_G
PROG			VLDO2_G	VSUP_G	RESERVED	RESERVED	RESERVED	RESERVED	IZC_M_CRC	IZC_M_REQ
<>	IOB		rent	A) Read	0x0000	Write	0x0000	2		
SCRPT EARPEOR	Window LOB	12		VSUP_O V_CFG	FOUT_STATE	INTB_REQ	M_OTP_EXIT	RESERVED	EXT_FIN_SEL	PLL_LOCK_RT
ACCESS	1.	10	EXT_FIN_ SEL_RT	EXT_FIN_DIS	MAIN_N ORMAL	RESERVED	RESERVED	W2DIS	W1DIS	GOTOSTBY
- Charles			M_REG_CTRL	.1 (0x02)	Read 0x000	00 Write	e 0x0000			
Bar -			VPRE_PD_DIS	VPREDIS	BOOSTDIS	RESERVED	RESERVED	BUCKDIS	LDO1DI5	LDO2DIS
			RESERVED	VPREEN	BOOSTEN	RESERVED	RESERVED	BUCKEN	LDO1EN	LDO2EN
č			M_REG_CTRL	2 (0x03)	Read 0x000	00 Write	e 0x0000			
Tool Access			BOOSTSR[1]	BOOSTSR[0]	BOOSTT SDCFG	RESERVED	RESERVED	BUCKTSDCFG	LDO1TSDCFG	LDO2TSDCFG
T00			VPRESRHS_ RISE[1]	VPRESRHS_ RISE[0]	RESERVED	VPRESRLS[1]	VPRESRLS[0]	RESERVED	VPRESRHS_ FALL[1]	VPRESRHS_ FALL[0]
			Select All M		- (19)	Read Wr				
CU: FRDM-	-KL25Z State: NOT DETECTED Protoc					FS CURRENT STATE :	Undefined			24/09/2021 16:55:38
		Mici	ro and De	vice Sta	tus					aaa-044233

You are now using the PF5030 GUI interface. It can be divided in several parts:

- Settings: Import or export files, configure framework.
- Device Manager: Start communication with device. Enter or exit test mode. I<sup>2</sup>C communication settings.
- **Tool Access Bar:** Quick access to the PF5030 evaluation tools and features.
- Window Log: Microcontroller and device communication events.
- Tab Content: Content of each tool or tab. There can be more tabs, boxes, or windows.

• **Micro and Device Status:** Indicates if the computer USB is connected to the kit. Displays firmware and GUI version. Displays the current state of the fail-safe state machine. Click Display button to refresh.

**Note:** The tool access bar shows the GUI tools in the sequence that they must be used. The first step is to verify device POWER dissipation and then configure the OTP. When the power is verified and OTP is done, the device can be programmed or emulated with a SCRIPT. MIRROR registers can be read/modified to a configuration validation. To verify states and configure safety reactions, the Access tab allows registers handling.

## 6.2 Power tab

NXP GUI ( DEV\_build ) - FS8600 - 3.1.233 File View Export NXP Help DEV build FS8600 Start Test Mode Exit OTP Mode 🖒 💭 I2C Frequency(KHz):400 Main ADD: 0x2 \* Fail Safe ADD: 0x2 \* Enable WatchDog Refresh 🗆 Period 3 NP System Power Dissipation IC Power Dissipation Import OTP Config Import Mirror Config Load Power Config Save Power Config INPUT PARAMETERS VPRE VBOOST BUCK 7 INPUT Main Supply \* INPUT VPRE INPUT VPRE v Main Supply 12 \* V VOUT 5.0 VOUT VOUT 1.8 - V 6 V Main Current 2,479 A IOUT IOUT A 0.5 A IOUT 1.5 A FSW1 455 KH<sub>7</sub> ISYS 0.113 0.000 1.572 A ISYS ISYS A Α <> FSW2 2220 KHz FREQ 2220 KHz FREQ 2220 KHZ FREQ 455 • KHz Total POUT 27.86 w Total POUT 3.68 w POUT 2.70 w THERMAL CHARACTERISTICS Chip Loss 59.2 mW Chip Loss 214.4 mW Chip Los 302.1 mW T Ambient 27 °C 0 Ext Loss 1831.4 mW Ext Loss 330.5 mW Ext Loss 133.0 mW T Junction 57.95 °C Eff 93.65 % Eff 87.11 % 86.12 % OPTIONS \* RØJA 23 °C/W OPTIONS ENABLED OPTIONS ENABLED ENABLED LD01 LD02 SYSTEM POWER DISSIPATION -VPRE \* INPUT VBOOST INPUT External Loss 2295 mW - V VOUT VOUT 1.5 1.8 - V SWs Loss 576 mW IOUT 0.1 A IOUT 0.1 Α 770 0,150 0 180 LDOs Loss POUT w mW POUT w PMIC Power 1346 mW PLOSS 350 mW PLOSS 420 mW nSYSTEM 87.934 % OPTIONS ENABLED OPTIONS **ENABLED** MCU: FRDM-KL25Z State: DISCONNECTED Protocol: I<sup>C</sup>C Hirmware: Application 3.1.233 Device Mode: user-mode Color legend: High 🛑 Low 🛑 FS CURRENT STATE : Undefi 24/09/2021 16:55:38 aaa-044234

The POWER tool allows the calculation of power management power dissipation.

Figure 21. NXP GUI framework - POWER tab

VPRE external MOSFET parameters can be added on the VPRE > OPTIONS > EXTERNAL MOSFET SELECTION option and then chosen with VPRE > OPTIONS > COMPONENT SELECTION. Special care must be given to MOSFET thermal resistance.

COMPONENT SELECTION is also available for BOOST and BUCK regulators. Components values are required for power dissipation calculation.

## 6.3 OTP tab

The OTP tool allows the configuration of OTP registers and generates scripts for OTP emulation or OTP programming. These scripts program parameters that the main state machine and the fail-safe state machine control.

The OTP tool includes four tabs:

- System Configuration
- Switching and LDO Regulators
- Functional Safety

Calculator

These four tabs are used to define the entire FS86 OTP configuration.

When the OTP configuration is defined, TBB/OTP scripts can be generated using the Export menu. Generate a TBB file for emulation and an OTP file for OTP programming.

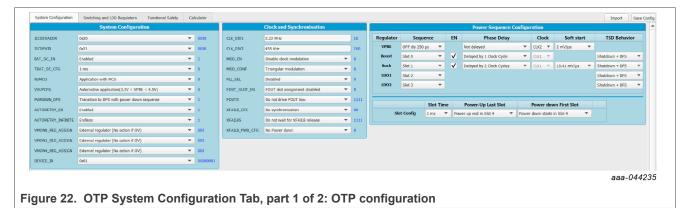
It is possible to save a configuration to use or modify it later. To export the OTP configuration, click save config. To import a configuration initially saved from the OTP tool or the Mirrors tab, click the Import button.

### 6.3.1 System configuration tab

The system configuration tab has several sections, divided into two groups. The first group is related to OTP configuration itself:

- System Configuration: I<sup>2</sup>C, battery switch, auto retry...
- Clock and Synchronization: Clocks, modulation, FOUT, XFAILB...
- **Power Sequence Configuration**: This box is used to define the power sequence of the device. If the configuration is modified, the power-up sequence graph is updated automatically.

Figure 22 shows an OTP configuration example.

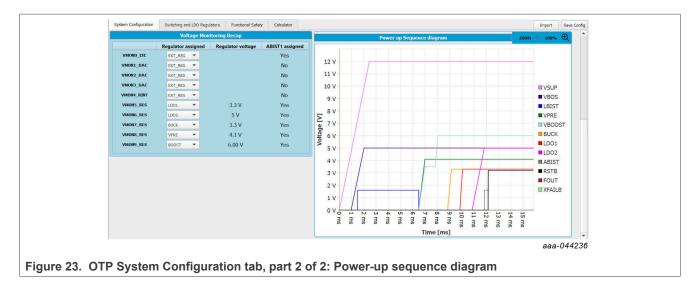


The second group is related to VMON board connection and start-up sequence diagram:

- Voltage monitoring recap for power-up sequence diagram drawing: This box is NOT related to the OTP configuration. It allows the definition of an assignment between the VMONx and the regulators to plot the power-up sequence graph. It does not configure any registers. It is only used as information. It is saved as comment on the configuration script.
- Power-up sequence diagram: This diagram reflects the power-up sequence of the FS8600 depending on the OTP configuration. To plot the associated configuration, it uses the "Voltage Monitoring Recap". The power-up sequence timing may not be 100 % accurate. If shown, the RSTB, the FOUT, and the XFAILB voltages are different from 3.3 V to differentiate between the different curves. The VSUP input voltage is set to 12 V.

Figure 23 shows a voltage monitoring recap connection and the resulting power-up sequence diagram.

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### 6.3.2 Switching and LDO regulators tab

The switching and LDO Regulators tab shown in <u>Figure 24</u> has several sections:

- Block diagram: Summarize the output voltages of each regulator
- **VPRE configuration**: Minimum ON and OFF time and the low-side slew rate are set and cannot be modified. Other parameters can be chosen.
- VBOOST configuration: VBOOST minimum ontime is already set. Other parameters can be chosen.
- **BUCK configuration**: Overall configuration available. Depending on the output voltage value, the transconductance value is updated automatically.
- LDO1/LDO2 configuration: Linear dropout configuration



Figure 24. OTP SMPS and LDO regulators Configuration tab

### 6.3.3 Functional safety tab

The functional safety tab shown in Figure 25 has several sections:

- System Safety Configuration: Watchdog, FCCU, ERRMON, RSTB...
- Voltage Monitoring: Define the voltage monitoring configuration. Some protections have been implemented to avoid any OTP configuration issue.

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	System Safety Configuration							Voltage Mo	itorina							
					1											
RRMON_EN	Disabled	• 0		EN	Voltage	UV	тн	OV TH	UV Deb	ounce	OV Debo	ince	PG00D Ctrl		ABIST1 Assignm	ent
CCU_EN	Disabled	• 0	VMON0_I2C	~	3.3 V 🔹	90.0	% *	110.0% *	25 µs	٣	25 µs	*	Assigned	*	Assigned	*
VD_DIS	Watchdog monitoring enabled	• 0	VMON1_DAC		1.4 V 🔹	90.0	% •	110.0% -	25 µs	۳	25 µs	*	Not assigned	Ŧ	Not assigned	٣
VD_SELECTION	Challenger watchdog	• 1	VMON2_DAC		0.7 V -	90.0	% *	110.0% *	25 µs	*	25 µs	*	Not assigned	*	Not assigned	٣
LT RECOVERY EN	Disabled	• 0	VMON3_DAC		0.7 V 🔹	90.0	% •	110.0% -	25 µs		25 µs	*	Not assigned	-	Not assigned	*
STB_8s_DIS	Counter enabled	<b>v</b> 0	VMON4_RINT		1.8 V -	90.0	% *	110.0% -	25 µs	٣	25 µs	٣	Not assigned	Ŧ	Not assigned	٣
STB DLY	No delay	<b>v</b> 0	VMON5_RES	V	0.8 V	90.0	% •	110.0% -	25 µs	•	25 µs	*	Assigned	٣	Assigned	٠
STB2PGOOD	Fault asserting RSTb won't assert PGOOD	-	VMON6_RES	V	0.8 V	90.0	% •	110.0% -	25 µs	٣	25 µs	*	Assigned	٣	Assigned	٠
			VMON7_RES	V	0.8 V	90.0	% -	110.0% -	25 µs	*	25 µs	-	Assigned	-	Assigned	-
MON123_SVS_CLAMP	No SVS	• 00000	VMON8_RES	V	0.8 V	90.0	% *	110.0% -	25 µs		25 µs	-	Assigned	-	Assigned	•
			VMON9_RES	V	0.8 V	90.0	% •	110.0% -	25 µs	*	25 µs	-	Assigned	-	Assigned	*

Figure 25. OTP Functional Safety tab

### 6.4 Establishing the connection between the NXP GUI and the hardware

The device manager allows the connection of the FS86 development board with the NXP GUI.

Before plugging the KL25Z USB port USB to the computer, the MCU is in a "NOT DETECTED" state.

MCU: FRDM-KL25Z State: NOT DETECTED	Protocol: I <sup>2</sup> C Firmware:	Application 3.1.140 Device Mode: user-mode
		aaa-044252

After plugging in the USB, the MCU state changes to "DISCONNECTED". If the state does not change, press the RST button on the freedom board.

At this state, the communication with the MCU can be started.

aaa-044255

The MCU state changes to "CONNECTED" and the firmware version is displayed.

To start the communication with the FS8600, click the "START" button.

xit OTP Mode 🗂 💭 I2C Frequency(KHz):400 Main ADD: 0x20 🗸 Fail Safe ADD: 0x2 🗸 FS8600 Start aaa-044257

When the communication has started successfully, the FS8600 switches to Green.

 FS8600
 Stop
 Test Mode
 Exit OTP Mode
 Inc.
 Inc.
 Fail Safe ADD:
 Ox2 •

 saa-044258

When the device starts with the DBG pin voltage at 8 V (on the EVBs: SW3 ON, DBG jumper populated, OTP mode led ON), the state machine stops at the M/FS\_LOAD\_OTP state.

The current mode can be read using the refresh button and loop refresh button highlighted in red. Clicking Refresh reads the state one time. Clicking the loop refresh latches and reads the state periodically until a new click deactivates it.

When the "Exit OTP mode" button is green, the device is in OTP mode. An "Exit OTP mode" button click sends commands to the main state and the fail-safe state machine to exit OTP mode and device start-up.

FS8600 Stop Test Mode Exit OTP Mode 🗠 💭 I2C Frequency(KHz): 400 Main ADD: 0x2 - Fail Safe ADD: 0x2 - aaa-044259

The user can switch from User mode to Test mode (and vice versa) by clicking the Test Mode button when DBG pin voltage is 8 V (on the EVBs: SW3 ON, DBG jumper populated, OTP mode led ON). When the button is green, Test mode is activated. The button state can also be refreshed.



The current device mode is shown on the device status bar. When in Test mode, the device is necessarily in Debug mode. Test mode can be entered when device is not in OTP mode.

**Note:** With I<sup>2</sup>C, most of the time, the default addresses the device uses are 0x20 for main and 0x21 for fail-safe.

The I<sup>2</sup>C address is managed differently in Debug mode and User mode.

### 6.5 OTP mode and device programming

Device enters OTP mode when the DBG pin voltage is set to 7.95 V before start-up. The OTP mode consists of a device state machine stop at Main/FS OTP MODE states. When in Main/FS OTP mode states, the  $I^2C$  addresses are 0x20 for main and 0x21 for fail-safe. The Main/FS OTP mode states are left when one of these conditions is met:

- Imposing DBG pin voltage inferior to 5.5 V
- Sending Main/FS OTP mode exit command through I<sup>2</sup>C
- Clicking NXP GUI button "Exit OTP Mode"

The NXP GUI is able to identify these addresses automatically from the device.

Then, the device addresses are set based on the mirror registers values. User can only change these addresses in the mirror register in Test mode.

#### 6.5.1 Device programming

The Device Programming tab shown in <u>Figure 26</u> allows OTP device programming using a file initially generated by the OTP tool. This tab is only available when **Test mode** is active.

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Device Programming Conf           Select TBB/OTP File         Brite           File Name         Not Select           Status         Not Ready           Program         Reset	bowse ted /	FS   Mai	OTP Mode Exit OTP Mode Exit OTP Mode RT OTP Mode RT OTP Mode Exit OTP Mode Exit Read Write
	Fuse E	lox Status	
Main Programming Status	Main Sector Flags	FailSafe Programming Status	FailSafe Sector Flags
BUSYERRORONE_ERRTWO_ERRMAX_PGM_EXCEEDVRR_CHECK_TRIESPGM_FAIL_WPBOOT_ERRORVRR_ERRORBOOT_DONE	Sector 1 Flags CRC BOOT Enable(BE) Write Protected(WP) MTP bit Sector 1bis Flags CRC BOOT Enable(BE) Write Protected(WP) MTP	BUSY Constant of the second se	Sector 1 Flags CRC  BOOT Enable(BE)  Write Protected(WP)  MTP  Sector 1bis Flags CRC  BOOT Enable(BE)  Write Protected(WP)  MTP
		Read	
			aaa-044261

To set up the hardware before OTP burning, see <u>Section 7.3</u> configure put device in OTP mode, then follow the steps:

- Start the device in **OTP mode**.
- Enter Test mode.
- Browse and load the script file you want to burn (OTP or TBB type).
- The program button is available.
- Click Program.

Before programming, the GUI verifies if the DBG pin voltage is 7.95 V.

If the DBG pin voltage is less than 7.95 V, a pop-up window is shown requiring to turn on the 7.95 V. The blue LED on the board indicates that an 7.95 V voltage is available on the DBG pin. At the end of the first OTP programming, the MTP index = 1, WP, BE, and CRC flags are orange.

The Main/Fail-safe sector flags provide the OTP fuse status, as shown in <u>Table 20</u>. It helps to determine how many times the part was burned.

 Table 20. OTP burning flag status

OTP burning step	Sector	BE	WP	CRC	MTP index
mirrors empty, OTP not burned	1	blue	blue	blue	orange
	1bis	blue	blue	blue	blue
mirrors filled, OTP not burned	1	blue	blue	orange	orange
	1bis	blue	blue	orange	blue
OTP burned once	1	orange	orange	orange	orange
OTP burned twice	1bis	orange	orange	orange	orange

The example shown in Figure 26 corresponds to the OTP not burned, mirrors empty line in Table 20.

To check if a valid OTP configuration is already burned, switch off the supply and then on again. Start the device by clicking the "Exit OTP Mode" button. The device starts with the OTP configuration.

### 6.6 User mode controls

The device operation is called **User mode** when the Main/FS state machines are not in OTP MODE state and not in Test Mode. In this mode, the main/fail-safe addresses come from mirror registers / fused OTP.

When using the EVB, the voltages on device pins can be verified in ACCESS > AMUX > ADC Measurements (see <u>Section 6.6.3.9</u>).

### 6.6.1 Working with the script editor

The register and OTP emulation can be configured with the script editor shown in <u>Figure 27</u>. The script editor is useful for trying various OTP configurations in OTP mode.

Log Window	Device FS8600 Alias FS8600	×	Script Commands Window	Script Resul	ts Window
Sent and Received Commands	Digital Pins     Analog Pins     Analog Pins     Registers     Mnde     Control     Generator	Command Script Editor	Script Text Editor		Script Results
			Management Commands		
					aline and a second s
			IN DOF SHE OFN ILLA HEP	SAVE OPEN	aix

The main subareas of this panel are:

- Command Script Editor: Builds commands to be sent to the device.
- Script Text Editor: Sends a sequence of register configurations from a text file or from a command edited directly in this area.
- Script Results: Displays result status of each command sent to the device.
- Sent and Received Commands: Displays a summary of commands sent and received from the device.
- Management Commands: Used for scripts.

#### 6.6.1.1 Command script editor

Using the script editor, you can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if necessary.

All commands must follow a specific syntax. The Help menu describes the commands available in the script editor and the syntax to be used.

Figure 28 shows an example of building a command from the panel.

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#### 6.6.1.2 Management commands

Some commands are used for formatting the scripts. Figure 29 shows the description of each button.

	RUN LOOP JUE OFFN 8= ? PELP
	aaa-044265
Figure 29. Script editor commands	

- Run: Runs the script once.
- Loop: Runs the script continuously in a loop.
- Save: Save the script that is present in the script command window in text file.
- **Open**: Open a saved script from the desired location.
- ATE: Saves the script in ATE format.
- Clear: Clears the script command window.

• Script Editor Help Window: Describes the commands available in script editor and their formats.

#### 6.6.1.3 Script generator

The script editor allows the user to save script sequence files, as shown in <u>Figure 30</u>. However, a script sequence file is already saved as an example in the script generator. This script is used to release FS0B when the PF5030 is using simple watchdog.

Device FS8600	Script Commands Window	Script Results Window				
Alias FS8600	<ul> <li>SET_REG:FS8600:SAFETY:FS_WD_WINDOW_DUR:0x0208</li> <li>SET_REG:FS8600:SAFETY:FS_NOT_WD_WINDOW_DUR:0xFD04</li> </ul>	OK : Write Register : FS_WD_WINDOW_DUR : 0x020b OK : Write Register : FS_NOT_WD_WINDOW_DUR : 0xfd04				
Digital Pins	SET_REG:FS8600:SAFETY:FS_WD_ANSWER:0x5AB2	OK : Write Register : FS_WD_ANSWER : 0x5ab2				
Analog Pins	SET_REG:FS8600:SAFETY:FS_WD_ANSWER:0x5AB2 SET_REG:FS8600:SAFETY:FS_WD_ANSWER:0x5AB2	OK : Write Register : FS_WD_ANSWER : 0xSab2 OK : Write Register : FS_WD_ANSWER : 0xSab2				
Registers	SET REG:FS8600:SAFETY:FS WD ANSWER:0x5AB2	OK : Write Register : FS_WD_ANSWER : 0x5ab2				
Mode	SET_REG:FS8600:SAFETY:FS_WD_ANSWER:0x5AB2	OK : Write Register : FS_WD_ANSWER : 0xSab2				
Control	SET_REG:FS8600:SAFETY:FS_WD_ANSWER:0x5AB2 SET_REG:FS8600:SAFETY:FS_WD_ANSWER:0x5AB2	OK : Write Register : FS_WD_ANSWER : 0xSab2 OK : Write Register : FS_WD_ANSWER : 0xSab2				
Generator	SET_REG:FS8600:SAFETY:FS_WD_ANSWER:0X5AB2 SET_REG:FS8600:SAFETY:FS_WD_ANSWER:0X5AB2	OK : Write Register : PS_WD_ANSWER : 0x5ab2 OK : Write Register : PS_WD_ANSWER : 0x5ab2				
Generator: FS0B_RELEASE_SIMPLE_WATCHD	SET_REG:FS8600:SAFETY:FS_STATES:0x4000 SET_REG:FS8600:SAFETY:FS_RELEASE_FS08:0x82A5	OK : Write Register : FS_STATES : 0x4000 OK : Write Register : FS_RELEASE_FS0B : 0xb2a5				
Script Generator						
Script Generator		±. €.				
		بل الله الله الله الله الله الله الله ال				

## Figure 30. Script generator

#### 6.6.2 Mirrors tab

Test mode must be applied to enable the Mirrors tab. This tab is divided in main and fail-safe mirrors registers, shown in <u>Figure 31</u> and <u>Figure 32</u>, respectively.

The "Read All" / "Write All" buttons can be used to read/write all the mirror registers. The mirrors configuration content can be exported and imported in the OTP tool as OTP configuration to generate TBB/OTP script files.

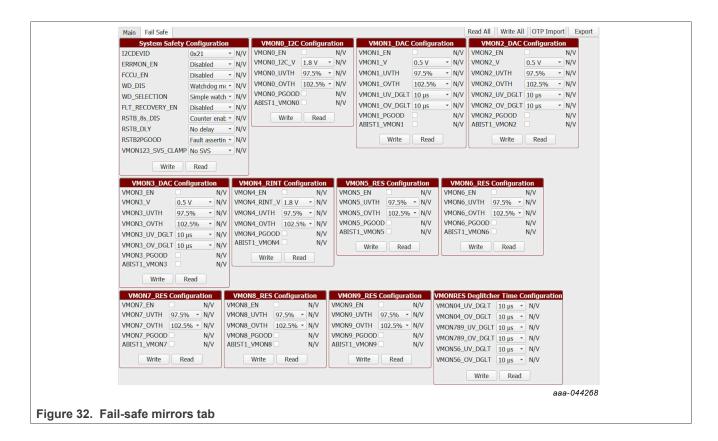
## **NXP Semiconductors**

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System	Configuration	Clock and	Synchronisation	Power Seque	nce Configuration	VPRE	Configuration
I2CDEVADDR	0x20 - N	I/V CLK_DIV1	2.85 MHz • N/	V TSLOT	0.5 ms • N/\	VPRETON	25 ns N/V
BAT_SW_EN	Disabled * N	I/V CLK_DIV2	2.5 MHz * N/	V BOOSTS	Slot 0 • N/\	VPREV	3.3 V • N/V
TBAT_SW_CFG	1 ms • N	I/V MOD_EN	Disable clock - N/	V BUCKS	Slot 0 • N/\	VPRESSRAMP	1 mV/µs • N/V
VSUPCFG	Automotive a * N	I/V MOD_CONF	Triangular m 🝷 N/	V LDO1S	Slot 0 • N/\	VPRESC	21 mV/µs • N/V
PWRDWN_DFS	Transition to • N	I/V PLL_SEL	Disabled • N/	V LDO2S	Slot 0 • N/\	VPREILIM	50 mV - N/V
AUTORETRY_EN	Disabled * N	I/V FOUT_SLOT_EN	FOUT slot as: • N/		Power up enc * N/\		80 ns N/V
AUTORETRY_INFI	NITE 15 times • N	I/V FOUTS	Drive FOUT I * N/	V PWRDWN_FIRSTS	Power down * N/\	VPRESRLS	PU/PD/130 n * N/V
VMON0_REG_ASSI	GN External regu * N	I/V XFAILB_CFG	No synchroni * N/	VWrite	Read	VPRESRHS	PU/PD/130 n * N/V
VMON1_REG_ASSI			Do not wait f - N/	V	Redu	VPRE_CLK_SEL	
VMON4_REG_ASSI	GN External regu * N	I/V XFAILB_PWD_C	FG No Power do * N/	V		VPRE_PH	Not delayed * N/V
DEVICE_ID	0x00 - N	I/V Writ	e Read			VPRE_OFF_DL	' OFF dly 250   * N/V
Write	Read					Write	Read
	onfiguration	BUCK Con		LDO1 Config		LDO2 Con	figuration
BOOSTEN			Disabled - N/V				1.1 V - N/V
BOOSTV	5.00 V - N/V						100 mA - N/V
BOOSTTONTIME	50 ns N/V			CONF_TSD_LDO1 Re	gulator sht - N/V C	ONF_TSD_LDO2	Regulator sht - N/V
BOOSTSC	358 mV/µs • N/V		CLK1 - N/V	Write	Read	Write	Read
BOOSTRCOMP	750 kΩ • N/V		Not delayed   N/V				
	125 pF • N/V		55KΩ - N/V				
BOOSTCCOMP	2 A • N/V		18 μS - N/V				
BOOSTILIM			2.1 A - N/V				
BOOSTILIM BOOSTSR	50 V/µs • N/V						
BOOSTILIM BOOSTSR BOOST_CLK_SEL	CLK1 • N/V	DVS_BUCK	10.41 mV/µs + N/V				
BOOSTILIM BOOSTSR BOOST_CLK_SEL BOOST_PH	CLK1 • N/V Not delayed • N/V		10.41 mV/µs + N/V				
BOOSTILIM BOOSTSR BOOST_CLK_SEL BOOST_PH	CLK1 • N/V	DVS_BUCK	10.41 mV/µs + N/V				

#### Figure 31. Main mirrors tab



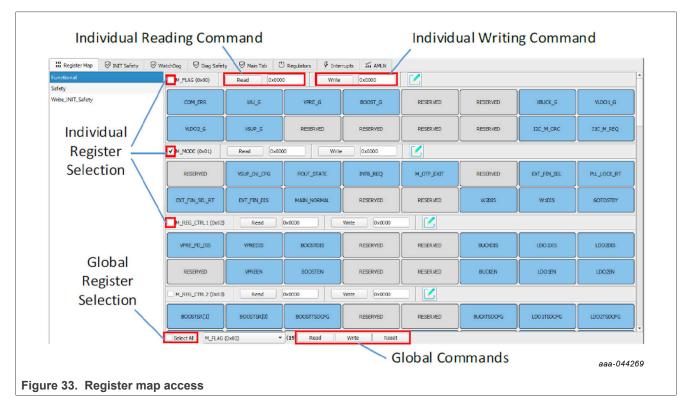
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### 6.6.3 Access tab

#### 6.6.3.1 Register map

All PF5030 I<sup>2</sup>C registers can be accessed in write and read mode using this tab shown in <u>Figure 33</u>. These registers are divided into three sections:

- **Functional**: Main functional I<sup>2</sup>C registers (diagnostics, configuration, and controls)
- **Safety**: Safety I<sup>2</sup>C registers (diagnostics and configuration)
- Write INIT safety: Safety registers that can be written only during initialization phase (INIT\_FS state).



To read the values of a register, click the **READ** button. The value is read from the device and is displayed on a label near the **READ** button. It is also displayed in the log window.

To write the bit values individually, click the desired bit. The corresponding bit button color changes. The value is updated in the log window. Click the WRITE button to write the register. To write the values through a text box near the **WRITE** button, enter the appropriate write value. Then click the **WRITE** button to write the register.

When registers have been selected, global commands can also be used:

- WRITE: Writes data to all the selected register at once.
- **READ**: Reads data back from the selected register at once.
- **RESET**: Resets all the input text boxes to 0x00. Write bits are set to 0. Change register bit buttons are set to the default setting.

The value can also be written by selecting the Edit option near the **WRITE** button. Bits and corresponding values are displayed in a pop window as shown in <u>Figure 34</u>. Select the options of all write bits, close the input dialog box, and click the **WRITE** button. Selected input combinations are written to the register.

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□ M_MODE (0x01) R	ead 0x0000	Write 0x0	000 🛛 🗹					
RESERVED VSUP_OV_	CFG FOUT_STATE	INTB_REQ	M_OTP_	Т	RESERVED	EXT_FIN_SEL	PLL_LOC	CK_RT
EXT_FIN_ SEL_RT EXT_FIN_	DIS MAIN_N ORMAL	RESERVED	RESERV		W2DI5	W1DI5	GOTOS	STBY
MP M_MODE (0x01)	Bit-Map Dialog						х	
Set Value (Ed	Set Value (Editable)			Register Content				
			VSUP_OV_CFG: 30V min - 32V type - 34V max			c		
FOUT_STATE:			FOUT_STATE: Drive FOUT pin low state					
INTB_REQ: M_OTP_EXIT:			PLL_LOCK_RT: PLL not locked EXT_FIN_SEL_RT: Internal dock oscillator is select		tod			
EXT_FIN_sel:				MAIN_NORMAL: State Machine NOT in Normal				
EXT_FIN_DIS:			W2DIS: wake up enabled		mode			
W2DIS:	wake up enabled					wake up enabled		
W1DIS:	wake up enabled							
GOTOSTBY:	Device remains in current state							
							aaa-(	044270
Bitmap dialog							aaa-(	044270

Writing an INIT FS register automatically updates the corresponding NOT register.

### 6.6.3.2 INIT Safety tab

This tab allows the initialization phase (INIT\_FS state) configuration, that must be done before the first good watchdog refresh until the 2 seconds timeout limit.

In this tab, safety features can be configured, such as the safety output reaction when voltage monitoring fault is detected, watchdog refresh counter, fault error counter, as shown in <u>Figure 35</u>. The Analog Built-In Self-Test 2 ABIST2 (used for voltage monitoring assigned to external regulator), the VMON1 Static Voltage Scaling, counters limit, and other INIT\_FS registers are also configurable from this tab. See the PF5030 data sheet for a complete description of these registers.

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To ease the configuration, Read and Write All buttons are implemented.

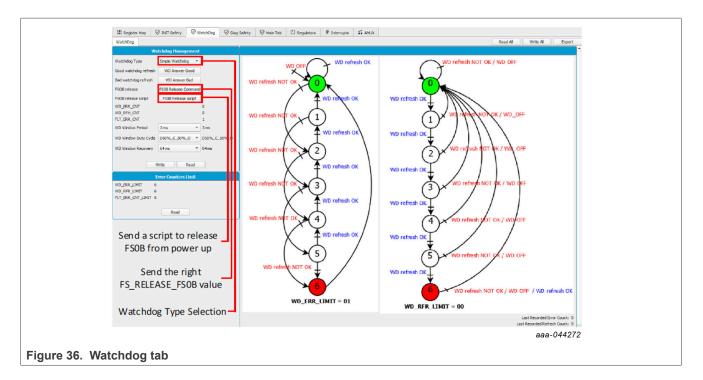
## 6.6.3.3 Watchdog tab

The watchdog tab gathers all the registers and configurations having an impact on the watchdog, except "Watchdog Type". The watchdog error and refresh counters are displayed depending on the limit configuration. Watchdog answers can be generated and sent to the device depending on the watchdog type. The watchdog type configured in the OTP must be manually selected in the drop-down list to explore the watchdog features. If the user is not aware of the type of watchdog configured in the OTP, it can be found in Mirrors tab.

The "FS0B Release Command" calculates and sends the right secure 16-bit word to release FS0B.

A simplified way to release FS0B after power-up is to select the right type of watchdog configured in the OTP and then click the "FS0B Release script" button. This action sends the right sequence to close the initialization sequence, sets the error counter back to 0, and then releases FS0B, shown in <u>Figure 36</u>.

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#### 6.6.3.4 Diagnostic Safety tab

The diagnostic safety tab shown in <u>Figure 37</u> makes it possible to know the safety status of the device. The safety function events, like voltage monitoring flags, analog and logical BIST status, and safety pins are automatically reported in this tab. The PF5030 can also get out of OTP or Debug mode using this tab.

Safe IO	Diag. Safety	OV/UV Status	Status and States	General Flags
Report PECODD Change     No Failure       Report PECOD Event     No Power GOOD       Report PECOD End Control     POCOD pad conced high       External Reset     No external RESET       STB driver     High       STB active     No reset       STB drag     No failure       STB request     -       SFOB driver     High       SFOB driver     High       SFOB request     -       SFOB request     -       Write     Read	FCCU12Error     No Error       FCCU12Error RT     No Error       FCCU1Error RT     No Error       FCCU1Error RT     No Error       FCCU2Error     No Error       FCCU2Error     No Error       FCCU2Error RT     No Error       FCCU2Error RT     No Error       FCCU2Error     No error       FCCU2Error     No error       FCCU2Error     No error       ErrMon Input Error     No error       ErrMon Input Error     No error       FS I2C CRC Status     No Error       FS I2C CRC Status     No Error       FS I2C CRC Status     No Error       Write     Read	VMCND_J/V         No Lindervoltage           VMCND_OV         No Overvoltage           VMCN1_VV         No Undervoltage           VMCN1_VV         No Undervoltage           VMCN1_VV         No Undervoltage           VMCN1_VV         No Undervoltage           VMCN2_VV         No Overvoltage           VMCN3_OV         No Overvoltage           VMCN3_OV         No Overvoltage           VMCN3_OV         No Overvoltage           VMCN4_VV         No Undervoltage           VMCN5_VV         No Overvoltage           VMCN5_VV         No Undervoltage           VMCN6_VV         No Overvoltage           VMCN8_VVV         No Undervoltage <td< td=""><td>ABIST 1 Status Pess ABIST 2 Status Pess IBIST Status Pess F5 Test Mode Activation Status Active F5 Debug Mode Exit F5 Debug Mode Exit F6 OTP Mode Exit F6 OTP Mode Exit F6 OTP Mode Exit F3 Stafe Machine State F3 Stafe Machine State Write Read</td><td>PS 12C Communication Error Active Watchdog Refresh Error No action Fail Safe 102 Error No debug Voltage Monitoring Error 0x00 0TP Bit Comruption No error detected INIT Register Corruption No comption Write Read</td></td<>	ABIST 1 Status Pess ABIST 2 Status Pess IBIST Status Pess F5 Test Mode Activation Status Active F5 Debug Mode Exit F5 Debug Mode Exit F6 OTP Mode Exit F6 OTP Mode Exit F6 OTP Mode Exit F3 Stafe Machine State F3 Stafe Machine State Write Read	PS 12C Communication Error Active Watchdog Refresh Error No action Fail Safe 102 Error No debug Voltage Monitoring Error 0x00 0TP Bit Comruption No error detected INIT Register Corruption No comption Write Read

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#### 6.6.3.5 Main tab

Main configuration is possible from the main tab shown in <u>Figure 38</u>. The clock management box allows the configuration of the clock modulation. A regulator can be assigned to a voltage monitoring using the VMON assignment box, leading to a shutdown if OV occurs on the associated regulator.

The PF5030 can go STANDBY / LPOFF state using "Go to Standby" command, setting the bit GOTO\_STBY = 1.

Clock Management				Miscellaneo	us		VMON Assignment	
Clock Modulation Enable Clock Modulation Deable Clock Modulation CFG Triangular modulatis Clock Prequency Turing 0 • 0 External FIN Disable External FIN Select FIN Divider Select FIN Clock Select Kit selected FIN To clock Select Kit selected Virtie Resid Virtie Resid		scillator is selected	VSLP OV threshold configura Waice Dashle Waice 2 Dashle Waice 2 Dashle Waice 2 RT KFALB 8 RT Main 12C CRC Status Main 12C CRC Status INTB Assertion Recuest	Sov min - 32Y type	30V min - 32V type - 34V max wake up enabled WAKE is high wake up enabled WAKE2 is low level VFALE is low level No error No error Read	VMON1     External Regulator     External Regulator (no action if OV)       VMON2     External Regulator     External Regulator (no action if OV)       VMON3     External Regulator     External Regulator (no action if OV)       VMON4     External Regulator     External Regulator (no action if OV)       VMON5     External Regulator     External Regulator (no action if OV)       VMON6     External Regulator     External Regulator (No action if OV)       VMON7     External Regulator     External Regulator (No action if OV)       VMON8     External Regulator     External Regulator (No action if OV)       VMON8     External Regulator     External Regulator (No action if OV)       VMON8     External Regulator     External Regulator (No action if OV)       VMON8     External Regulator     External Regulator (No action if OV)       VMON8     External Regulator     External Regulator (No action if OV)       VMON9     External Regulator     External Regulator (No action if OV)		
	Battery Switch	Ge	neral Flags		Device State		Power Sequence	
AT SW Driver AT SW Sense AT SW Assertion AT SW Release AT Short Timer CFG	BAT_SW driver command sensed high BAT_SW pad sensed high OTP_TBAT_SC_CFG Ite Read	Main 12C Communic Wake Up Event VSUP Event VRE Event VBOOST Event Buck Event LDO1 Event LDO2 Event	ation Error: No Failure Wake event Event occurred No Event No Event No Event No Event No Event No Event	Main Normal Main OTP Mode RT Main OTP Mode Exit Go to Standby Resume from Standby o Resume from Standby o Resume from DFS due to Resume from DFS due to	lue to XFAILB Does not resume from STBY o TSD Event Does not resume from deep Does not resume from deep	due to XFAILB fail safe due to TSD fail safe	NFALID Slot Do not assert durin   FOUT Slot Do not day FOUT Slot Do not day FOUT Slot Do not drive during   Drive FOU  Write Read	

#### 6.6.3.6 Regulators tab

The regulator tab shown in Figure 39 is used to configure the PF5030 SMPS or LDO. Regulators can be enabled or disabled on registers using  $I^2C$  commands, and the state / status of each regulators is also shown.

Each regulator has its own thermal shutdown (TSD) protection. After a TSD, the regulator is automatically reenabled when the temperature returns to the normal operation range. Nevertheless, an additional configuration, by regulator, is available to make device transition to deep fail-safe (DEEP-FS) state in case of TSD and consequently shut down all regulators. In a practical perspective, it means that TSD on regulators supplying MCU rails can be configured to make a transition to DEEP-FS while regulators supplying external loads wont.

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	Voltage R	tegulators		Regulators Co	ntrol
	VPRE		VBOOST	VPRE Enable in Normal Mode	
PRE HS Rising SR PRE HS Falling SR	PU/PC/130mA    PU/PD/130mA   PU/PD/130mA   PU/PD/130mA	Behavior in case of TSD VBOOST LS SR	Regulator shutdown   Regulator shutdown + State machine transition to Standby mode  500 V/us   500 V/us	VPRE Disable in Normal Mode Boost Enable in Normal Mode Boost Disable in Normal Mode	
RE LS SR RE Pull Down Disable	PU/P0/2001A         PU/P0/2001A           PU/P0/900mA         PU/P0/900mA           no effect         Write	10003112334	Write	Boost Disable in Normal Mode Boost State Buck Enable in Normal Mode Buck Disable in Normal Mode Buck State	
ehavior in case of TSD	BUCK Regulator shutdown + State machine transition to Standby mode write	Behavior in case of TSD	LDO1 Regulator shutdowr + Regulator shutdown + State machine transition to Standby mode Write	LDO 1 Enable in Normal Mode LDO 1 Disable in Normal Mode LDO 1 State LDO 2 Enable in Normal Mode	
ehavior in case of TSD	LD02 Regulator shutdown + State machine transition to Standby mode	L		LDO2 Disable in Normal Mode LDO2 State	
	Write	Read		Write	Read

#### 6.6.3.7 Main interrupts tab

The main interrupts tab shown in <u>Figure 40</u> allows the monitoring of the regulators, the wake inputs, and the communication events or status. It allows the reading, writing, and polling of overvoltage/undervoltage, overtemperature, and overcurrent flags.

- Main Interru	nt Eail	Safe Interru	nt											Read All
Main Interru					1	0	<b>.</b>	-				Over Cur		Itedd All
	Clear	r/Under Vo Clear Status	Mask	Mask Status		Clear	er Temper Clear Status	ature Mask	Mask Status		Clear	Clear Status	Mask	Mask Status
VSUP UVL				Not Mas	BOOSTOT				Not Mas	VPREOC				Not Mas
VSUP UVH				Not Mas	BUCKOT				Not Mas	BUCKOC				Not Mas
SUP UV7				Not Mas	LDO10T				Not Mas	LDO10C				Not Mas
/SUP OV				Not Mas	LDO2OT				Not Mas	LDO2OC				Not Mas
VBOS UVH				Not Mas	С	lear	Write R	ead	Poll		Clear	Write	Read	Poll
VPRE UVL	V						/(				/_		/	
VPRE UVH	V			Not Mas										
VPRE OV				Not Mas										
BOOST OV				Not Mas										
Clea	ar V	Vrite R	ead	Poll	]									
		Miscellaneo	DUS		l i									
	Clear	Clear Status	Mask	Mask Status										
WK1FLG			<b>v</b>	Masked										
WK2FLG			<b>v</b>	Masked										
COM_ERR				Not Mas										
Clea	ar V	Vrite R	ead	Poll										

Figure 40. Interrupts tab

Different commands can be used to manage the interrupts:

- Clear: Interrupt flags latched and selected are cleared
- Write: Masks an interruption when the mask is selected
- Read: Gives the status of all interrupts
- Poll: Reads interrupts values in a loop

Additionally, Clear All / Read All buttons are available to control all interrupts on one click.

#### 6.6.3.8 Fail-safe interrupts tab

The fail-safe interrupts tab shown in <u>Figure 41</u> allows the monitoring of the overvoltage/undervoltage fail-safe monitoring status and the watchdog. It allows the reading, writing, and polling of overvoltage/undervoltage flags.

	U	nder Volta	ge		Over Voltage				Safety Interrupts					
	Clear	Clear Status	Mask	Mask Status		Clear	Clear Status	Mask	Mask Status		Clear	Clear Status	Mask	Mask Status
MON0 UV				Not Mas	VMON0 OV				Not Mas	FCCU1				Not Mas
MON1 UV				Not Mas	VMON1 OV				Not Mas	FCCU2				Not Mas
MON2 UV				Not Mas	VMON2 OV				Not Mas	FCCU12				
MON3 UV				Not Mas	VMON3 OV				Not Mas	ERRMON				Not Mas
/MON4 UV				Not Mas	VMON4 OV				Not Mas	BAD_WD_DATA				
MON5 UV				Not Mas	VMON5 OV				Not Mas	BAD_WD_TIMING				
MON6 UV				Not Mas	VMON6 OV				Not Mas	Clear	Write	Read	Poll	
MON7 UV				Not Mas	VMON7 OV				Not Mas					
MON8 UV				Not Mas	VMON8 OV				Not Mas					
/MON9 UV				Not Mas	VMON9 OV				Not Mas					
Clea	ar W	rite Re	ad I	Poll	Clea	ar V	Vrite Re	ead	Poll					

The same set of commands is used as the set to manage the interrupts as main interrupts.

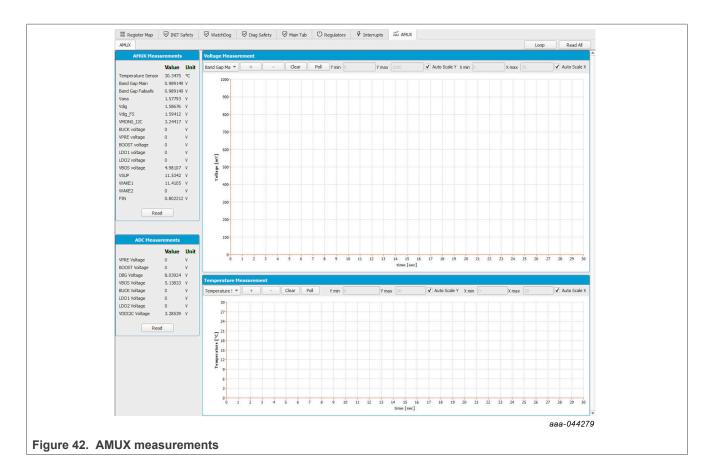
#### 6.6.3.9 AMUX

The AMUX tab shown in Figure 42 allows the selection of an AMUX pin channel and gets its current value by using the exclusive KL25Z AMUX ADC channel. You can do a single read or display various channels dynamically on the voltage or temperature graph. The displayed values already apply the divider and temperature formulas.

The input / output voltage rails are also monitored independently using additional the KL25Z ADC channels.

To use the dynamic graph, select the channel then click the "+" button to add to the graph. To start polling, click the "Poll" button. Click the "Poll" button again to stop measurements.

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### 7 Using an evaluation board

Before starting the process, consult your development board scheme and user manual to configure your required use case.

Learn about OTP before operating with the device. The device has a high level of flexibility due to the parameter configuration available in the OTP. It impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers, and the PF5030 device.

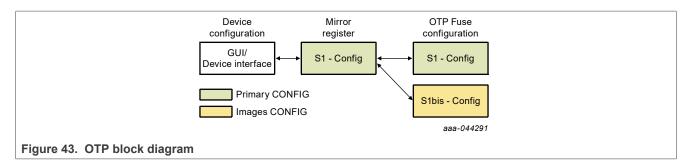
The OTP-related operations can only be performed in test mode (emulation) and OTP mode (programming, test mode is enabled automatically). When using emulation, the device loses the configuration when the power supply is switched off, when the device enters deep fail-safe (DEEP-FS) state, or when it goes standby.

#### 7.1 OTP and mirrors registers

The device incorporates two OTP blocks. One is for the main section, the other for the fail-safe section. During configuration, each of them uses dedicated sectors.

Each block is divided in two sectors, S1 and S1bis respectively, so the device can be fused two times. The OTP configuration scheme is shown in Figure 43 (same implementation for main and fail-safe).

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At device starts-up, the content of the valid (last programmed) sector is loaded into mirror registers. The mirror register content is accessible from the NXP GUI, using specific I<sup>2</sup>C commands. The NXP GUI manages the mirror configuration, which facilitates access. The mirror register content handling is called "OTP emulation".

To burn the OTP configuration, the mirror register content must be loaded with the desired content. Then a command must be sent to burn the mirror content to the next available OTP sector. The first sector to be burned is S1, the second S1bis. The NXP GUI automatically manages the next sector to be burned. It is not possible to revert to the previous sector. When the user reaches the sector S1bis, there is no other possibility for burn. However, the emulation is still available.

#### 7.2 Device modes

There are several modes that describe device operation.

There are three modes to run the device:

- User mode: Only user-related registers can be accessed and handled.
- **OTP mode**: OTP fuse content loaded to mirror registers. OTP programming / emulation (mirror registers handling) possible.
- **Test mode**: OTP programming and mirror registers handling (emulation) granted.

There are two modes to run the device related to the fail-safe state machine:

- Normal mode: Watchdog windowing and initialization (INIT FS state) timeout depend on OTP configuration.
- Debug mode: Watchdog windowing disabled, no initialization timeout, fail-safe safety reactions disabled.

Debug and OTP modes are enabled by applying voltage on DBG pin during startup and/or restart.

OTP mode activation implies in Debug mode activation.

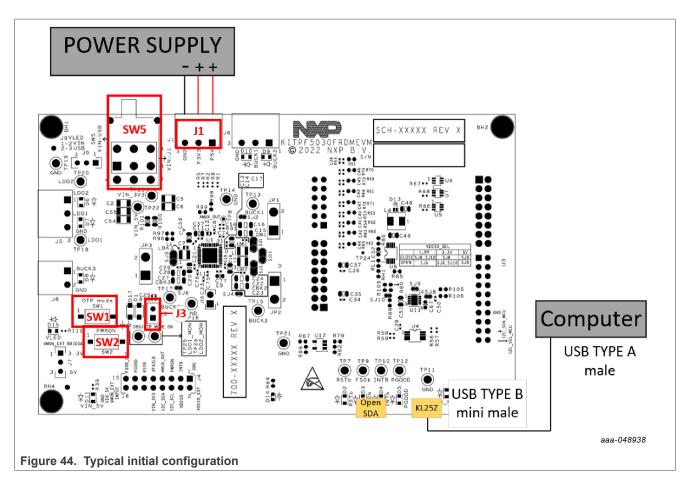
Debug and OTP modes can be disabled with an  $I^2C$  command.

Test mode can be enabled at any moment with an I<sup>2</sup>C command when the voltage is applied on DBG pin.

#### 7.3 Configuring the hardware for start-up

<u>Figure 44</u> presents a typical hardware configuration incorporating the development board, power supply and, Windows PC workstation.

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To configure the hardware and workstation as illustrated in <u>Figure 44</u>, complete the following procedure:

1. Install jumpers and switches for the configuration shown in Table 21.

Table 21.	Hardware	configuration
-----------	----------	---------------

Board		Configuration			
configuration	Normal mode	OTP / test mode entry			
Watchdog	Watchdog windowing enabled, 2 seconds INIT_FS timeout (OTP WDW_INF = 0)	Watchdog windowing disabled,	OTP programming / emulation,		
configuration	Watchdog windowing disabled, no INIT_FS timeout (OTP WDW_INF = 1)	no INIT_FS timeout	Debug mode enabled		
J3 (DBG)	Open	Connect 1 to 2 DBG pin voltage pulled to 4.5 V or 7.95 V (SW1)			
SW2 (PWRON)	Close (PWRON pin high-logic level)				
SW5 (VIN)	Midd	le position (supplies OFF)			
SW1 (OTP mode)	Open (DBG = VIN	_5V)	Close (OTP mode ON)		

- 2. Connect the Windows PC USB port to the KITPF5030FRDMEVM board using the provided USB 2.0 cable.
- 3. If external power supplies are used, set the power supplies to 3.3 V and 5.0 V, and current limit to 1.0 A. With power turned off, attach the power supplies positive and negative outputs to J1, then turn on.
- 4. Put SW5 in LEFT position if USB power is used or RIGHT position if external power supply is used.

At this step, if the product is in OTP mode entry configuration, all regulators are OFF. The user can power up with an OTP configuration or configure the mirror registers before powering up. Power-up sequence starts as soon as one of these four actions occurs:

- J3 jumper is removed
- SW1 is switched OFF
- OTP mode exit command is sent using I<sup>2</sup>C
- NXP GUI button "Exit OTP Mode" is clicked

#### 7.4 Working in OTP emulation mode

At start-up, the device always uses the content of the mirror register. This content can come from OTP fuse or from a configuration written directly in the mirror register. OTP emulation means that the user can emulate the fuse content by writing in the mirror register, which allows trials before burning the OTP.

- 1. Configure the hardware for OTP mode entry.
- 2. Launch the NXP GUI for Automotive PMIC Families software.
- 3. Create an OTP configuration and export/generate the TBB/OTP script file.
- 4. Establishing the connection between the NXP GUI and the hardware.

MCU: FRDM-KL25Z State: CONNECTED	Protocol: I <sup>2</sup> C Firmware: 0.3 Application 3.1.144 Device Mode: user-mode Color legend	High 🦲	Low	FS CURRENT STATE :	OTP_MODE	
					aaa-044	4294

Check that the fail-safe state machine is in OTP MODE state and "Exit OTP mode" must be green. If not, check 1 and redo this step. While in OTP mode, all regulators are off.

- 5. On the script editor, load the TBB/OTP script file and send content to the mirror registers.
- 6. Click "Exit OTP mode" button, if all goes right, regulators start-up and fail-safe state machine must be in INIT\_FS state.

MCU: FRDM-KL25Z State: CONNECTED	Protocol: I <sup>2</sup> C Firmware: 0.3 Application 3.1.144 Device Mode: test-mode Color legend: High Low FS CURRENT STATE :	INIT_FS
		aaa-044295

- a. If the mirror registers are filled (with a configuration using the Script editor), that configuration is used in the emulation session.
- b. If the mirror registers are not filled (with a configuration using the Script editor), the currently programmed OTP fuse configuration is used, if it exists.
- c. Otherwise, the mirror registers are not filled and the OTP fuse is not burned. The device does not start up properly.

Device is in Debug mode. As long as Debug mode is not exited by writing FS\_STATES: [FS\_DBG\_MODE\_EXIT] bit to 1, the FS0B pin cannot be released.

#### 7.5 Releasing FS0B script

The following script can be used to release FS0B:

- Disable the watchdog windowing (simple watchdog configuration is used here).
- Close the initialization phase with (a first) good watchdog refresh.
- Exit the Debug mode.
- Send six (default) additional consecutive good watchdog refreshes to revert the fault error counter to 0.
- Release FS0B pin, which is only valid if watchdog windowing is activated in OTP.

Step	Register name	Value	Description
1	FS_WD_WINDOW_DUR	0x020B	WDW_PERIOD[4:0] = 0x00000 (watchdog disabled)
2	FS_NOT_WD_WINDOW_DUR	0xFD04	NOT of FS_WD_WINDOW_DUR
3	FS_WD_ANSWER	0x5AB2	1st good watchdog answer (close the initialization phase)
4	FS_STATES	0x4000	FS_DBG_MODE_EXIT = 1 (exit debug mode)
5	FS_WD_ANSWER	0x5AB2	2nd good watchdog answer
6	FS_WD_ANSWER	0x5AB2	3rd good watchdog answer
7	FS_WD_ANSWER	0x5AB2	4th good watchdog answer
8	FS_WD_ANSWER	0x5AB2	5th good watchdog answer
9	FS_WD_ANSWER	0x5AB2	6th good watchdog answer
10	FS_WD_ANSWER	0x5AB2	7th good watchdog answer
11	FS_RELEASE_FS0B	0xB2A5	FS0B pin released (pulled to high level)

Table 22. Release FS0B sequence example for simple watchdog (ASIL B)

This sequence can be sent using a script built with NXP GUI. There are two options:

- Clicking ACCESS > WatchDog > "Watchdog Management" > "FS0B Release script". Remember to chose appropriated "Watchdog Type" before.
- Clicking SCRIPT (editor) > Generator > "FS0B\_RELEASE\_XX\_WATCHDOG", then click "RUN".

#### 8 References

KITPF5030FRDMEVM — detailed information on this board, including documentation, downloads, and software and tools

www.nxp.com/KITPF5030FRDMEVM

- [2] **PF5030** detailed information on PF5030 http://www.nxp.com/PF5030
- [3] NXP GUI for Automotive PMIC Families Software GUI for NXP Automotive PMIC products https://www.nxp.com/PMIC-GUI-SW

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