TJF1441

High-speed CAN transceiver

Rev. 2 — 15 October 2021 Product data sheet

1 General description

The TJF1441 is a member of the TJA144x family of transceivers that provide an interface between a Controller Area Network (CAN) or CAN FD (Flexible Data rate) protocol controller and the physical two-wire CAN bus. TJA144x transceivers implement the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5, and are fully interoperable with high-speed Classical CAN and CAN FD transceivers. All TJA144x variants enable reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

The TJF1441 is designed for CAN industrial applications allowing networks to run at very low bit rates up to 5 Mbit/s CAN-FD. A VIO supply input allows for direct interfacing with 3.3 V and 5 V-supplied microcontrollers. It is intended as a replacement for high-speed Classical CAN and CAN FD transceivers, such as the TJF1051 from NXP. It offers pin compatibility and is designed to avoid changes to hardware and software design, allowing the TJF1441 to be easily retrofitted to existing applications.

A variant intended for high-speed CAN applications in the automotive industry, the TJA1441, is also available.

2 Features and benefits

2.1 General

- ISO 11898-2:2016, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- Standard CAN and CAN FD data bit rates up to 5 Mbit/s
- Optimized for industrial applications
- Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI)
- Silent mode for node diagnosis and failure containment
- VIO input for interfacing with 3.3 V to 5 V microcontrollers
- Available in SO8 package
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.2 Predictable and fail-safe behavior

- Undervoltage detection with defined handling on all supply pins
- Full functionality guaranteed from the undervoltage detection thresholds up to the maximum limiting voltage values
- Defined behavior below the undervoltage detection thresholds
- Transceiver disengages from the bus (high-ohmic) when the supply voltage drops below the Off mode threshold
- Internal biasing of TXD and mode selection input pin, to enable defined fail-safe behavior

2.3 Protection

- High ESD handling capability on the bus pins (8 kV IEC and HBM)
- Thermally protected

3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
I_{CC}	supply current	Normal mode, dominant	-	38	60	mA
		Normal mode, recessive	-	4	7	mA
		Silent mode	-	3	6	mA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin VCC		4	-	4.5	V
$V_{uvhys(VCC)}$	undervoltage hysteresis voltage on pin VCC		50	-	-	mV
V_{IO}	supply voltage on pin VIO		2.95	-	5.5	V
I_{IO}	supply current on pin VIO	Normal mode, dominant; V_{TXD} = 0 V	-	250	760	µA
		Normal mode, recessive; V_{TXD} = V_{IO}	-	150	460	µA
		Silent mode; V_{TXD} = V_{IO}	-	70	200	µA
$V_{uvd(swoff)(VIO)}$	switch-off undervoltage detection voltage on pin VIO		2.65	-	2.95	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins CANH and CANL	-8	-	+8	kV
V_{CANH}	voltage on pin CANH	limiting value according to IEC 60134	-36	-	+40	V
V_{CANL}	voltage on pin CANL	limiting value according to IEC 60134	-36	-	+40	V
T_{vj}	virtual junction temperature		-40	-	+150	°C

4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJF1441AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Table 3. TJF1441 feature overview

See Section 18 for a feature overview of the complete TJx144x/TJx146x/TJF1441 family.

	Modes					Supplies			Data rate		Additional features					
Device[1]	Normal	Standby	Sleep	Silent/Listen-only	Selectable Off	VCC pin	VIO pin	VBAT pin	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN FD	Signal improvement[2]	Wake-up source recognition[3]	Short WUP support [0.5 - 1.8 µs][4]	Single supply pin wake-up	TXD dominant timeout	Local diagnostics via ERR_N pin
TJF1441A	●			●		●	●		●						[5]	

[1] TJF1441 is AEC-Q100 Grade 1.
[2] CAN FD Signal Improvement Capability (SIC) according to CiA 601-4:2019.
[3] RXD is held LOW after wake-up request, enabling wake-up source recognition.
[4] WUP = wake-up pattern according ISO11898-2:2016.
[5] Not having TXD dominant timeout allows for very low data rates in non-automotive grade applications.

5 Block diagram

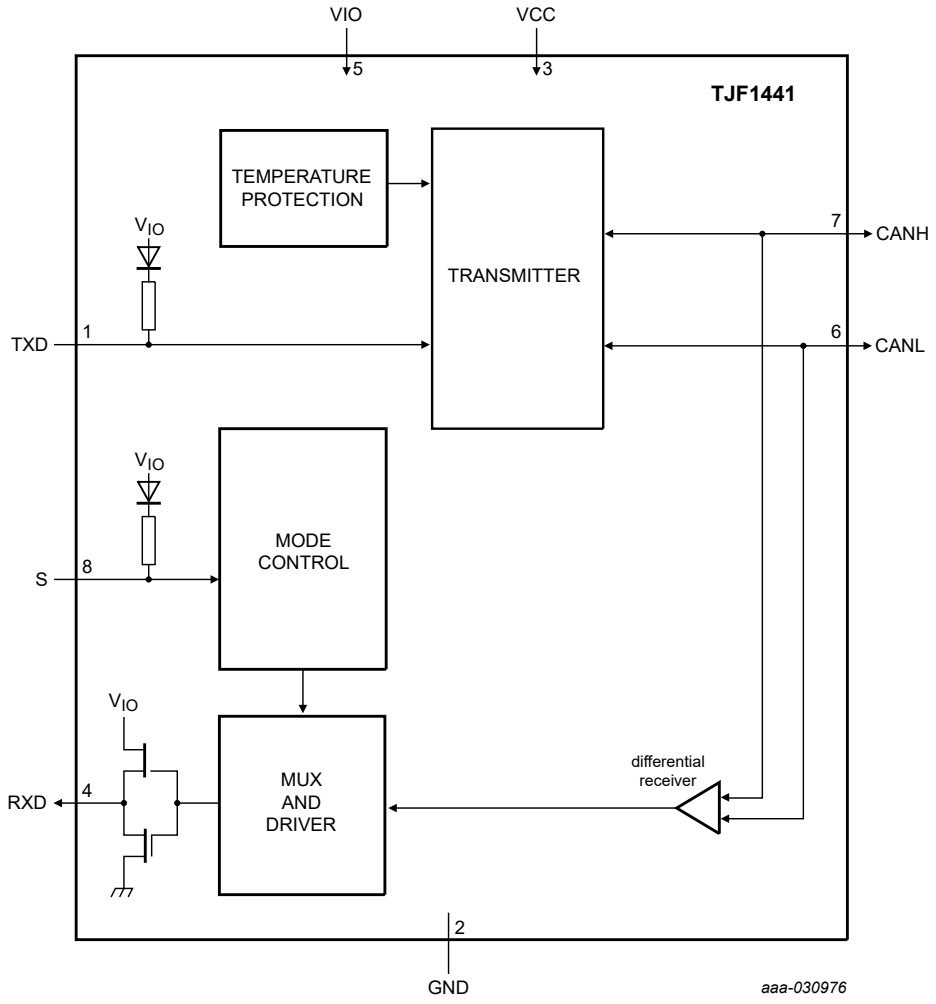


Figure 1. Block diagram

6 Pinning information

6.1 Pinning

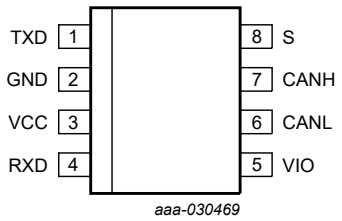


Figure 2. Pin configuration diagram

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1]	Description
TXD	1	I	transmit data input; inputs data (from the CAN controller) to be written to the bus lines
GND	2	G	ground
VCC	3	P	5 V supply voltage input
RXD	4	O	receive data output; outputs data read from the bus lines (to the CAN controller).
VIO	5	P	supply voltage for I/O level adapter
CANL	6	AIO	LOW-level CAN bus line
CANH	7	AIO	HIGH-level CAN bus line
S	8	I	Silent mode control input

[1] I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.

7 Functional description

7.1 Operating modes

The TJF1441 supports three operating modes, Normal, Silent, and Off. The operating mode is selected via pin S. See Table 5 for a description of the operating modes under normal supply conditions. Mode changes are completed after transition time $t_{t(moch)}$.

Table 5. Operating modes

Mode	Inputs		Outputs	
	Pin S	Pin TXD	CAN driver	Pin RXD
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Silent	HIGH	X	biased to $V_{CC}/2$	LOW when bus dominant
				HIGH when bus recessive
Off[1]	X	X	high-ohmic state	high-ohmic state

[1] Off mode is only entered when the voltage on pin VCC is below $V_{uvd(VCC)}$ or the voltage on pin VIO is below $V_{uvd(swoff)VIO}$ (see Figure 3).

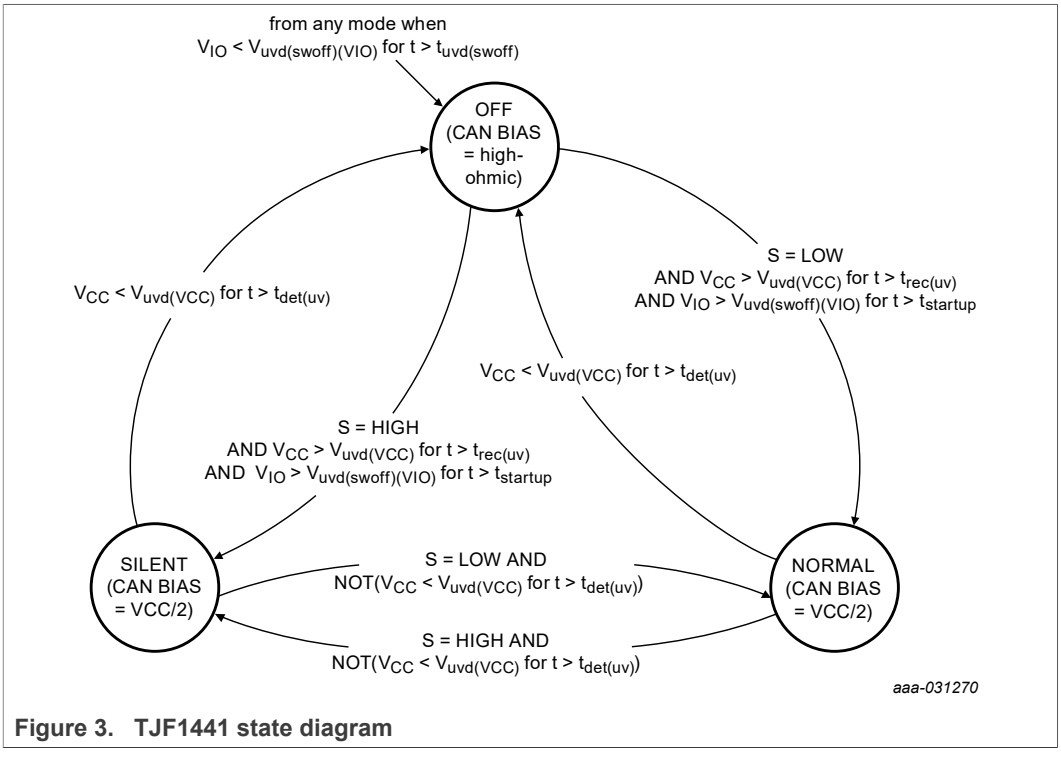


Figure 3. TJF1441 state diagram

7.1.1 Off mode

The TJF1441 switches to Off mode from any mode when the supply voltage on pin VIO falls below the switch-off undervoltage detection threshold ($V_{uvd(swoff)(VIO)}$) or when V_{CC} drops below $V_{uvd(VCC)}$. This is the default mode when the supply is first connected.

The CAN pins and pin RXD are in a high-ohmic state in Off mode.

When the supply voltage rises above the switch-off undervoltage detection threshold, the TJF1441 starts to boot up, triggering an initialization procedure. It switches to the selected mode after $t_{startup}$, provided $V_{CC} > V_{uvd(VCC)}$.

7.1.2 Silent mode

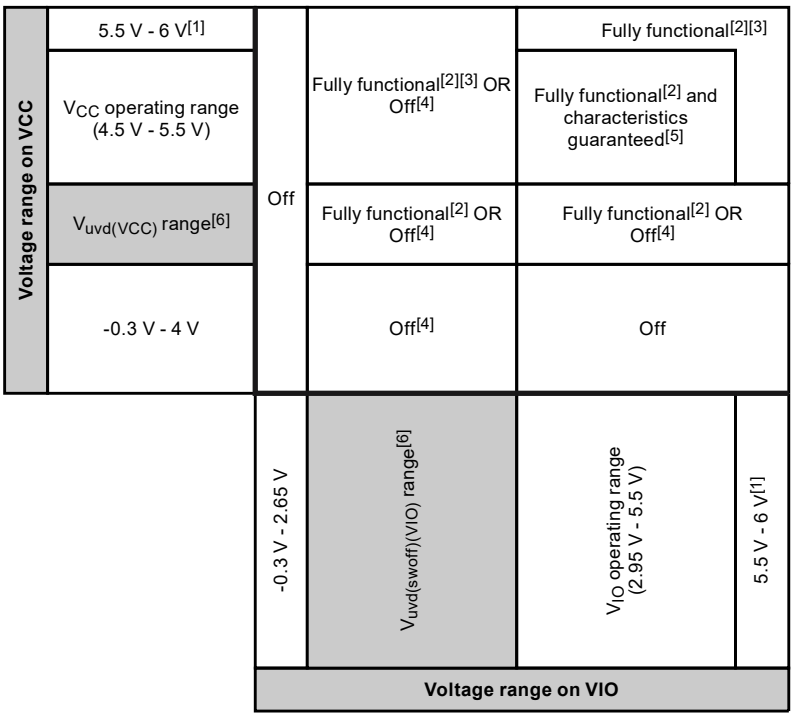
A HIGH level on pin S selects Silent mode. The transmitter is disabled in Silent mode, releasing the bus pins to $V_{CC}/2$. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller disrupting network communications.

7.1.3 Normal mode

A LOW level on pin S selects Normal mode. In Normal mode, the transceiver can transmit and receive data via bus lines CANH and CANL. Pin TXD must be HIGH at least once in Normal mode before transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME. In recessive state, the output voltage on the bus pins is $V_{CC}/2$.

7.1.4 Operating modes and gap-free operation

Gap-free operation guarantees defined behavior at all voltage levels. Supply voltage-to-operating mode mapping is detailed in Figure 4 and in the state diagram (Figure 3).



[1] 6 V is the IEC 60134 Absolute Maximum Rating (AMR) for VCC and VIO (see Limiting values table). Above the AMR, irreversible changes in characteristics, functionality or performance may occur. Returning from above AMR to the operating range, datasheet characteristics and functionality cannot be guaranteed.
[2] Target transceiver functionality as described in this datasheet is applicable.
[3] Prolonged operation of the device outside the operating range may impact reliability over lifetime. Returning to the operating range, datasheet characteristics are guaranteed provided the AMR has not been exceeded.
[4] For a given value of V_{CC} or V_{IO}, a specific device will be in a single defined state determined by its undervoltage detection thresholds ($V_{uvd(VCC)}$ and $V_{uvd(swoff)(VIO)}$). The actual thresholds can vary between devices (within the ranges specified in this data sheet). To guarantee the device will be in a specific state, V_{IO} and V_{CC} must be either above the maximum or below the minimum thresholds specified for these undervoltage detection ranges.
[5] Datasheet characteristics are guaranteed within the V_{CC} and V_{IO} operating ranges. Exceptions are described in the Static and Dynamic characteristics tables.
[6] The device is fully functional when both V_{CC} and V_{IO} are above the undervoltage threshold. If V_{CC} or V_{IO} falls below any undervoltage threshold, the device switches to Off mode.

aaa-038711

Figure 4. Supply voltage ranges and gap-free operation

7.2 Fail-safe features

7.2.1 Internal biasing of TXD and S input pins

Pins TXD and S have internal pull-ups to VIO to ensure a safe, defined state in case one or more of these pins is left open or become floating. Pull-up resistors are active on these pins in all states; they should be held at the V_{IO} level in Silent mode to minimize supply current.

7.2.2 Undervoltage detection on pins VCC and VIO

If V_{CC} or V_{IO} drops below the undervoltage detection threshold ($V_{uvd(VCC)}$ or $V_{uvd(swoff)VIO}$) the transceiver switches to Off mode and disengages from the bus (zero load; bus pins high-ohmic) until the supply voltage has recovered. If Normal mode is selected, the output drivers are enabled once both V_{CC} and V_{IO} are again within their operating ranges and TXD has been reset to HIGH.

7.2.3 Overtemperature protection

The device is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the CAN bus drivers are disabled. When the junction temperature drops below $T_{j(sd)rel}$, the CAN bus drivers recover once TXD has been reset to HIGH and Normal mode is selected (waiting for TXD to go HIGH prevents output driver oscillation due to small variations in temperature).

7.2.4 VIO supply pin

Pin VIO should be connected to the microcontroller supply voltage (see Figure 8). This adjusts the signal levels on pins TXD, RXD and S to the I/O levels of the microcontroller, allowing for direct interfacing without additional glue logic. Spurious signals from the microcontroller on pin S are filtered out with a filter time of $t_{filtr(IO)}$.

8 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	on pins VCC, VIO, TXD, S	-0.3	+6	V
			-	+7[2]	
		on pins CANH, CANL	-36	+40	V
		on pins RXD	-0.3	V_{IO}+0.3[3]	
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-40	+40	V
V_{trt}	transient voltage	on pins CANH, CANL [4]			
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [5]			
		on pins CANH, CANL	-8	+8	kV
		Human Body Model (HBM)			
		on any pin [6]	-4	+4	kV
		on pins CANH, CANL [7]	-8	+8	kV
		Charged Device Model (CDM) [8]			
		on corner pins	-750	+750	V
		on any other pin	-500	+500	V
T_{vj}	virtual junction temperature	[9]	-40	+150	°C
T_{stg}	storage temperature	[10]	-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
[2] The device can withstand voltages between 6 V and 7 V for a total of 20 s over the product lifetime.
[3] Subject to the qualifications detailed in Table notes 1 and 2 above for pins VCC, VIO, TXD, and S.
[4] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO7637.
[5] Verified by an external test house according to IEC TS 62228, Section 4.3.
[6] According to AEC-Q100-002.
[7] Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 8). HBM pulse as specified in AEC-Q100-002 used.
[8] According to AEC-Q100-011.
[9] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \# R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[10] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

9 Thermal characteristics

Table 7. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		96	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		9	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).

10 Static characteristics

Table 8. Static characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJF1441A); R_L = 60 Ω; unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	supply voltage		4.5	-	5.5	V
V_{uvd}	undervoltage detection voltage	[2]	4	-	4.5	V
V_{uvhys}	undervoltage hysteresis voltage		50	-	-	mV
I_{CC}	supply current	Normal mode				
		dominant; V_{TXD} = 0 V	-	38	60	mA
		dominant; V_{TXD} = 0 V; short circuit on bus lines; -3 V < (V_{CANH} = V_{CANL}) < +40 V	-	-	125	mA
		recessive; V_{TXD} = V_{IO}	-	4	7	mA
		Silent mode; V_{TXD} = V_{IO}	-	3	6	mA
I/O level adapter supply; pin VIO						
V_{IO}	supply voltage		2.95	-	5.5	V
$V_{uvd(swoff)}$	switch-off undervoltage detection voltage	[2]	2.65	-	2.95	V
I_{IO}	supply current	Normal mode; dominant; V_{TXD} = 0 V	-	250	760	µA
		Normal mode; recessive; V_{TXD} = V_{IO}	-	150	460	µA
		Silent mode; V_{TXD} = V_{IO}	-	70	200	µA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		0.7V_{IO}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3V_{IO}	V
$V_{hys(TXD)}$	hysteresis voltage on pin TXD		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	kΩ

Table 8. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJF1441A); R_L = 60 Ω; unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance	[3]	-	-	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO}$ - 0.4 V	-10	-	-1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V	+1	-	+10	mA
Silent control inputs; pins S						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$	V
V_{hys}	hysteresis voltage		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	kΩ
C_i	input capacitance	[3]	-	-	10	pF
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; $V_{CC} \geq$ 4.75 V				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; C_{SPLIT} = 4.7 nF; f_{TXD} = 250 kHz, 1 MHz or 2.5 MHz [3] [4]	$0.9V_{CC}$	-	$1.1V_{CC}$	V
$V_{cm(step)}$	common mode voltage step	[3] [4] [5]	-150	-	+150	mV
$V_{cm(p-p)}$	peak-to-peak common mode voltage	[3] [4] [5]	-300	-	+300	mV
$V_{O(dif)}$	differential output voltage	dominant; Normal mode; V_{TXD} = 0 V; $V_{CC} \geq$ 4.75 V				
		R_L = 50 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω [3]	1.5	-	5	V
		recessive; no load				
		Normal or Silent mode; $V_{TXD} = V_{IO}$	-50	-	+50	mV
$V_{O(rec)}$	recessive output voltage	Normal or Silent mode; $V_{TXD} = V_{IO}$; no load	2	2.5	3	V
$V_{th(RX)dif}$	differential receiver threshold voltage	Normal or Silent mode; -12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V	0.5	-	0.9	V
$V_{rec(RX)}$	receiver recessive voltage	Normal or Silent mode; -12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V	-4	-	0.5	V

Table 8. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJF1441A); R_L = 60 Ω; unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{dom(RX)}$	receiver dominant voltage	Normal or Silent mode; -12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V	0.9	-	9	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	Normal or Silent mode; -12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V	50	-	-	mV
$I_{O(sc)}$	short-circuit output current	-15 V ≤ V_{CANH} ≤ +40 V; -15 V ≤ V_{CANL} ≤ +40 V	-	-	115	mA
$I_{O(sc)rec}$	recessive short-circuit output current	Normal mode; V_{TXD} = V_{IO}; -27 V ≤ V_{CANH} ≤ +32 V; -27 V ≤ V_{CANL} ≤ +32 V	-3	-	+3	mA
I_L	leakage current	V_{CC} = V_{IO} = 0 V or pins shorted to GND via 47 KΩ; V_{CANH} = V_{CANL} = 5 V;	-10	-	+10	µA
R_i	input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	25	40	50	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V	-3	-	+3	%
$R_{i(dif)}$	differential input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	50	80	100	kΩ
$C_{i(cm)}$	common-mode input capacitance	[3]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[3]	-	-	10	pF
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature		180	-	200	°C
$T_{j(sd)rel}$	release shutdown junction temperature		175	-	195	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
[3] Not tested in production; guaranteed by design.
[4] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 9.
[5] See Figure 7

11 Dynamic characteristics

Table 9. Dynamic characteristics

T_{vj} = −40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJF1441A); R_L = 60 Ω; unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN timing characteristics; $t_{bit(TXD)}$ ≥ 200 ns; see Figure 5, Figure 6 and Figure 9						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	-	102.5	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	-	102.5	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal or Silent mode	-	-	115	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal or Silent mode	-	-	115	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	215	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	215	ns
CAN FD timing characteristics; see Figure 6 and Figure 9						
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns	155	-	210	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns	120	-	220	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	-65	-	40	ns
		$t_{bit(TXD)}$ = 200 ns	-45	-	15	ns
Mode transitions						
$t_{t(moch)}$	mode change transition time	[2]	-	-	50	µs
$t_{startup}$	start-up time	[2]	-	-	1	ms
IO filter; pins S						
$t_{filtr(IO)}$	I/O filter time	[3]	1	-	5	µs
Undervoltage detection; see Figure 3						
$t_{det(uv)}$	undervoltage detection time	on pin VCC [2]	-	-	30	µs
$t_{uvd(swoff)}$	switch-off undervoltage detection time	on pin VIO [2]	-	-	30	µs
$t_{rec(uv)}$	undervoltage recovery time	on pin VCC [2]	-	-	50	µs

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Not tested in production; guaranteed by design.
[3] Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.

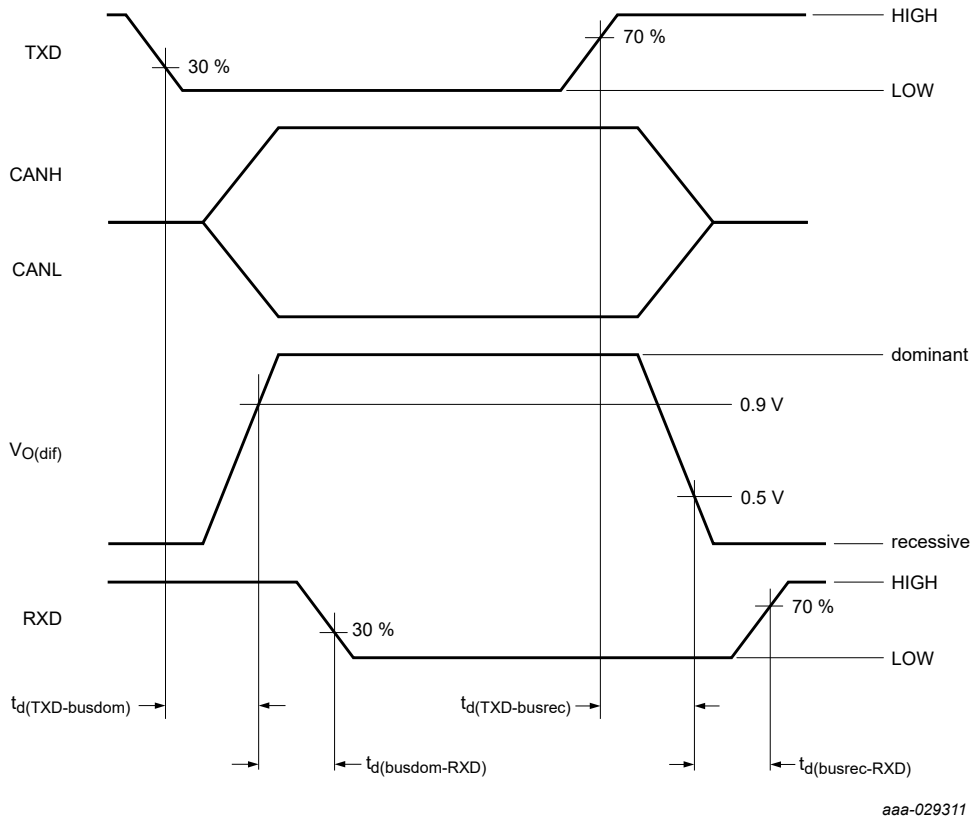


Figure 5. CAN transceiver timing diagram

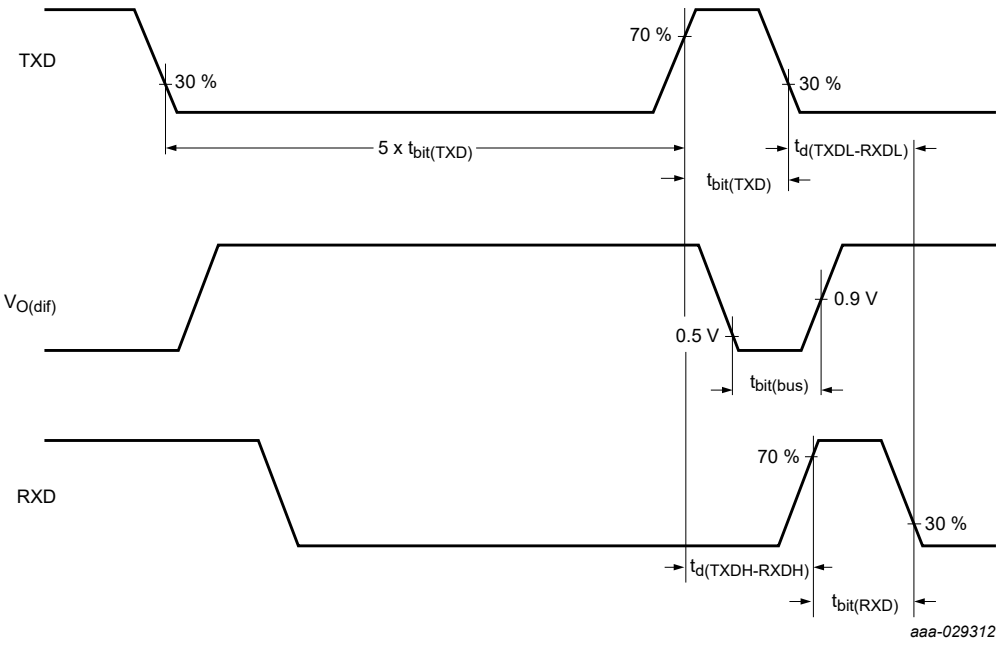


Figure 6. CAN FD timing definitions according to ISO 11898-2:2016

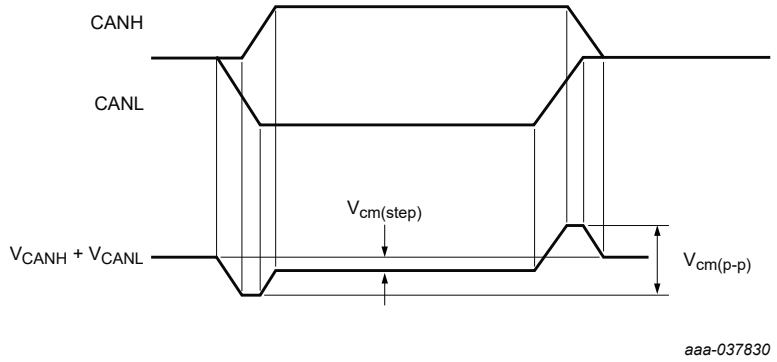


Figure 7. CAN bus common-mode voltage

12 Application information

12.1 Application diagram

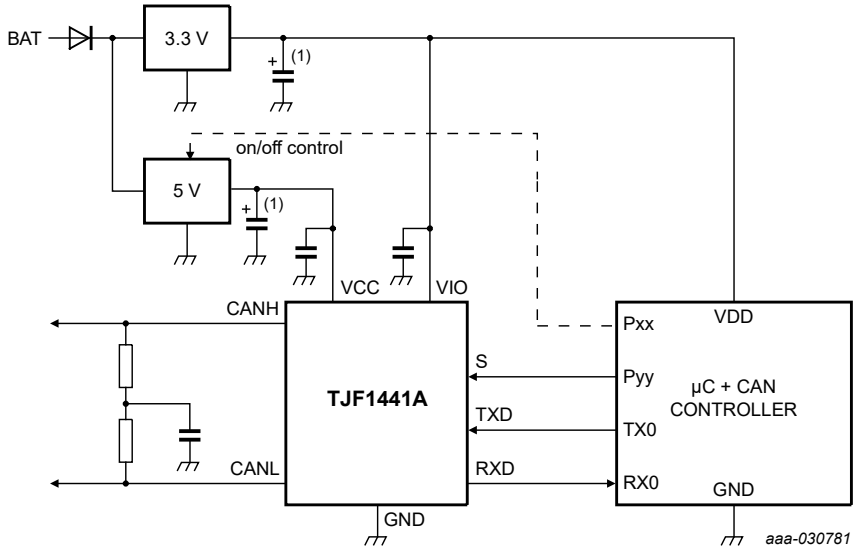


Figure 8. Typical application

12.2 Application hints

Further information on the application of the TJF1441 can be found in NXP application hints AH2002 *'TJx144x/TJx146x Application Hints'*, available on request from NXP Semiconductors.

13 Test information

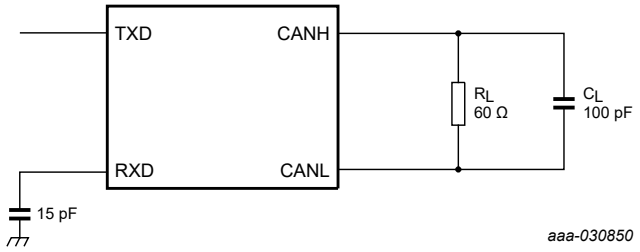


Figure 9. CAN transceiver timing test circuit

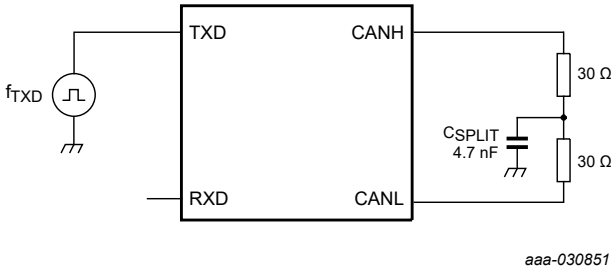
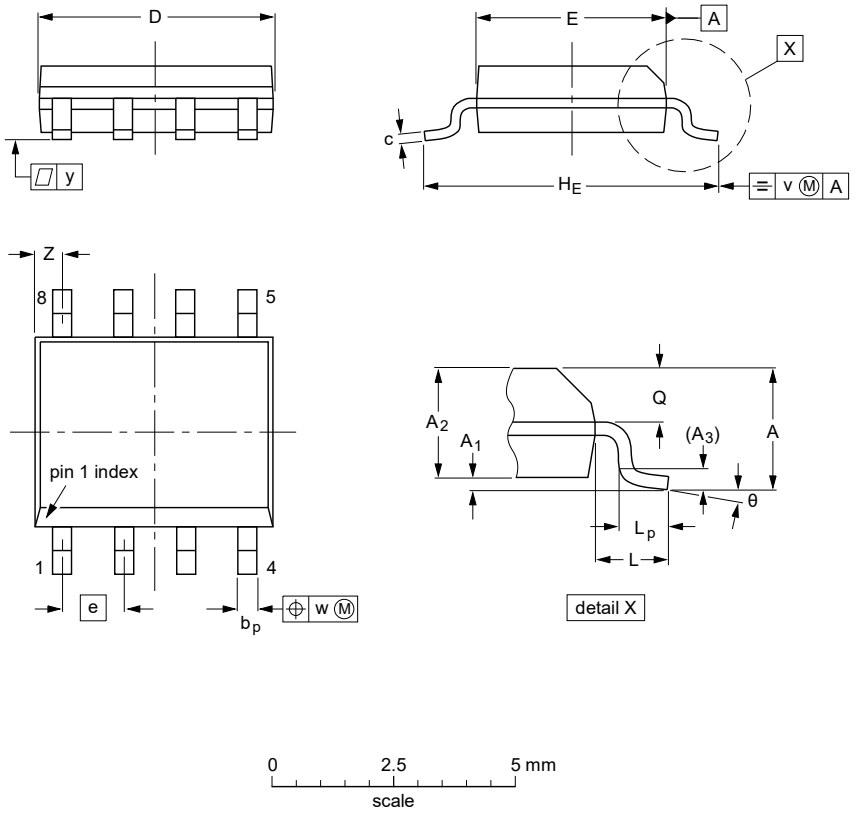


Figure 10. Test circuit for measuring transceiver driver symmetry

14 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 11. Package outline SOT96-1 (SO8)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and Table 11

Table 10. SnPb eutectic process (from J-STD-020D)

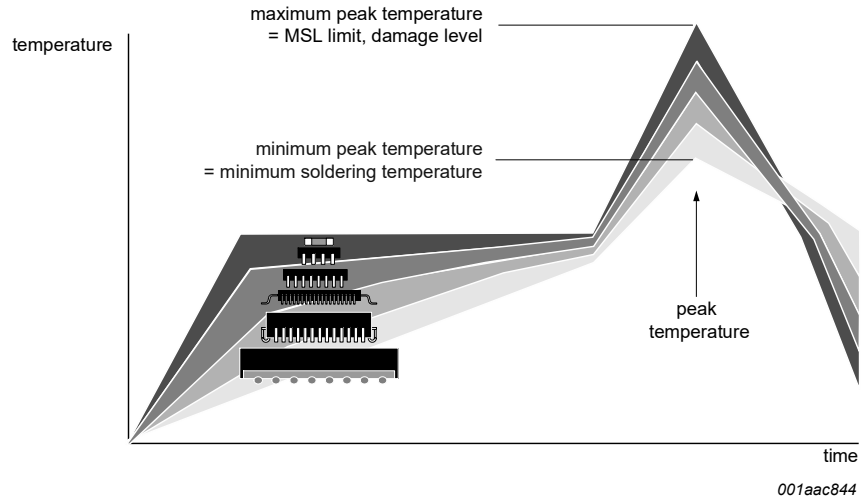
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 12.



MSL: Moisture Sensitivity Level

Figure 12. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17 Appendix: ISO 11898-2:2016 parameter cross-reference list

Table 12. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{SYM}	V_{TXsym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)dom}$	dominant short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_i	input resistance
Matching of internal resistance	MR	ΔR_i	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}	receiver timing symmetry

Table 12. ISO 11898-2:2016 to NXP data sheet parameter conversion*...continued*

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating VCAN_H and VCAN_L			
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current

18 Appendix: TJx144x/TJx146x/TJF1441 family overview

Table 13. Feature overview of the complete TJx144x/TJx146x/TJF1441 family

	Modes					Supplies			Data rate		Additional features					
Device[1]	Normal	Standby	Sleep	Silent/Listen-only	Selectable Off	VCC pin	VIO pin	VBAT pin	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN FD[2]	Signal improvement[3]	Wake-up source recognition[4]	Short WUP support [0.5 - 1.8 µs][5]	Single supply pin wake-up[6]	TXD dominant timeout	Local diagnostics via ERR_N pin
TJx1441A	●			●		●	●		●						●	
TJx1441B	●			●		●			●						●	
TJx1441D	●			●	●	●			●						●	
TJF1441A	●			●		●	●		●						[7]	
TJx1442A	●	●				●	●		●				●	●	●	
TJx1442B	●	●				●			●				●		●	
TJx1443A	●	●	●	●		●	●	●	●			●	●	●	●	●
TJx1448A	●	●				●	●		●				●	●	●	
TJx1448B	●	●				●			●				●		●	
TJx1448C	●	●				●	●		●			●	●	●	●	
TJx1462A	●	●				●	●		●	●	●		●	●	●	
TJx1462B	●	●				●			●	●	●		●		●	
TJx1463A	●	●	●	●		●	●	●	●	●	●	●	●	●	●	●

[1] TJx: TJA14xxx is AEC-Q100 Grade 1; TJR14xxx is AEC-Q100 Grade 0; TJF1441A is non-automotive grade.
[2] Only guaranteed for TJA146x, AEC-Q100 Grade 1.
[3] CAN FD Signal Improvement Capability (SIC) according to CiA 601-4:2019.
[4] RXD is held LOW after wake-up request, enabling wake-up source recognition.
[5] WUP = wake-up pattern according ISO11898-2:2016.
[6] Only VIO supply needed for wake-up in TJA1442A, TJA1448A, TJA1448C, TJA1462A; only VBAT supply needed for wake-up in TJA1443A, TJA1463A.
[7] Not having TXD dominant timeout allows for very low data rates in non-automotive grade applications.

19 Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJF1441 v.2	20211015	Product data sheet	-	TJF1441 v.1
Modifications	• Added device (Table 3) and family (Section 18) feature overviews • Table 6: table note 10 added • Table 9: CAN delay timing characteristics revised			
TJF1441 v.1	20200812	Product data sheet	-	-

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 15 October 2021
Document identifier: TJF1441

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:
TJF1441AT/0Z