

High-Voltage Types (20-Volt Rating)
XL4514 Output "High" on Select
XD4514 Output "Low" on Select

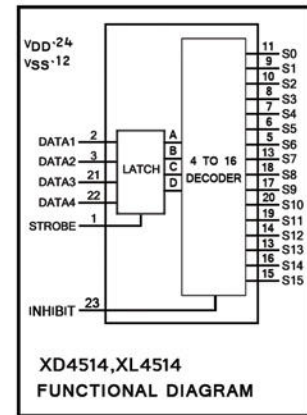
■ XL4514 and -XD4514 consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0 (XL4514) or 1 (XD4514) regardless of the state of the data or strobe inputs. The decode truth table indicates all combinations of data inputs and appropriate selected outputs. These devices are similar to industry types XL4514 and XD4514.

Features:

- Steebed input latch
- Inhibit control
- 100% tested for quiescent current at 20V
- Maximum input current of 1 μ A at 18V over full package-temperature range; 100 nA at 18V and 25°C
- Noise margin (over full package temperature range):
1V at $V_{DD} = 5V$
1V at $V_{DD} = 10V$
2.5V at $V_{DD} = 15V$
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding
- Program-counter decoding
- Control decoder



MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
Voltages referenced to V_{SS} Terminal	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500 mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100 mW
OPERATING-TEMP-TEMPERATURE RANGE (T_A)	-55°C to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65°C to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1-32 inch (1.59 \pm 0.79 mm) from case for 10s max	+265 $^\circ\text{C}$

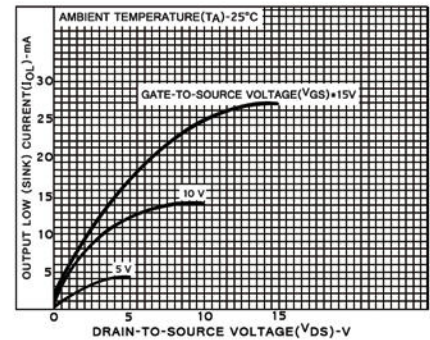


Fig.1-Typical output low (sink) current characteristics.

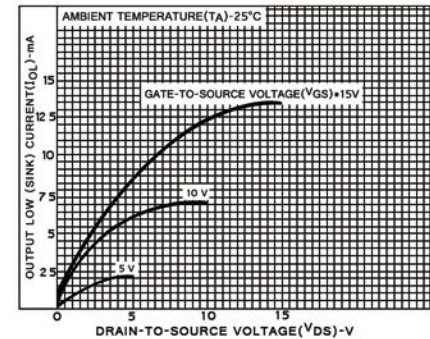


Fig. 2-Minimum output low (sink) current characteristics

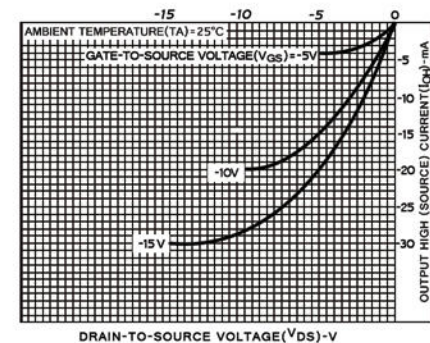


Fig.3-Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected to that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$)		3	18	V
Data Setup Time, t_S	5 10 15	150 70 40	-	ns
Strobe Pulse Width, t_W	5 10 15	250 100 25	-	ns

XL4514 SOP24/XD4514 DIP-24 XD74HC4514Z DIP-24/XD14514 DIP-24

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	VO (V)	VN (V)	VDD (V)	+25							
				-55	-40	+85	+125	Min	Typ	Max	
Quiescent Device Current, I _{DD} Max	-	0,5	5	5	5	150	150	-	0.04	5	μA
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
Output Low (Sink) Current I _{OL} Min	0,4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0,5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1,5	0,15	15	4.6	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current I _{OL} Min	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2,5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9,5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13,5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-level, VO _L Max	-	0,5	5	0.05			-	0	0.05	-	V
	-	0,10	10	0.05			-	0	0.05	-	
	-	0,15	15	0.05			-	0	0.05	-	
Output Voltage: High-Level, VO _H Min	-	0,5	5	4.95			4.95	5	-	-	V
	-	0,10	10	9.95			9.95	5	-	-	
	-	0,15	15	14.95			14.95	15	-	-	
Input Low Voltage, V _{IL} Max	0,5,4,5	-	5	1.5			-	-	1.5	-	V
	1,5	-	10	3			-	-	3	-	
	1,5,13,5	-	15	4			-	-	4	-	
Input High Voltage, V _{IH} Min	0,5,4,5	-	5	3.5			3.5	-	-	-	V
	1,9	-	10	7			7	-	-	-	
	1,5,13,5	-	15	11			11	-	-	-	
Input Current I _{IN} Max	-	0,18	18	±0.1	±0.1	±1	±1	-	+10 ⁻⁵	±0.1	μA

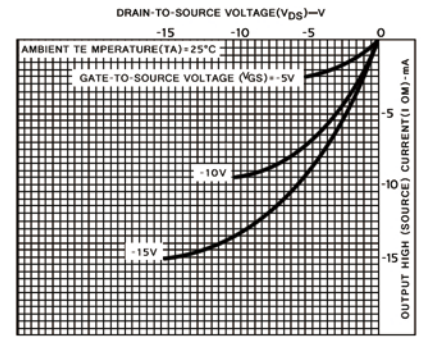


Fig.4-Minimum output high (source) current characteristics.

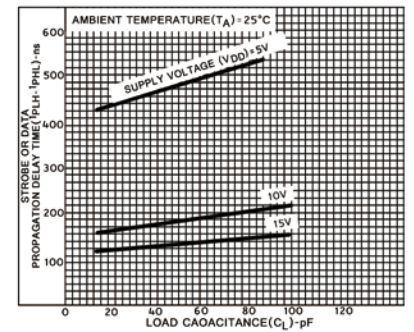


Fig.5-Typical strobe or data propagation delay time vs. load capacitance.

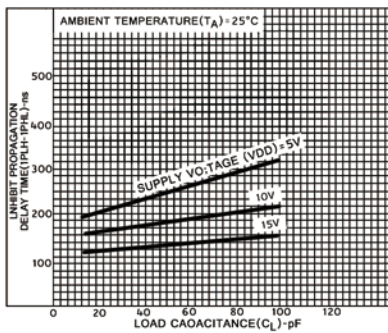


Fig.6-Typical inhibit propagation delay time vs. load capacitance.

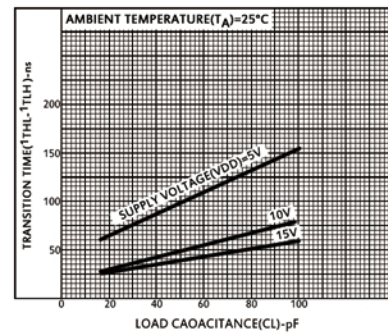


Fig.7-Typical Typical low-to-high transition time vs. load capacitance.

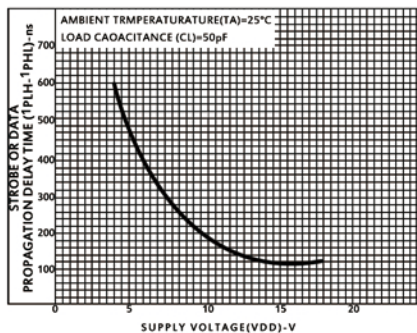


Fig.8-Typical strobe or data propagation delay time vs. supply voltage.

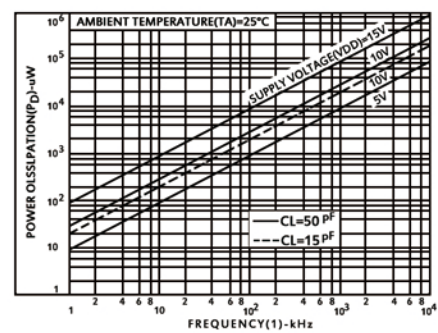


Fig.9-Typical power dissipation vs. frequency.

XL4514 SOP24/XD4514 DIP-24 XD74HC4514Z DIP 24/XD14514 DIP-24

DYNAMIC ELECTRICAL CHARACTERISTICS at TA = 25°C; Input tr,tf = 20 ns,
CL = 50 pF, RL = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		VDD V	Typ.		Max.
Propagation Delay Time: t _{pHL} , t _{pLH} Strobe or Data		5	485	970	ns
		10	185	370	
		15	135	270	
Inhibit		5	250	500	ns
		10	110	220	
		15	85	170	
Transition Time, t _{TLH} , t _{THL}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Strobe Pulse Width, t _w		5	125	250	ns
		10	50	100	
		15	40	75	
Minimum Data Setup Time, t _s		5	75	150	ns
		10	35	70	
		15	20	40	
Input Capacitance, C _{IN}	Any Input	-	5	7.5	pF

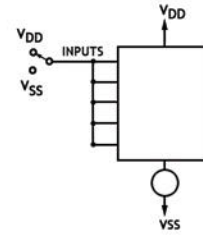


Fig.10-Quiescent device current test circuit.

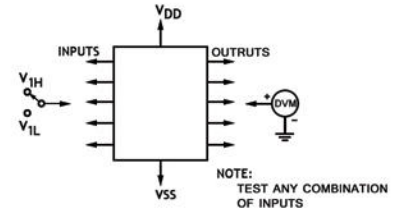


Fig.11-Input voltage test circuit

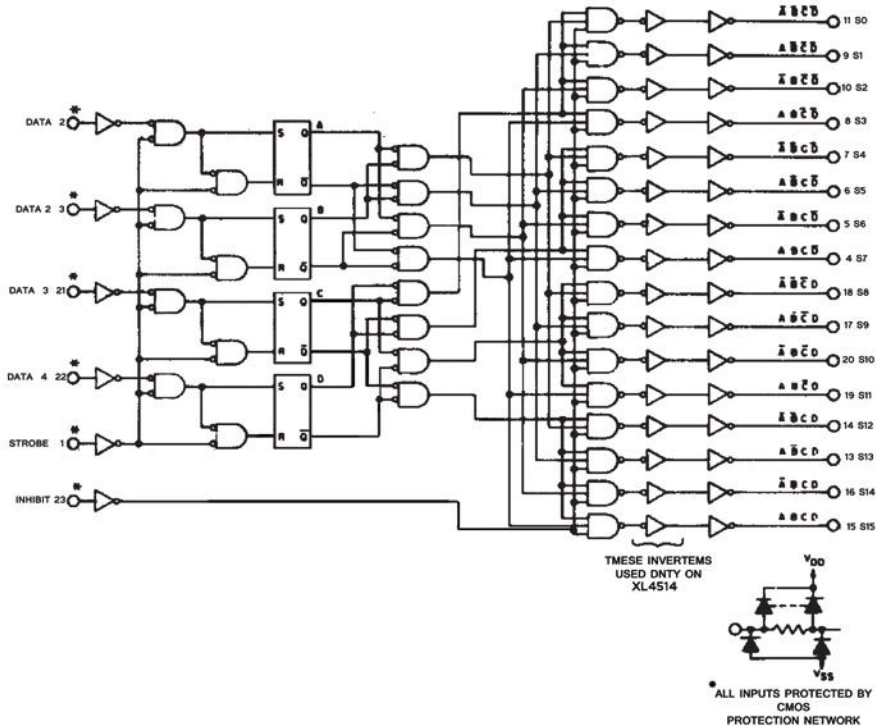


Fig.13-Logic diagram for XL4514 and XD4514

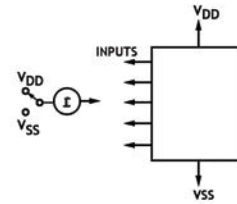


Fig. 12- Input current test circuit

XL4514 SOP24/XD4514 DIP-24 XD74HC4514Z DIP_窄24/XD14514 DIP-24

DECODER TRUTH TABLE(Strobr=1)

INHIBIT	DECODER INPUTS				SELECTED OUTPUT XL4514 = Logic 1(High) XD4514 = Logic 0(Low)
	B	C	B	A	
0	0	0	0	0	S0
	0	0	0	1	S1
	0	0	0	0	S2
	0	0	0	1	S3
0	0	1	0	0	S4
	0	1	0	1	S5
	0	1	1	0	S6
	0	1	1	1	S7
0	1	0	0	0	S8
	1	0	0	1	S9
	1	0	1	0	S10
	1	0	1	1	S11
0	1	1	0	0	S12
	1	1	0	1	S13
	1	1	1	0	S14
	1	1	1	1	S15
1	X	X	X	X	All Output= 0, XL4514 All Output= 1, XD4514

X = Don't Care Logic 1 = high Logic 0 = Low

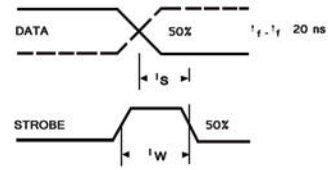
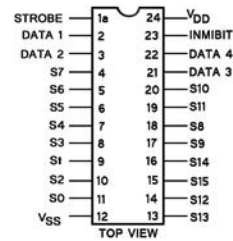
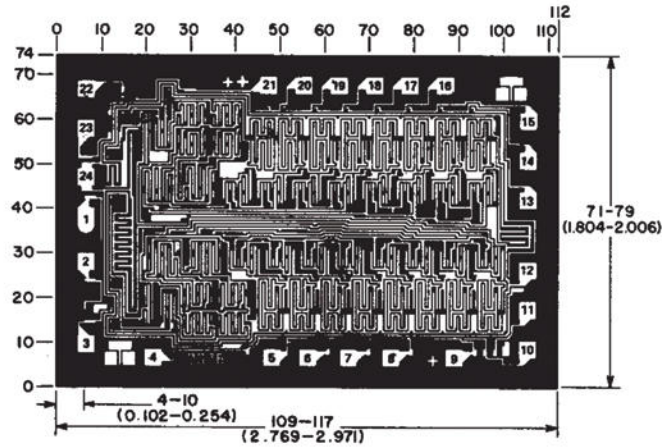


Fig.14-Waveforms for setup time and strobe pulse width



XL4514
XD4514

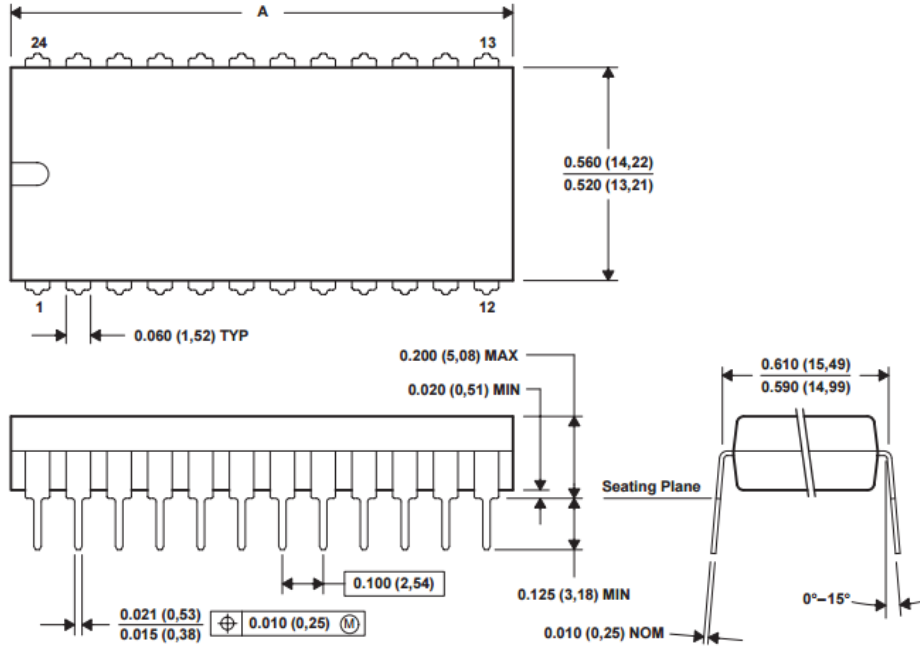
TERMINAL ASSIGNMENT



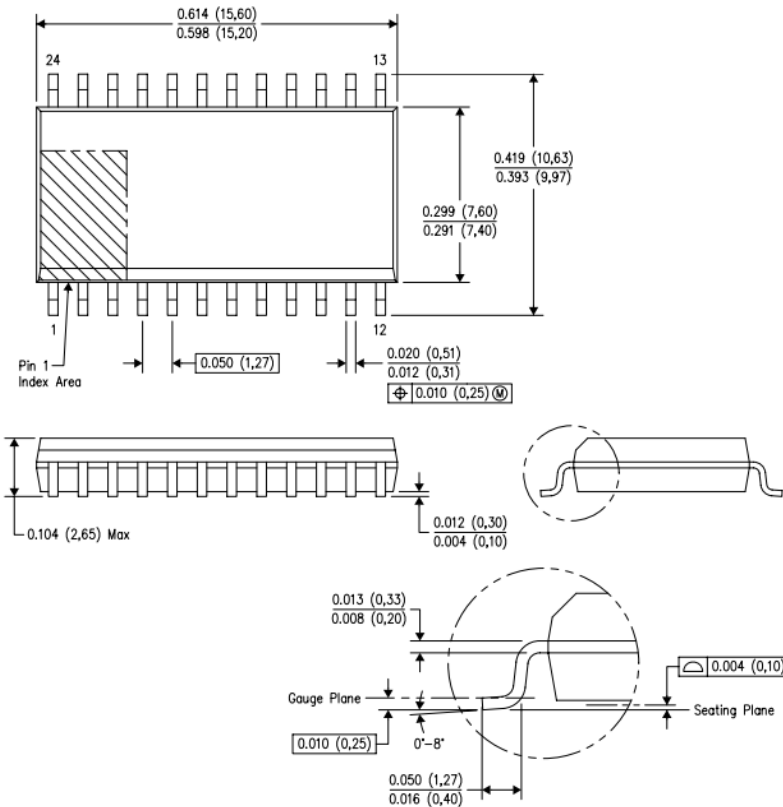
Dimensions and Pad Layout for XL4514 Chip
(Dimensions and pad layout for the XD4514 are identical)

Dimensions in paren theses are in millime ters and are derived from the basic inch dimensions as indicated.
Grid graduations are in mils (10⁻³ inch)

XL4514 SOP24/XD4514 DIP-24 XD74HC4514Z DIP窄24/XD14514 DIP-24



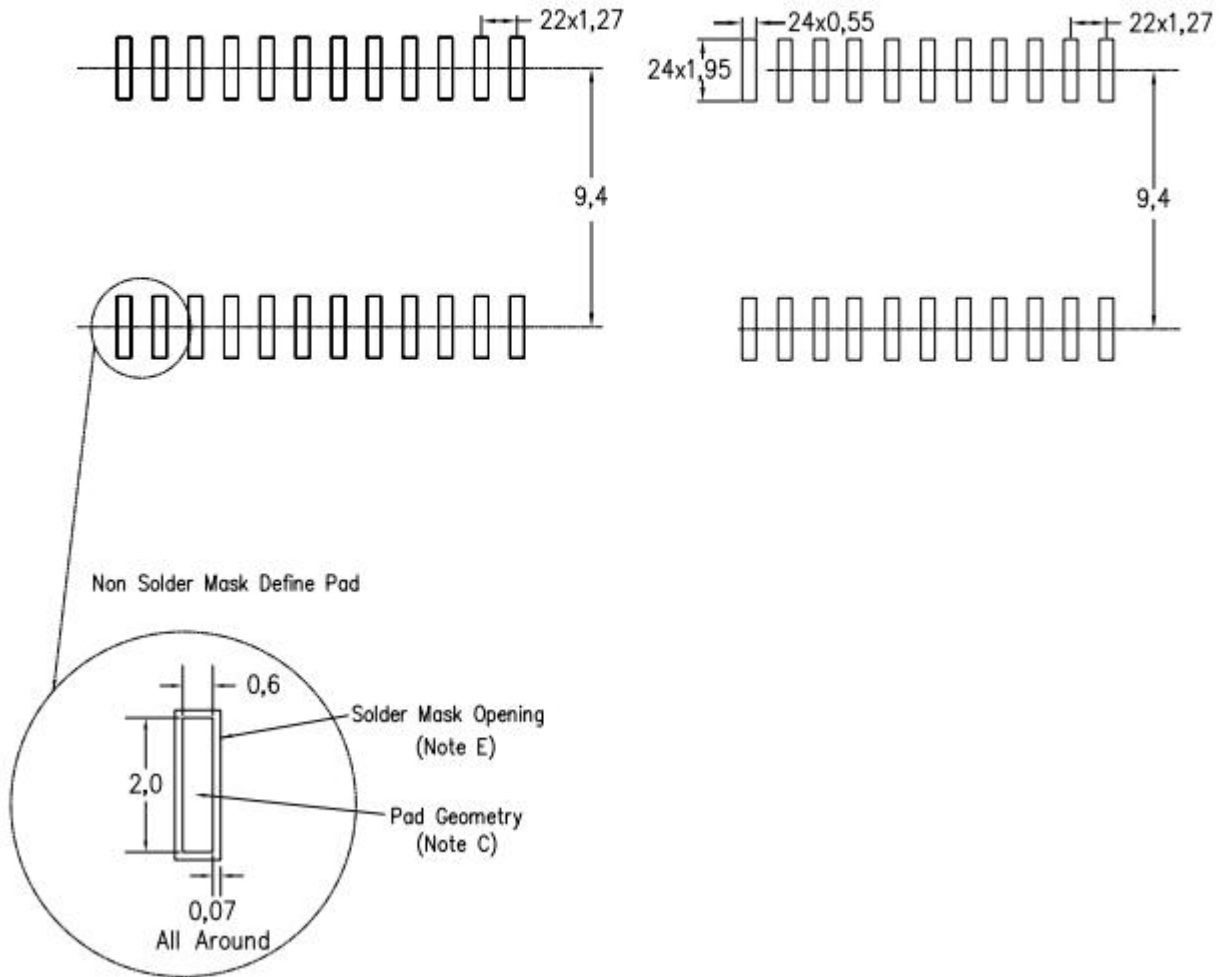
DIM \ PINS **	24	28	32	40	48	52
	A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)



XL4514 SOP24/XD4514 DIP-24
XD74HC4514Z DIP窄24/XD14514 DIP-24

Example Board Layout
(Note C)

Stencil Openings
(Note D)



以上信息仅供参考. 如需帮助联系客服人员。谢谢 XINLUDA