



SPECIFICATIONS<sup>1, 2</sup>

( $V_{DD} = DV_{DD} = 3.0\text{ V}$  or  $5.0\text{ V}$   $\pm 610\%$ ,  $REF_{IN}/REF_{OUT} = 2.5\text{ V}$  Internal Reference,  $MCLKIN = 11.0592\text{ MHz}$ ,  $f_{SAMPLE} = 200\text{ kHz}$ , DAC  $V_{OUT}$  Load to AGND;  $R_L = 2\text{ k}\Omega$ ,  $C_L = 100\text{ pF}$ . All specifications  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

Parameter	ADuC831BS		Unit	Test Conditions/Comments
	$V_{DD} = 5\text{ V}$	$V_{DD} = 3\text{ V}$		
<b>ADC CHANNEL SPECIFICATIONS</b>				
<b>DC ACCURACY<sup>3, 4</sup></b>				
Resolution	12	12	Bits	
Integral Nonlinearity	$\pm 1/2$	$\pm 1/2$	LSB typ	$f_{SAMPLE} = 100\text{ kHz}$
	$\pm 1.5$	$\pm 1.5$	LSB max	$f_{SAMPLE} = 100\text{ kHz}$
	$\pm 1.5$	$\pm 1.5$	LSB typ	$f_{SAMPLE} = 200\text{ kHz}$
Differential Nonlinearity	$\pm 1$	$\pm 1$	LSB typ	$f_{SAMPLE} = 100\text{ kHz}$ . Guaranteed No Missing Codes at 5 V
<b>CALIBRATED ENDPOINT ERRORS<sup>5, 6</sup></b>				
Offset Error	$\pm 5$	$\pm 5$	LSB max	
	$\pm 1$	$\pm 1$	LSB typ	
Offset Error Match	1	1	LSB typ	
Gain Error	$\pm 6$	$\pm 6$	LSB max	
	$\pm 1$	$\pm 1$	LSB typ	
Gain Error Match	1.5	1.5	LSB typ	
<b>USER SYSTEM CALIBRATION<sup>7</sup></b>				
Offset Calibration Range	$\pm 5$	$\pm 5$	% of $V_{REF}$ typ	
Gain Calibration Range	$\pm 2.5$	$\pm 2.5$	% of $V_{REF}$ typ	
<b>DYNAMIC PERFORMANCE</b>				
Signal-to-Noise Ratio (SNR) <sup>8</sup>	70	70	dB typ	$f_{IN} = 10\text{ kHz}$ Sine Wave $f_{SAMPLE} = 100\text{ kHz}$
Total Harmonic Distortion (THD)	-78	-78	dB typ	
Peak Harmonic or Spurious Noise	-78	-78	dB typ	
<b>ANALOG INPUT</b>				
Input Voltage Ranges	0 to $V_{REF}$	0 to $V_{REF}$	Volts	
Leakage Current	$\pm 1$	$\pm 1$	$\mu\text{A}$ max	
	$\pm 0.1$	$\pm 0.1$	$\mu\text{A}$ typ	
Input Capacitance <sup>9</sup>	20	20	pF max	
<b>TEMPERATURE SENSOR<sup>10</sup></b>				
Voltage Output at 25°C	600	600	mV typ	Can vary significantly ( $> \pm 20\%$ ) from device to device
Voltage TC	-3.0	-3.0	mV/°C typ	
Acquisition Time Required	1	1	$\mu\text{s}$ typ	
<b>DAC CHANNEL SPECIFICATIONS</b>				
<b>DC ACCURACY<sup>11</sup></b>				
Resolution	12	12	Bits	
Relative Accuracy	$\pm 3$	$\pm 3$	LSB typ	Guaranteed 12-Bit Monotonic
Differential Nonlinearity	$\pm 0.5$	$\pm 1$	LSB typ	
Offset Error	$\pm 60$	$\pm 60$	mV max	
	$\pm 15$	$\pm 15$	mV typ	
Full-Scale Error	$\pm 30$	$\pm 30$	mV max	
	$\pm 10$	$\pm 10$	mV typ	
Full-Scale Mismatch	$\pm 0.5$	$\pm 0.5$	% typ	% of Full-Scale on DAC1
<b>ANALOG OUTPUTS</b>				
Voltage Range_0	0 to $V_{REF}$	0 to $V_{REF}$	V typ	
Voltage Range_1	0 to $V_{DD}$	0 to $V_{DD}$	V typ	
Resistive Load	10	10	k $\Omega$ typ	
Capacitive Load	100	100	pF typ	
Output Impedance	0.5	0.5	$\Omega$ typ	
$I_{SINK}$	50	50	$\mu\text{A}$ typ	

ADuC831–SPECIFICATIONS<sup>1,2</sup>  
(continued)

Parameter	ADuC831BS		Unit	Test Conditions/Comments
	V <sub>DD</sub> = 5 V	V <sub>DD</sub> = 3 V		
<b>DAC AC CHARACTERISTICS</b>				
Voltage Output Settling Time	15	15	μs typ	Full-Scale Settling Time to Within 1/2 LSB of Final Value 1 LSB Change at Major Carry
Digital-to-Analog Glitch Energy	10	10	nV sec typ	
<b>REFERENCE INPUT/OUTPUT</b>				
REF <sub>IN</sub> Input Voltage Range <sup>9</sup>	2.3/V <sub>DD</sub>	2.3/V <sub>DD</sub>	V min/max	Initial Tolerance @ 25°C
Input Impedance	150	150	kΩ typ	
REF <sub>OUT</sub> Output Voltage	2.5 ±2.5%	2.5 ±2.5%	V min/max	
REF <sub>OUT</sub> Tempco	100	100	V typ ppm/°C typ	
<b>FLASH/EE MEMORY PERFORMANCE CHARACTERISTICS<sup>12, 13</sup></b>				
Endurance	100,000	100,000	Cycles min	
Data Retention	100	100	Years min	
<b>WATCHDOG TIMER CHARACTERISTICS</b>				
Oscillator Frequency	32	32	kHz typ	±10% Accurate
<b>TIME INTERVAL COUNTER</b>				
Oscillator Frequency	32	32	kHz typ	±10% Accurate
<b>POWER SUPPLY MONITOR (PSM)</b>				
AV <sub>DD</sub> Trip Point Selection Range	2.63 4.63		Vmin Vmax	Four Trip Points Selectable in This Range Programmed via TPA 1-0 IN PSMCON
AV <sub>DD</sub> Power Supply Trip Point Accuracy	±3.5		% max	
DV <sub>DD</sub> Trip Point Selection Range	2.63 4.63		Vmin Vmax	Four Trip Points Selectable in This Range Programmed via TPD1-0 in PSMCON
DV <sub>DD</sub> Power Supply Trip Point Accuracy	±3.5		% max	
<b>DIGITAL INPUTS</b>				
Input High Voltage (V <sub>INH</sub> )	2.4		V min	V <sub>IN</sub> = 0 V or V <sub>DD</sub> V <sub>IN</sub> = 0 V or V <sub>DD</sub>
XTAL1 Input High Voltage (V <sub>INH</sub> ) Only	4		V min	
Input Low Voltage (V <sub>INL</sub> )	0.8		V max	
Input Leakage Current (Port 0, EA)	±10 ±1	±1	μA max μA typ	
Logic 1 Input Current (All Digital Inputs)	±10 ±1	±1	μA max μA typ	V <sub>IN</sub> = V <sub>DD</sub> V <sub>IN</sub> = V <sub>DD</sub>
Logic 0 Input Current (Port 1, 2, 3)	-80 -40	-40	μA max μA typ	V <sub>IL</sub> = 450 mV
Logic 1-0 Transition Current (Port 1, 2, 3)	-700 -400	-400	μA max μA typ	V <sub>IL</sub> = 2 V V <sub>IL</sub> = 2 V
Input Capacitance	10	10	pF typ	

Parameter	ADuC831BS		Unit	Test Conditions/Comments
	V <sub>DD</sub> = 5 V	V <sub>DD</sub> = 3 V		
DIGITAL OUTPUTS				
Output High Voltage (V <sub>OH</sub> )	2.4		V min	V <sub>DD</sub> = 4.5 V to 5.5 V I <sub>SOURCE</sub> = 80 μA
	4.0	2.6	V typ	V <sub>DD</sub> = 2.7 V to 3.3 V I <sub>SOURCE</sub> = 20 μA
Output Low Voltage (V <sub>OL</sub> ) ALE, PSEN, Ports 0 and 2	0.4		V max	I <sub>SINK</sub> = 1.6 mA
	0.2	0.2	V typ	I <sub>SINK</sub> = 1.6 mA
Port 3	0.4		V max	I <sub>SINK</sub> = 8 mA
	0.2	0.2	V typ	I <sub>SINK</sub> = 8 mA
Floating State Leakage Current	±10		μA max	
	±5	±5	μA typ	
Floating State Output Capacitance	10	10	pF typ	
POWER REQUIREMENTS <sup>14, 15, 16</sup>				
I <sub>DD</sub> Normal Mode <sup>17</sup>	43		mA max	MCLKIN = 16 MHz
	32	16	mA typ	MCLKIN = 16 MHz
	26	12	mA typ	MCLKIN = 12 MHz
	8	3	mA typ	MCLKIN = 1 MHz
I <sub>DD</sub> Idle Mode	25		mA max	MCLKIN = 16 MHz
	18	17	mA typ	MCLKIN = 16 MHz
	15	6	mA typ	MCLKIN = 12 MHz
	7	2	mA typ	MCLKIN = 1 MHz
I <sub>DD</sub> Power-Down Mode <sup>18</sup>	50	50	μA max	
	5	5	μA typ	

## NOTES

<sup>1</sup>Specifications apply after calibration.

<sup>2</sup>Temperature range -40°C to +85°C.

<sup>3</sup>Linearity is guaranteed during normal MicroConverter Core operation.

<sup>4</sup>Linearity may degrade when programming or erasing the 640 Byte Flash/EE space during ADC conversion times due to on-chip charge pump activity.

<sup>5</sup>Measured in production at V<sub>DD</sub> = 5 V after Software Calibration Routine at 25°C only.

<sup>6</sup>User may need to execute Software Calibration Routine to achieve these specifications, which are configuration dependent.

<sup>7</sup>The offset and gain calibration spans are defined as the voltage range of user system offset and gain errors that the ADuC831 can compensate.

<sup>8</sup>SNR calculation includes distortion and noise components.

<sup>9</sup>Specification is not production tested, but is supported by characterization data at initial product release.

<sup>10</sup>The temperature sensor will give a measure of the die temperature directly; air temperature can be inferred from this result.

<sup>11</sup>DAC linearity is calculated using:

reduced code range of 48 to 4095, 0 to V<sub>REF</sub> range

reduced code range of 48 to 3995, 0 to V<sub>DD</sub> range

DAC output load = 10 kΩ and 50 pF.

<sup>12</sup>Flash/EE Memory Performance Specifications are qualified as per JEDEC Specification (Data Retention) and JEDEC Draft Specification A117 (Endurance).

<sup>13</sup>Endurance Cycling is evaluated under the following conditions:

Mode = Byte Programming, Page Erase Cycling

Cycle Pattern = 00Hex to FFHex

Erase Time = 20 ms

Program Time = 100 μs

<sup>14</sup>I<sub>DD</sub> at other MCLKIN frequencies is typically given by:

Normal Mode (V<sub>DD</sub> = 5 V): I<sub>DD</sub> = (1.6 nAs x MCLKIN) + 6 mA

Normal Mode (V<sub>DD</sub> = 3 V): I<sub>DD</sub> = (0.8 nAs x MCLKIN) + 3 mA

Idle Mode (V<sub>DD</sub> = 5 V): I<sub>DD</sub> = (0.75 nAs x MCLKIN) + 6 mA

Idle Mode (V<sub>DD</sub> = 3 V): I<sub>DD</sub> = (0.25 nAs x MCLKIN) + 3 mA

Where MCLKIN is the oscillator frequency in MHz and resultant I<sub>DD</sub> values are in mA.

<sup>15</sup>I<sub>DD</sub> Currents are expressed as a summation of analog and digital power supply currents during normal MicroConverter operation.

<sup>16</sup>I<sub>DD</sub> is not measured during Flash/EE program or erase cycles; I<sub>DD</sub> will typically increase by 10 mA during these cycles.

<sup>17</sup>Analog I<sub>DD</sub> = 2 mA (typ) in normal operation (internal V<sub>REF</sub>, ADC and DAC peripherals powered on).

<sup>18</sup>EA = Port0 = DV<sub>DD</sub>, XTAL1 (Input) tied to DV<sub>DD</sub>, during this measurement.

Typical specifications are not production tested, but are supported by characterization data at initial product release.

Specifications subject to change without notice.

Please refer to User Guide, Quick Reference Guide, Application Notes, and Silicon Errata Sheet at [www.analog.com/microconverter](http://www.analog.com/microconverter) for additional information.

# ADuC831

## ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = 25°C unless otherwise noted)

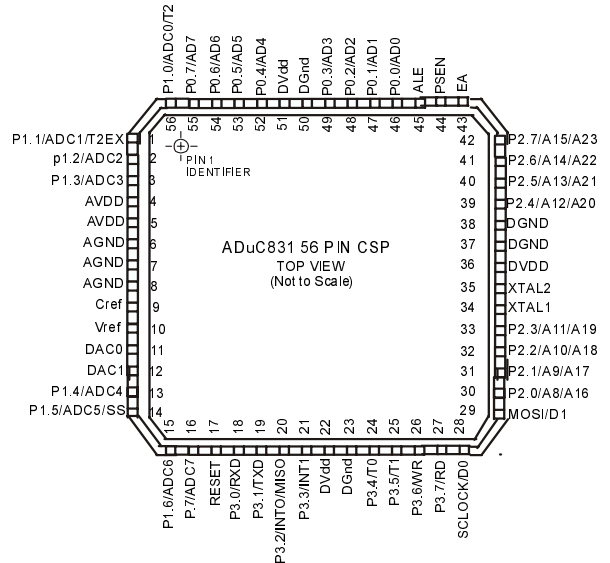
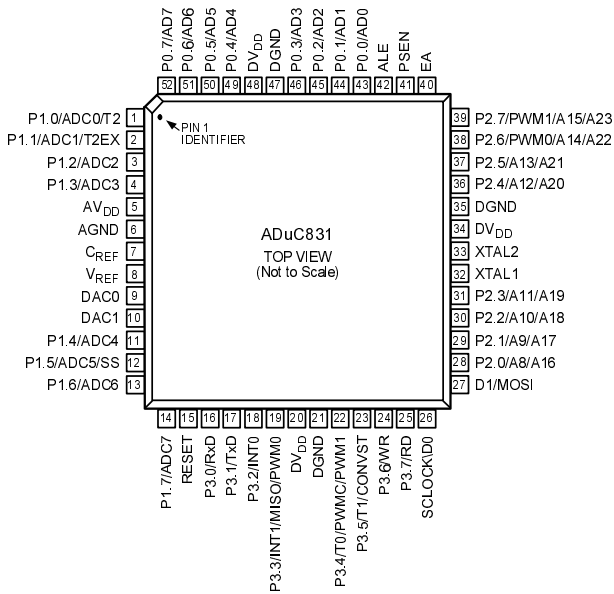
AV <sub>DD</sub> to DV <sub>DD</sub> .....	-0.3 V to +0.3 V
AGND to DGND .....	-0.3 V to +0.3 V
DV <sub>DD</sub> to DGND, AV <sub>DD</sub> to AGND .....	-0.3 V to +7 V
Digital Input Voltage to DGND .....	-0.3 V, DV <sub>DD</sub> + 0.3 V
Digital Output Voltage to DGND .....	-0.3 V, DV <sub>DD</sub> + 0.3 V
V <sub>REF</sub> to AGND .....	-0.3 V, AV <sub>DD</sub> + 0.3 V
Analog Inputs to AGND .....	-0.3 V, AV <sub>DD</sub> + 0.3 V
Operating Temperature Range Industrial (B Version)	
.....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	150°C
θ <sub>JA</sub> Thermal Impedance .....	90°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec) .....	215°C
Infrared (15 sec) .....	220°C

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADuC831BS	-40°C to +85°C	52-Lead Plastic Quad Flatpack	S-52
ADuC831BCP	-40°C to +85°C	56-Lead Chip Scale Package	CP-56

## PIN CONFIGURATION



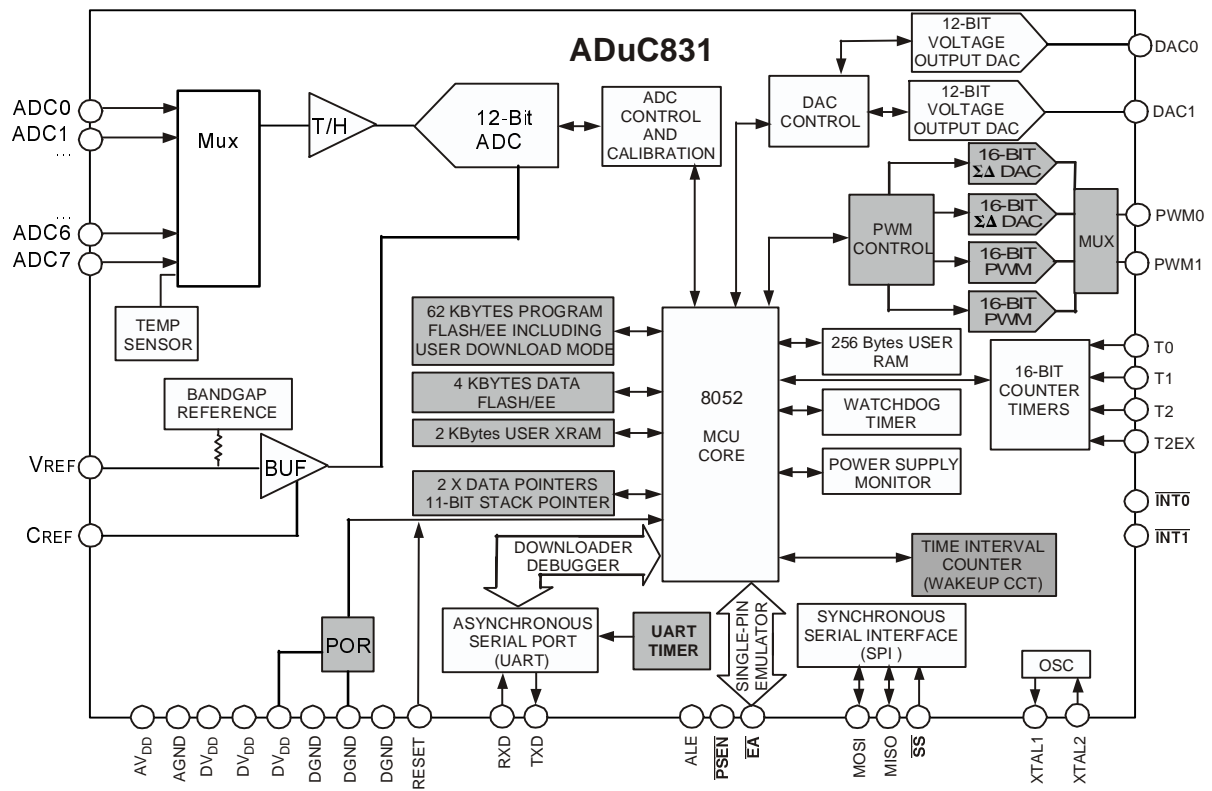


Figure 1 ADuC831 Block Diagram (Shaded areas are features not present on the ADuC812)

## PIN FUNCTION DESCRIPTIONS

Mnemonic	Type	Function
DV <sub>DD</sub>	P	Digital Positive Supply Voltage, 3 V or 5 V Nominal
AV <sub>DD</sub>	P	Analog Positive Supply Voltage, 3 V or 5 V Nominal
C <sub>REF</sub>	I	Decoupling Input for On-Chip Reference. Connect 0.1 $\mu$ F between this pin and AGND.
V <sub>REF</sub>	I/O	Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the reference source for the analog-to-digital converter. The nominal internal reference voltage is 2.5 V and this appears at the pin. This pin can be overdriven by an external reference.
AGND	G	Analog Ground. Ground Reference point for the analog circuitry.
P1.0-P1.7	I	Port 1 is an 8-bit Input Port only. Unlike other Ports, Port 1 defaults to Analog Input Mode, to configure any of these Port Pins as a digital input, write a "0" to the port bit. Port 1 pins are multifunction and share the following functionality.
ADC0-ADC7	I	Analog Inputs. Eight single-ended analog inputs. Channel selection is via ADCCON2 SFR.
T2	I	Timer 2 Digital Input. Input to Timer/Counter 2. When Enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input.
T2EX	I	Digital Input. Capture/Reload trigger for Counter 2 and also functions as an Up/Down control input for Counter 2.
SS	I	Slave Select Input for the SPI Interface
D1	O	Digital Output Pin
D0	O	Digital Output Pin
SCLOCK	I/O	Serial Clock Pin for Serial Interface Clock
MOSI	I/O	SPI Master Output/Slave Input Data I/O Pin for SPI Interface
MISO	I/O	SPI Master Input/Slave Output Data I/O Pin for SPI Serial Interface
DAC0	O	Voltage Output from DAC0
DAC1	O	Voltage Output from DAC1
RESET	I	Digital Input. A high level on this pin for 24 master clock cycles while the oscillator is running resets the device.
P3.0-P3.7	I/O	Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs Port 3 pins being pulled externally low will source current because of the internal pull-up resistors. Port 3 pins also contain various secondary functions which are described below.
PWMC	I	PWM Clock Input
PWM0	O	PMW0 Voltage Output. PWM outputs can be configured to uses ports 2.6 & 2.7 or 3.3 and 3.4
PWM1	O	PMW1 Voltage Output. See CFG831 Register for further Information.
RxD	I/O	Receiver Data Input (Asynchronous) or Data Input/Output (Synchronous) of Serial (UART) Port
TxD	O	Transmitter Data Output (Asynchronous) or Clock Output (Synchronous) of Serial (UART) Port
INT0	I	Interrupt 0, programmable edge or level triggered Interrupt input, which can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 0.
INT1	I	Interrupt 1, programmable edge or level triggered Interrupt input, which can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 1.
T0	I	Timer/Counter 0 Input
T1	I	Timer/Counter 1 Input
CONVST	I	Active low Convert Start Logic input for the ADC block when the external Convert start function is enabled. A low-to-high transition on this input puts the track/hold into its hold mode and starts conversion.
WR	O	Write Control Signal, Logic Output. Latches the data byte from Port 0 into the external data memory.
RD	O	Read Control Signal, Logic Output. Enables the external data memory to Port 0.
XTAL2	O	Output of the Inverting Oscillator Amplifier
XTAL1	I	Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
DGND	G	Digital Ground. Ground reference point for the digital circuitry.
P2.0-P2.7 (A8-A15) (A16-A23)	I/O	Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory and middle and high order address bytes during accesses to the external 24-bit external data memory space.

## PIN FUNCTION DESCRIPTION (continued)

Mnemonic	Type	Function
PSEN	O	Program Store Enable, Logic Output. This output is a control signal that enables the external program memory to the bus during external fetch operations. It is active every six oscillator periods except during external data memory accesses. This pin remains high during internal program execution. PSEN can also be used to enable serial download mode when pulled low through a resistor on power-up or RESET.
ALE	O	Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit address space accesses) of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
EA	I	External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000H to 1FFFFH. When held low this input enables the device to fetch all instructions from external program memory.
P0.7–P0.0 (A0–A7)	I/O	Port 0 is an 8-Bit Open Drain Bidirectional I/O port. Port 0 pins that have 1s written to them float and in that state can be used as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-ups when emitting 1s.

**TERMINOLOGY****ADC SPECIFICATIONS****Integral Nonlinearity**

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function.

The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition and full scale, a point 1/2 LSB above the last code transition.

**Differential Nonlinearity**

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Offset Error**

This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, i.e., +1/2 LSB.

**Gain Error**

This is the deviation of the last code transition from the ideal AIN voltage (Full Scale – 1.5 LSB) after the offset error has been adjusted out.

**Signal to (Noise + Distortion) Ratio**

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ( $f_s/2$ ), excluding dc.

The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02N + 1.76) \text{ dB}$$

Thus for a 12-bit converter, this is 74 dB.

**Total Harmonic Distortion**

Total Harmonic Distortion is the ratio of the rms sum of the harmonics to the fundamental.

**DAC SPECIFICATIONS****Relative Accuracy**

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

**Voltage Output Settling Time**

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

**Digital-to-Analog Glitch Impulse**

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV sec.

**Full-Scale Error**

This is the deviation of the full scale output voltage from the ideal.