ANALOG DEVICES

HMC463LP5 / 463LP5E

v09.0717

GaAs pHEMT MMIC LOW NOISE AGC AMPLIFIER, 2 - 20 GHz

Typical Applications

The HMC463LP5(E) is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military EW, ECM & C³I
- Test Instrumentation
- Fiber Optics

Features

Gain: 13 dB

Noise Figure: 2.8 dB @ 10 GHz

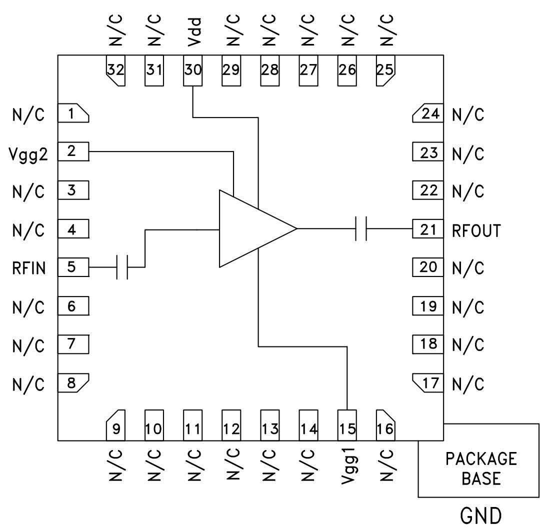
P1dB Output Power: +18 dBm @ 10 GHz

Supply Voltage: +5V @ 60mA

50 Ohm Matched Input/Output

32 Lead 5x5mm SMT Package: 25mm²

Functional Diagram



General Description

The HMC463LP5(E) is a GaAs MMIC pHEMT Low Noise AGC Distributed Amplifier packaged in a leadless 5x5 mm surface mount package which operates between 2 and 20 GHz. The amplifier provides 13 dB of gain, 2.8 dB noise figure and 18 dBm of output power at 1 dB gain compression while requiring only 60mA from a +5V supply. An optional gate bias (Vgg2) is provided to allow Adjustable Gain Control (AGC) of 8 dB typical. Gain flatness is excellent at ±0.5 dB from 6 - 18 GHz making the HMC463LP5(E) ideal for EW, ECM RADAR and test equipment applications. The HMC463LP5(E) LNA I/Os are internally matched to 50 Ohms and are internally DC blocked.

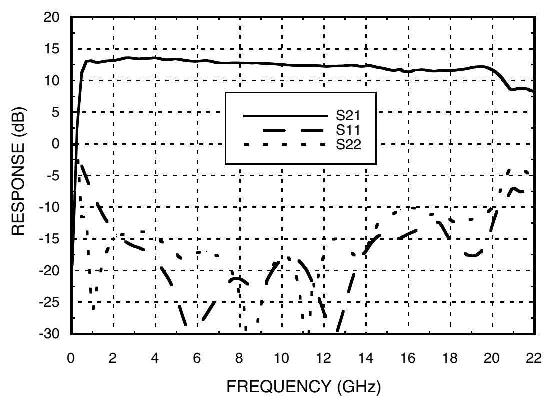
Electrical Specifications, T_A = +25 °C, Vdd = 5V, Idd = 60 mA*

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		2 - 6			6 - 18			18 - 20		GHz
Gain	10	13		9	12		8	11		dB
Gain Flatness		±0.5			±0.5			±0.5		dB
Gain Variation Over Temperature		0.010	0.015		0.010	0.015		0.010	0.015	dB/ °C
Noise Figure		3	4		3	5		5.5	6.5	dB
Input Return Loss		15			13			12		dB
Output Return Loss		13			10			10		dB
Output Power for 1 dB Compression (P1dB)	16	19		11	16		10	12		dBm
Saturated Output Power (Psat)		21			19			19		dBm
Output Third Order Intercept (IP3)		30			24			22		dBm
Supply Current (Idd) (Vdd = 5V, Vgg1 = -0.9V Typ.)		60	80		60	80		60	80	mA

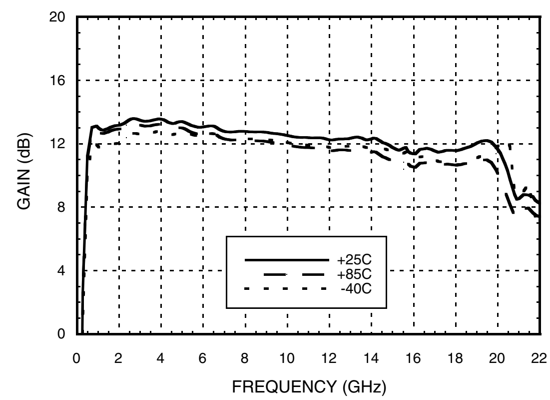
** Adjust Vgg1 between -2 to -0V to achieve Idd = 60 mA typical.*

*For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D*

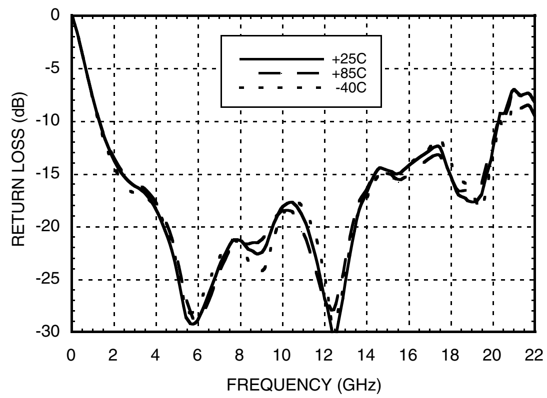
Gain & Return Loss



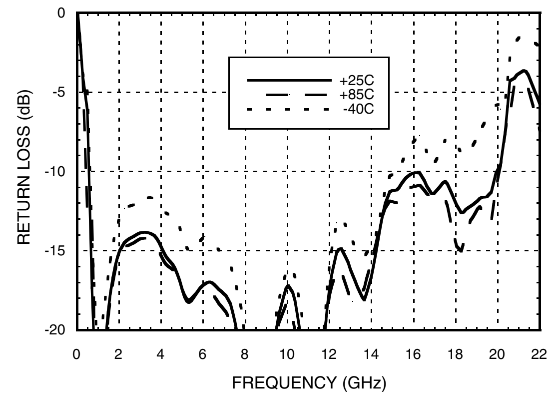
Gain vs. Temperature



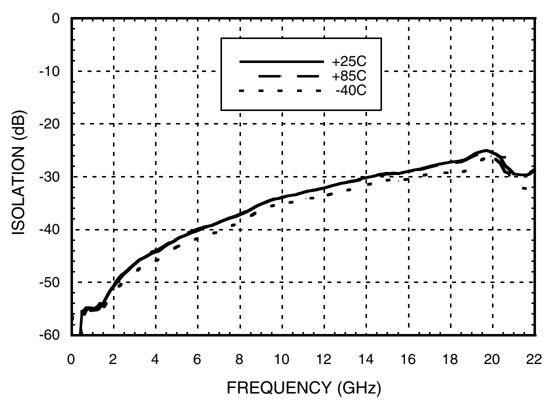
Input Return Loss vs. Temperature



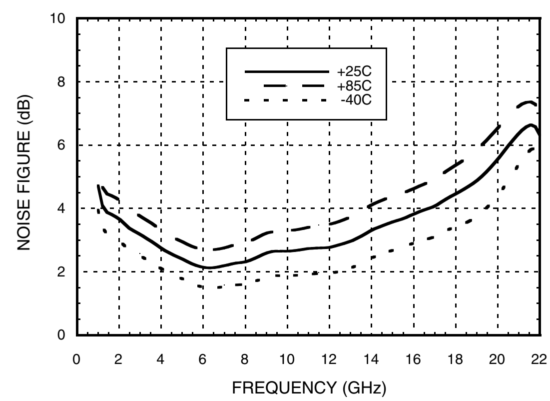
Output Return Loss vs. Temperature



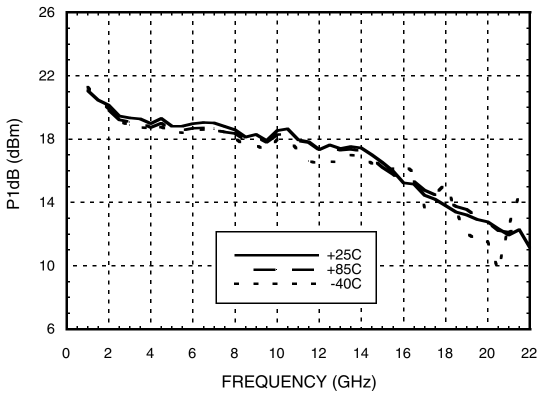
Reverse Isolation vs. Temperature



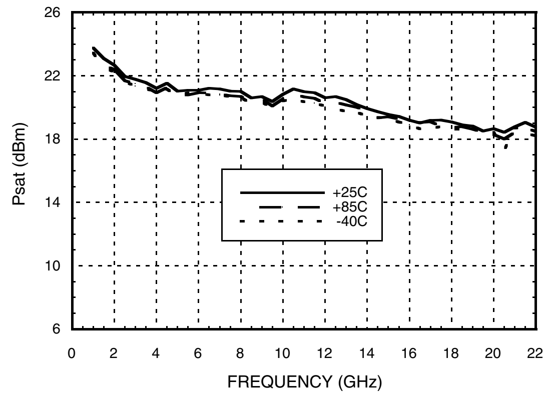
Noise Figure vs. Temperature



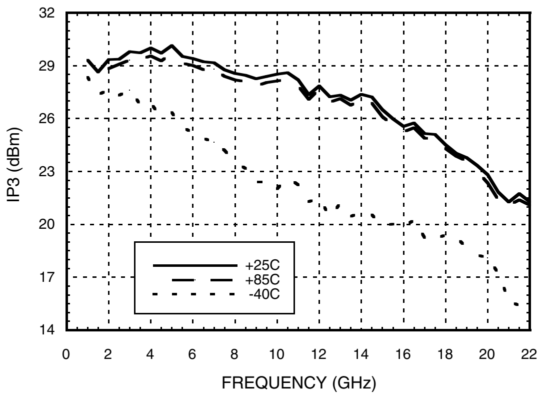
P1dB vs. Temperature



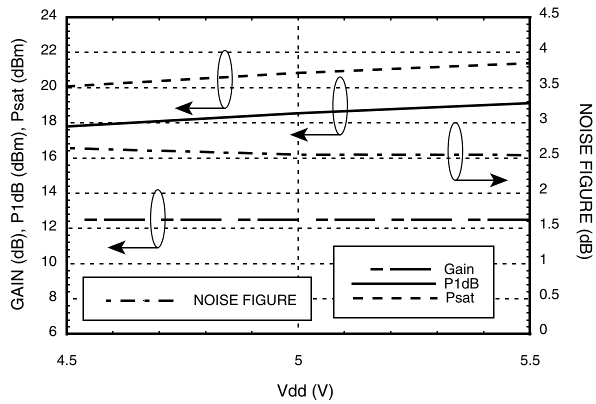
Psat vs. Temperature



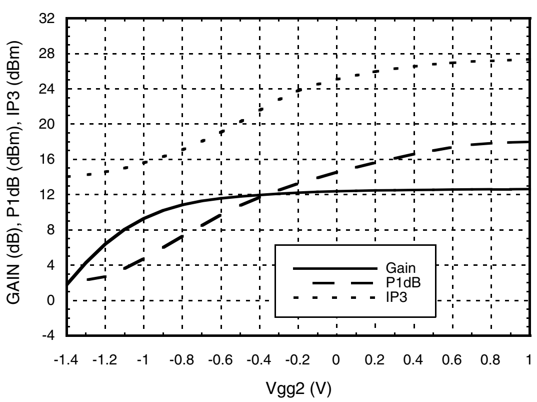
Output IP3 vs. Temperature



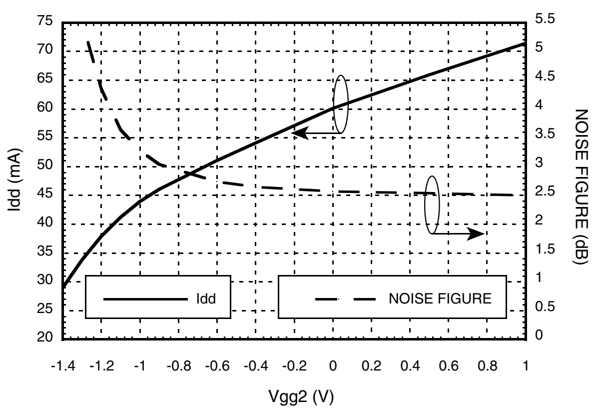
Gain, Power & Noise Figure vs. Supply Voltage @ 10 GHz, Fixed Vgg1



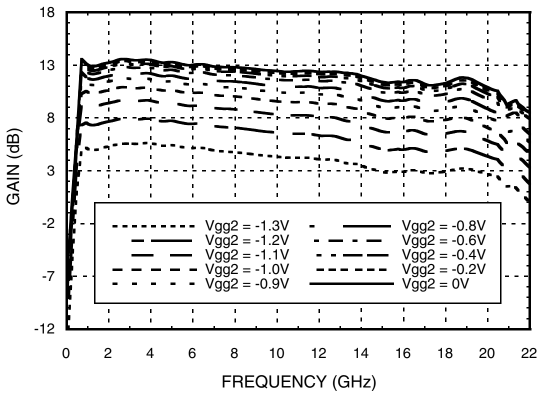
Gain, P1dB & Output IP3 vs. Control Voltage @ 10 GHz

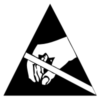


Noise Figure & Supply Current vs. Control Voltage @ 10 GHz



Gain @ Several Control Voltages (Vgg2)





ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

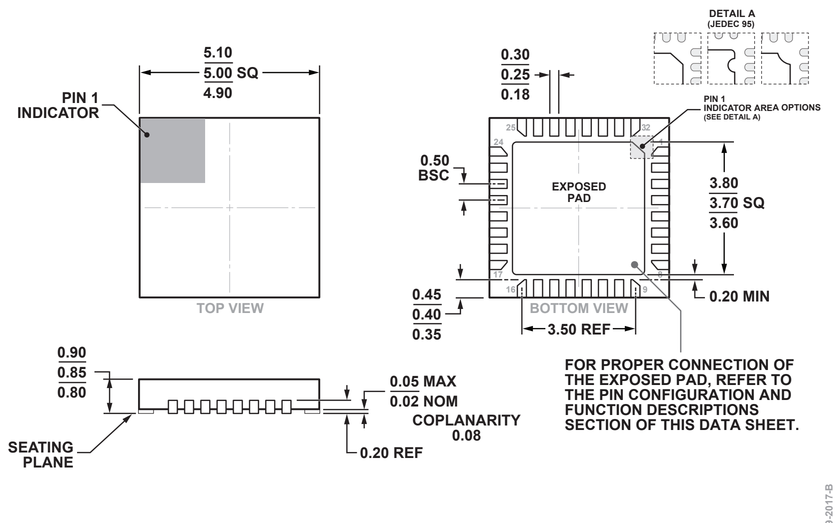
Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+9V
Gate Bias Voltage (Vgg1)	-2 to 0V
Gate Bias Current (Igg1)	2.5 mA
Gate Bias Voltage (Vgg2)(AGC)	(Vdd -9) Vdc to +2V
RF Input Power (RFIN)(Vdd = +5V)	+18 dBm
Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 19.1 mW/°C above 85 °C)	1.24 W
Thermal Resistance (channel to ground paddle)	52.3 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 0B - Passed 150V

Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+4.5	58
+5.0	60
+5.5	62

Outline Drawing



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-4.

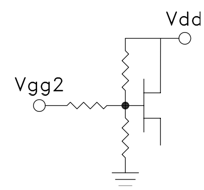
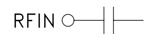
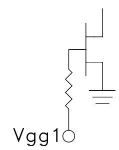
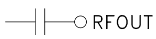
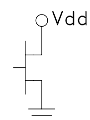
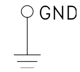
32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.90 mm Package Height
(HCP-32-1)
Dimensions shown in millimeters

Package Information

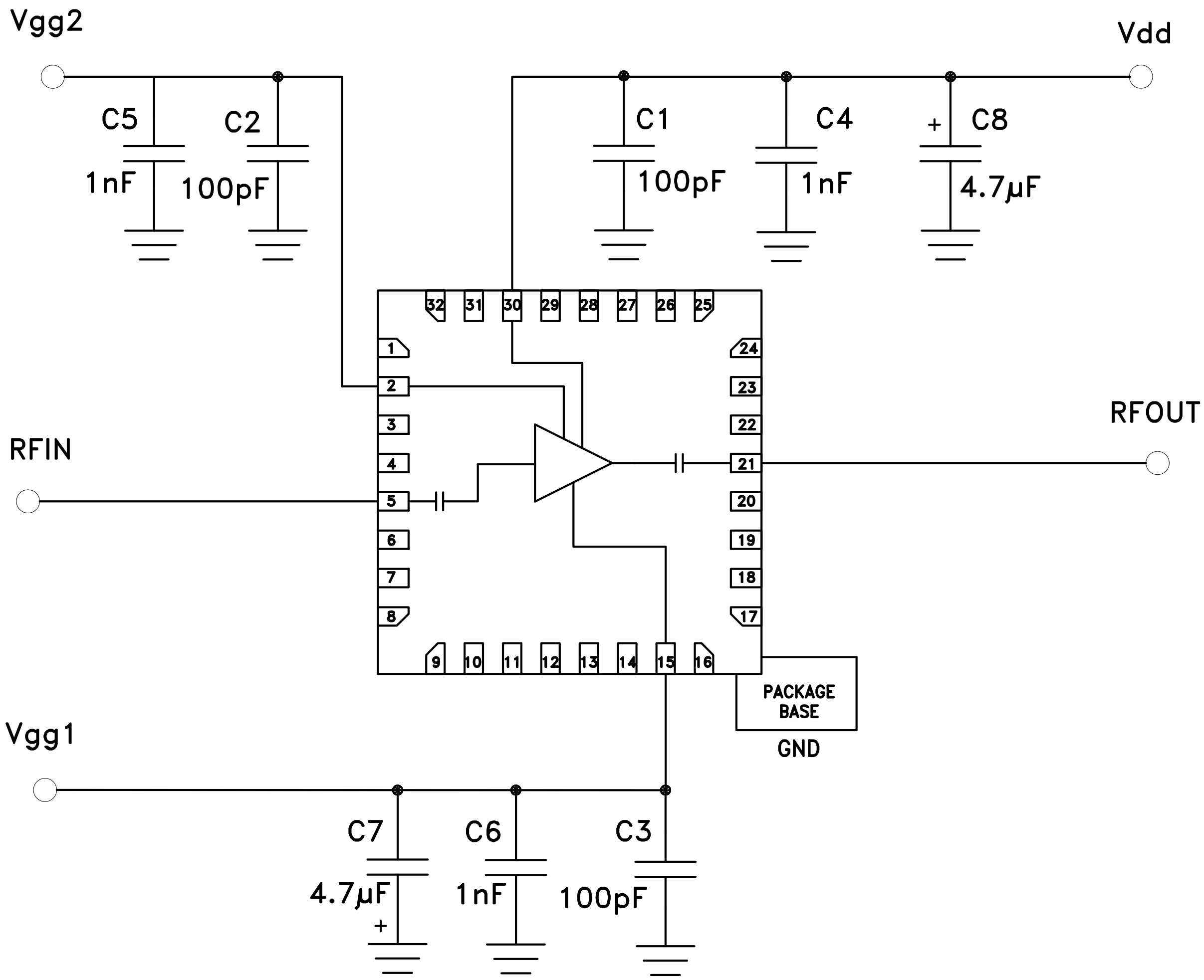
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC463LP5	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H463 XXXX
HMC463LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	<u>H463</u> XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

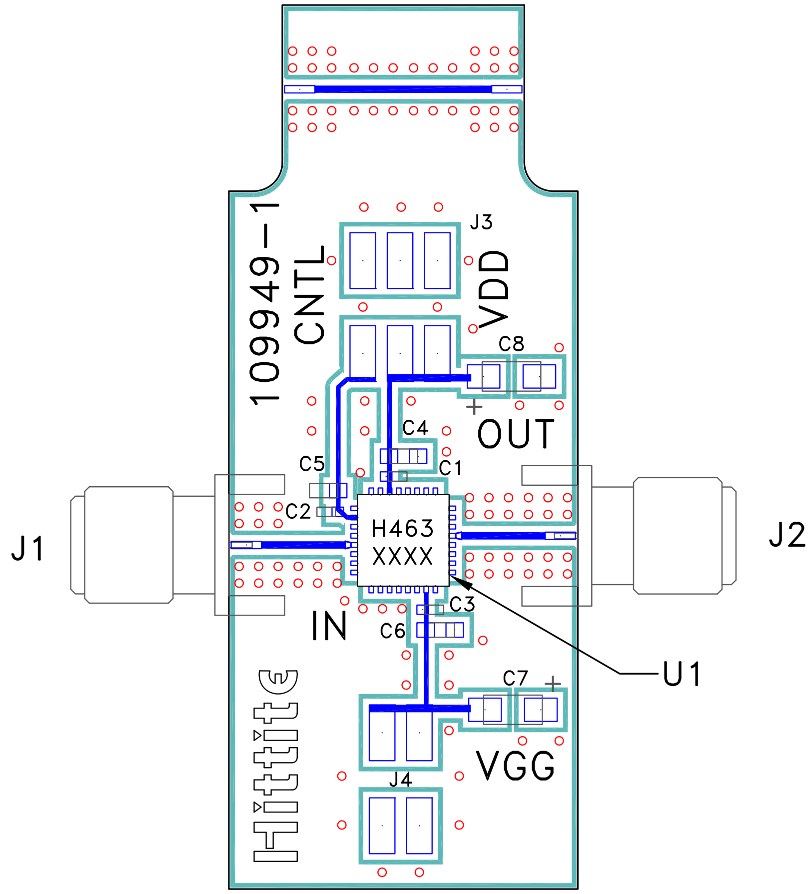
Pin Number	Function	Description	Interface Schematic
1, 3, 4, 6-14, 16-20, 22-29, 31, 32	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
2	Vgg2	Optional gate control if AGC is required. Leave Vgg2 open circuited if AGC is not required. Typical Vgg2 = -1.5V to 0V	
5	RFIN	This pad is AC coupled and matched to 50 Ohms	
15	Vgg1	Gate control for amplifier. Adjust to achieve Idd = 60mA.	
21	RFOUT	This pad is AC coupled and matched to 50 Ohms	
30	Vdd	Power supply voltage for the amplifier. External bypass capacitors are required	
Ground Paddle	GND	Ground paddle must be connected to RF/DC ground.	

Application Circuit



For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Evaluation PCB



List of Materials for Evaluation PCB 108341 [1]

Item	Description
J1 - J2	SRI K Connector
J3 - J4	2 mm Molex Header
C1 - C3	100 pF Capacitor, 0402 Pkg.
C4 - C6	1000 pF Capacitor, 0603 Pkg.
C7 - C8	4.7 µF Capacitor, Tantalum
U1	HMC463LP5(E) Amplifier
PCB [2]	109949 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Analog Devices upon request.