

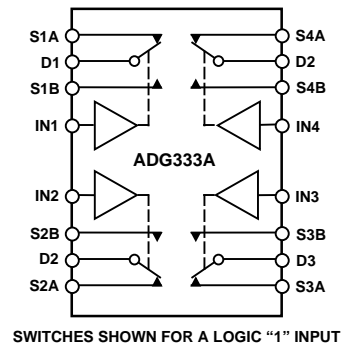
### FEATURES

- 44 V Supply Maximum Ratings
- $V_{SS}$  to  $V_{DD}$  Analog Signal Range
- Low On Resistance (45  $\Omega$  max)
- Low  $\Delta R_{ON}$  (5  $\Omega$  max)
- Low  $R_{ON}$  Match (4  $\Omega$  max)
- Low Power Dissipation
- Fast Switching Times
  - $t_{ON} < 175$  ns
  - $t_{OFF} < 145$  ns
- Low Leakage Currents (5 nA max)
- Low Charge Injection (10 pC max)
- Break-Before-Make Switching Action

### APPLICATIONS

- Audio and Video Switching
- Battery Powered Systems
- Test Equipment
- Communication Systems

### FUNCTIONAL BLOCK DIAGRAM



### GENERAL DESCRIPTION

The ADG333A is a monolithic CMOS device comprising four independently selectable SPDT switches. It is designed on an LC<sup>2</sup>MOS process which provides low power dissipation yet achieves a high switching speed and a low on resistance.

The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the part suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the part ideally suited for portable, battery powered instruments.

When they are ON, each switch conducts equally well in both directions and has an input signal range which extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

### PRODUCT HIGHLIGHTS

1. **Extended Signal Range**  
The ADG333A is fabricated on an enhanced LC<sup>2</sup>MOS process, giving an increased signal range which extends to the supply rails.
2. **Low Power Dissipation**
3. **Low  $R_{ON}$**
4. **Single Supply Operation**  
For applications where the analog signal is unipolar, the ADG333A can be operated from a single rail power supply. The part is fully specified with a single +12 V supply.

### REV. 0

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.  
Tel: 617/329-4700 Fax: 617/326-8703

# ADG333A—SPECIFICATIONS<sup>1</sup>

DUAL SUPPLY ( $V_{DD} = +15\text{ V}$ ,  $V_{SS} = -15\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	+25°C	-40°C to +85°C	Units	Test Conditions/Comments
<b>ANALOG SWITCH</b>				
Analogue Signal Range		$V_{SS}$ to $V_{DD}$	V	
$R_{ON}$	20		$\Omega$ typ	$V_D = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$
	45	45	$\Omega$ max	
$\Delta R_{ON}$		5	$\Omega$ max	$V_D = \pm 5\text{ V}$ , $I_S = -10\text{ mA}$
$R_{ON}$ Match		4	$\Omega$ max	$V_D = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.1$		nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
	$\pm 0.25$	$\pm 3$	nA max	$V_D = \pm 15.5\text{ V}$ , $V_S = +15.5\text{ V}$
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.1$		nA typ	Test Circuit 2
	$\pm 0.4$	$\pm 5$	nA max	$V_S = V_D = \pm 15.5\text{ V}$
				Test Circuit 3
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current				
$I_{INL}$ or $I_{INH}$		$\pm 0.005$	$\mu\text{A}$ typ	$V_{IN} = 0\text{ V}$ or $V_{DD}$
		$\pm 0.5$	$\mu\text{A}$ max	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	90		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ;
		175	ns max	$V_S = \pm 10\text{ V}$ ; Test Circuit 4
$t_{OFF}$	80		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ;
		145	ns max	$V_S = \pm 10\text{ V}$ ; Test Circuit 4
Break-Before-Make Delay, $t_{OPEN}$	10		ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ;
Charge Injection	2		pC typ	$V_S = +5\text{ V}$ ; Test Circuit 5
	10		pC max	$V_D = 0\text{ V}$ , $R_D = 0\ \Omega$ , $C_L = 10\text{ nF}$ ;
OFF Isolation	72		dB typ	$V_{DD} = +15\text{ V}$ , $V_{SS} = -15\text{ V}$ ; Test Circuit 6
Channel-to-Channel Crosstalk	85		dB typ	$R_L = 75\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ;
				$V_S = 2.3\text{ V rms}$ , Test Circuit 7
$C_S$ (OFF)	5		pF typ	$R_L = 75\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ;
$C_D$ , $C_S$ (ON)	20		pF typ	$V_S = 2.3\text{ V rms}$ , Test Circuit 8
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.05		mA typ	Digital Inputs = 0 V or 5 V
	0.25	0.35	mA max	
$I_{SS}$	0.01		$\mu\text{A}$ typ	
	1	5	$\mu\text{A}$ max	
$V_{DD}/V_{SS}$		$\pm 3/\pm 20$	V min/V max	$ V_{DD}  =  V_{SS} $

## NOTES

<sup>1</sup>Temperature range is as follows: B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**SINGLE SUPPLY** ( $V_{DD} = +12\text{ V}$ ,  $V_{SS} = 0\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	+25°C	-40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH Analog Signal Range $R_{ON}$	35	0 to $V_{DD}$ 75	V $\Omega$ typ $\Omega$ max	$V_D = +1\text{ V}$ , $+10\text{ V}$ , $I_S = -1\text{ mA}$
LEAKAGE CURRENTS Source OFF Leakage $I_S$ (OFF)  Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.1$ $\pm 0.25$ $\pm 0.1$ $\pm 0.4$	$\pm 3$ $\pm 5$	nA typ nA max nA typ nA max	$V_{DD} = +13.2\text{ V}$ $V_D = 12.2\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/12.2\text{ V}$ Test Circuit 2 $V_S = V_D = 12.2\text{ V}/1\text{ V}$ Test Circuit 3
DIGITAL INPUTS Input High Voltage, $V_{INH}$ Input Low Voltage, $V_{INL}$ Input Current $I_{INL}$ or $I_{INH}$		2.4 0.8 $\pm 0.005$ $\pm 0.5$	V min V max $\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = 0\text{ V}$ or $V_{DD}$
DYNAMIC CHARACTERISTICS <sup>2</sup> $t_{ON}$ $t_{OFF}$ Break-Before-Make Delay, $t_{OPEN}$ Charge Injection OFF Isolation Channel-to-Channel Crosstalk  $C_S$ (OFF) $C_D$ , $C_S$ (ON)	110 100 10 5 72 85 5 20	200 180	ns typ ns max ns typ ns max ns min ns min pC typ dB typ dB typ pF typ pF typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +8\text{ V}$ ; Test Circuit 4 $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +8\text{ V}$ ; Test Circuit 4 $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +5\text{ V}$ ; Test Circuit 5 $V_D = 6\text{ V}$ , $R_D = 0\ \Omega$ , $C_L = 10\text{ nF}$ ; $V_{DD} = +12\text{ V}$ , $V_{SS} = -0\text{ V}$ ; Test Circuit 6 $R_L = 75\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; $V_S = 1.15\text{ V rms}$ , Test Circuit 7 $R_L = 75\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; $V_S = 1.15\text{ V rms}$ , Test Circuit 8
POWER REQUIREMENTS $I_{DD}$  $V_{DD}$	0.05 0.25	0.35 +3/+30	mA typ mA max V min/V max	$V_{DD} = +13.5\text{ V}$ Digital Inputs = $0\text{ V}$ or $5\text{ V}$

## NOTES

<sup>1</sup>Temperature range is as follows: B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG333A

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> . . . . .	+44 V
V <sub>DD</sub> to GND . . . . .	-0.3 V to +30 V
V <sub>SS</sub> to GND . . . . .	+0.3 V to -30 V
Analog, Digital Inputs <sup>2</sup> . . . . .	V <sub>SS</sub> - 2 V to V <sub>DD</sub> + 2 V or 20 mA, Whichever Occurs First
Continuous Current, S or D . . . . .	20 mA
Peak Current, S or D . . . . .	40 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range	
Industrial (B Version) . . . . .	-40°C to +85°C
Storage Temperature Range . . . . .	-65°C to +125°C
Junction Temperature . . . . .	+150°C
Plastic Package	
θ <sub>JA</sub> , Thermal Impedance . . . . .	103°C/W
Lead Temperature, Soldering (10 sec) . . . . .	+260°C

## SOIC Package

θ <sub>JA</sub> , Thermal Impedance . . . . .	74°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec) . . . . .	+215°C
Infrared (15 sec) . . . . .	+220°C

## SSOP Package

θ <sub>JA</sub> , Thermal Impedance . . . . .	130°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec) . . . . .	+215°C
Infrared (15 sec) . . . . .	+220°C

## NOTES

<sup>1</sup>Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG333A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG333ABN	-40°C to +85°C	N-20
ADG333ABR	-40°C to +85°C	R-20
ADG333ABRS	-40°C to +85°C	RS-20

\*N = Plastic DIP, R = Small Outline IC (SOIC). RS = Shrink Small Outline Package (SSOP).

Table I. Truth Table

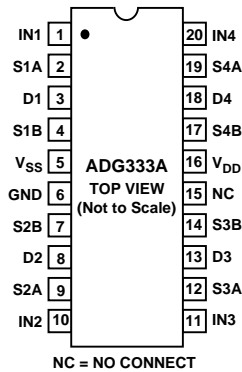
Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

**TERMINOLOGY**

S	Source Terminal. May be an input or output.	$C_D, C_S$ (ON)	“ON” Switch Capacitance.
D	Drain Terminal. May be an input or output.	$t_{ON}$	Delay between applying the digital control input and the output switching on.
IN	Logic Control Input.	$t_{OFF}$	Delay between applying the digital control input and the output switching off.
$R_{ON}$	Ohmic resistance between D and S.	$t_{OPEN}$	Break Before Make delay when switches are configured as a multiplexer.
$\Delta R_{ON}$	$R_{ON}$ variation due to a change in the analog input voltage with a constant load current.	$V_{INL}$	Maximum input voltage for logic “0.”
$R_{ON}$ Match	Difference between the $R_{ON}$ of any two channels.	$V_{INH}$	Minimum input voltage for logic “1.”
$I_S$ (OFF)	Source leakage current with the switch “OFF.”	$I_{INL}$ ( $I_{INH}$ )	Input current of the digital input.
$I_D$ (OFF)	Drain leakage current with the switch “OFF.”	Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
$I_D, I_S$ (ON)	Channel leakage current with the switch “ON.”	Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
$V_D$ ( $V_S$ )	Analog voltage on terminals D, S.	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
$C_S$ (OFF)	“OFF” Switch Source Capacitance.		
$C_D$ (OFF)	“OFF” Switch Drain Capacitance.		

**PIN CONFIGURATION**

**DIP/SOIC/SSOP**



# ADG333A—Typical Performance Graphs

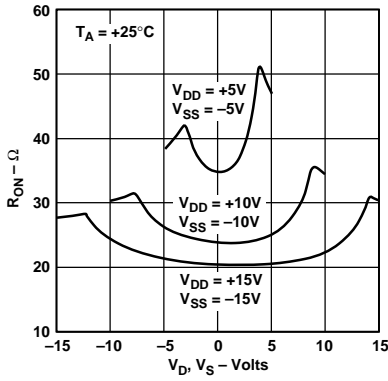


Figure 1.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Dual Supply

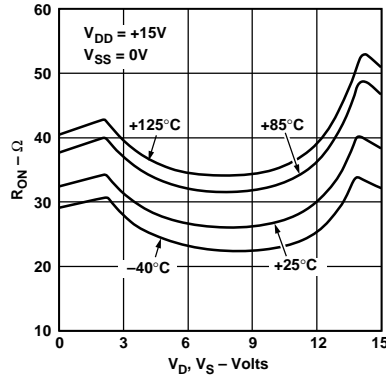


Figure 4.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures: Single Supply

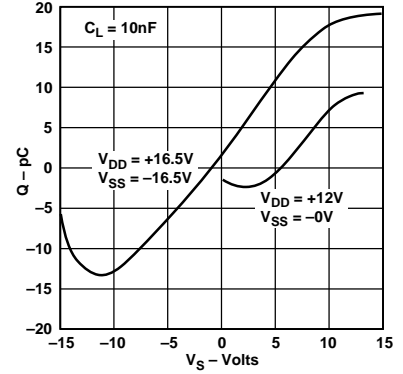


Figure 7. Charge Injection as a Function of  $V_S$

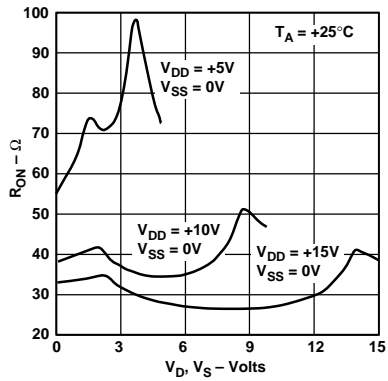


Figure 2.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Single Power Supply

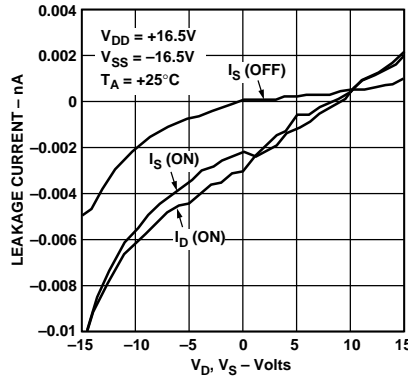


Figure 5. Leakage Currents as a Function of  $V_D$  ( $V_S$ ): Dual Supply

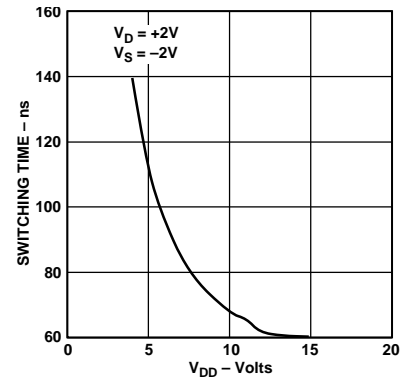


Figure 8. Switching Time as a Function of  $V_{DD}$

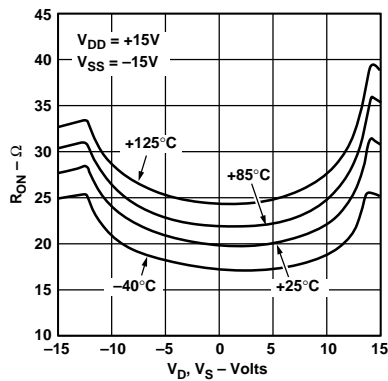


Figure 3.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures: Dual Supply

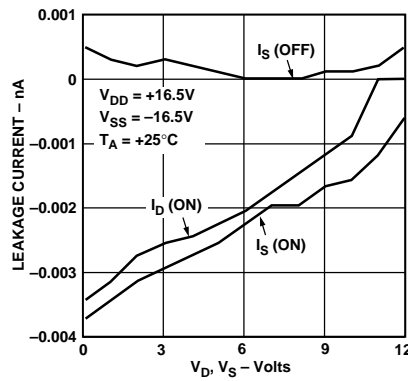


Figure 6. Leakage Currents as a Function of  $V_D$  ( $V_S$ ): Single Supply

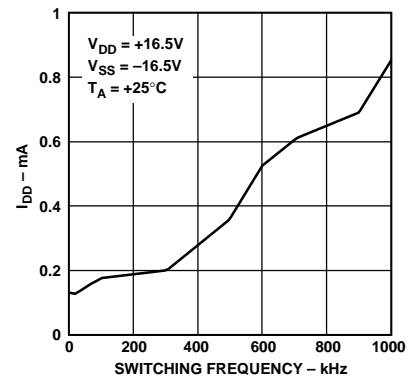
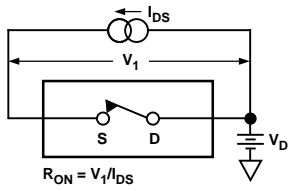
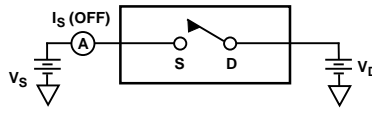


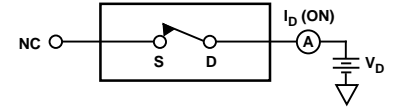
Figure 9.  $I_{DD}$  as a Function of Switching Frequency



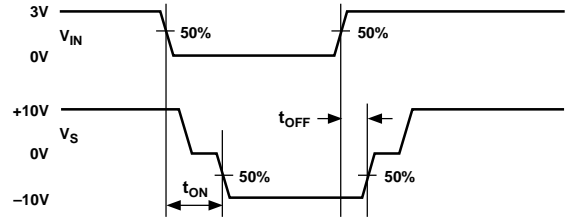
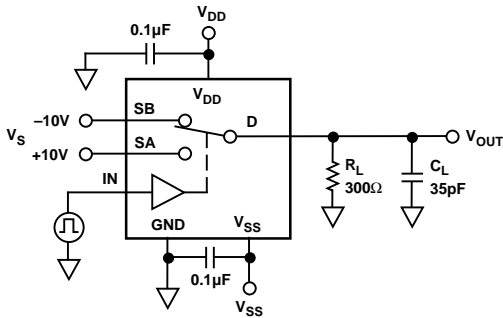
Test Circuit 1. On Resistance



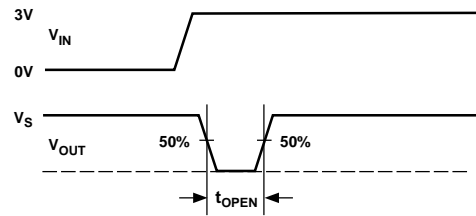
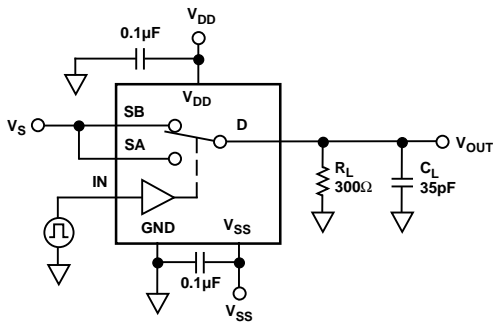
Test Circuit 2. Off Leakage



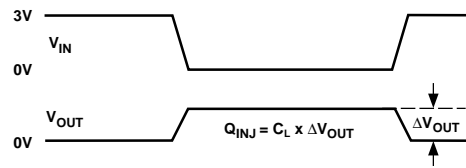
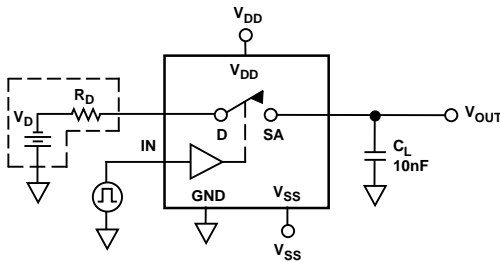
Test Circuit 3. On Leakage



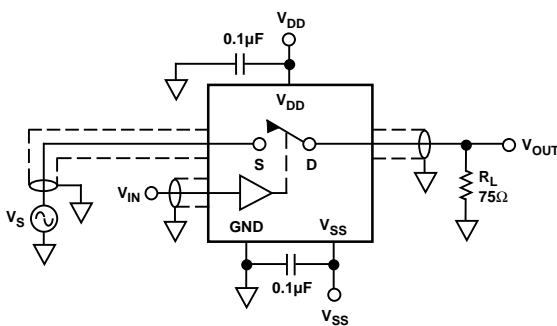
Test Circuit 4. Switching Times



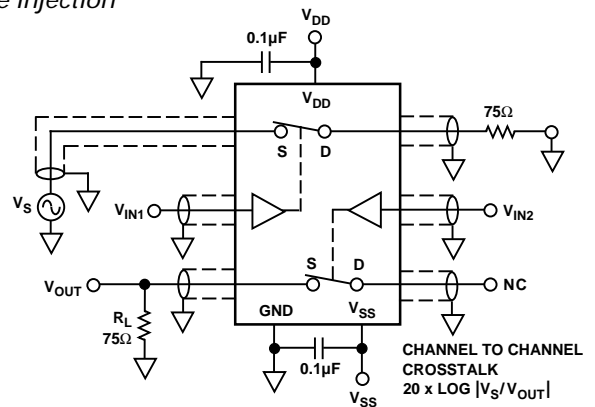
Test Circuit 5. Break-Before-Make Delay,  $t_{OPEN}$



Test Circuit 6. Charge Injection



Test Circuit 7. Off Isolation



Test Circuit 8. Channel-to-Channel Crosstalk

# ADG333A

## APPLICATIONS INFORMATION

### ADG333A Supply Voltages

The ADG333A can operate off a dual or signal supply.  $V_{SS}$  should be connected to GND when operating with a single supply. When using a dual supply the ADG333A can also operate with unbalanced supplies, for example  $V_{DD} = 20\text{ V}$  and  $V_{SS} = -5\text{ V}$ . The only restrictions are that  $V_{DD}$  to GND must not exceed 30 V,  $V_{SS}$  to GND must not drop below -30 V and  $V_{DD}$  to  $V_{SS}$  must not exceed +44 V. It is important to remember that the ADG333A supply voltage directly affects the input signal range, the switch ON resistance and the switching times of the part. The effects of the power supplies on these characteristics

can be clearly seen from the characteristic curves in this data sheet.

### Power Supply Sequencing

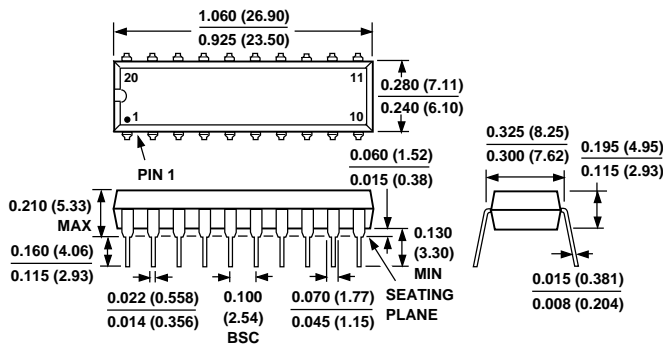
When using CMOS devices care must be taken to ensure correct power-supply sequencing. Incorrect power-supply sequencing can result in the device being subjected to stresses beyond those maximum ratings listed in the data sheet. This is also true for the ADG333A. Always sequence  $V_{DD}$  on first followed by  $V_{SS}$  and the logic signals. An external signal within the maximum specified ratings can then be safely presented to the source or drain of the switch

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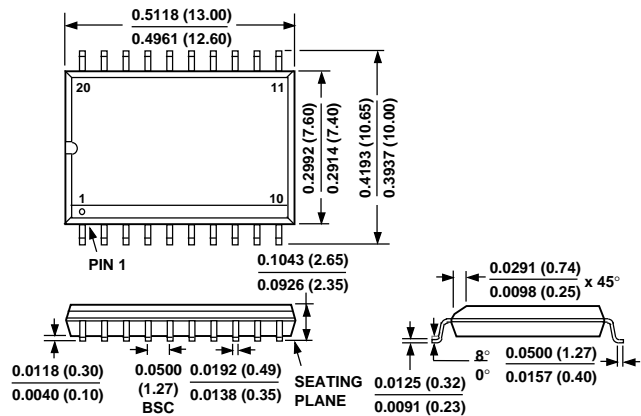
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

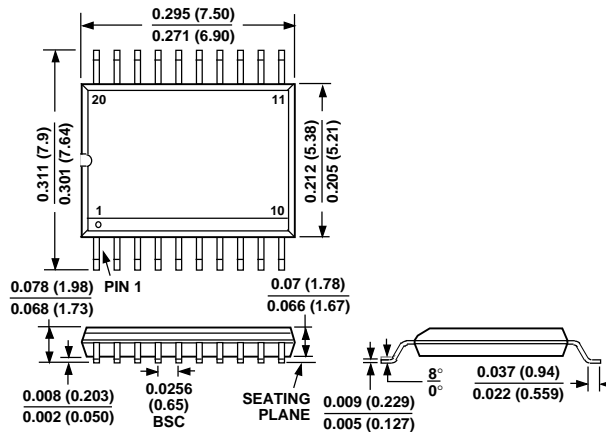
### 20-Pin Plastic DIP (N-20)



### 20-Pin SOIC (R-20)



### 20-Pin SSOP (RS-20)



LEADS WILL BE EITHER TIN PLATED OR SOLDIER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

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